Dec, 2020

# SCB13H8Gxx2BF
# SCB15H8Gxx2BF

**8Gbit DDR3(L) SDRAM**
**EU RoHS Compliant Products**

# Data Sheet

**Rev. D**

| Revision History | | |
|---|---|---|
| **Date** | **Revision** | **Subjects (major changes since last revision)** |
| 2019-01 | A | Initial Release |
| 2019-05 | B | Add the feature ASR & PASR<br>Update the Timing Parameters by Speed Grade |
| 2020-07 | C | Add MRS,DC/AC Information |
| 2020-12 | D | Modify POD |
| | | |

**We Listen to Your Comments**
Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to:
info@unisemicon.com

# Contents

Contents ........ 3
1 Features ........ 4
2 Product List ........ 5
3 Ball configuration ........ 6
4 Ball Description ........ 8
5 Functional Description ........ 10
5.1 Truth Tables ........ 10
5.2 Mode Register 0 (MR0) ........ 13
5.3 Mode Register 1 (MR1) ........ 15
5.4 Mode Register 2 (MR2) ........ 17
5.5 Mode Register 3 (MR3) ........ 19
5.6 Burst Order ........ 20
6 Operating Conditions and Interface Specification ........ 21
6.1 Absolute Maximum Ratings ........ 21
6.2 Operating Conditions ........ 22
6.3 Interface Test Conditions ........ 23
6.4 Voltage Levels ........ 24
6.4.1 DC and AC Logic Input Levels ........ 24
6.4.2 DC and AC Output Measurements Levels ........ 26
6.5 Output Slew Rates ........ 27
6.6 ODT DC Impedance and Mid-Level Characteristics ........ 28
6.7 ODT DC Impedance Sensitivity on Temperature and Voltage Drifts ........ 28
6.8 Interface Capacitance ........ 29
6.9 Overshoot and Undershoot Specification ........ 30
7 Electrical Specifications ........ 32
8 Speed Bin ........ 33
9 Electrical Characteristics & Timing ........ 36
9.1 Reference Load for AC Timing and Output Slew Rate ........ 36
9.2 Timing Parameters by Speed Grade ........ 37
10 Package Outlines ........ 47
11 Product Type Nomenclature ........ 49
List of Figures ........ 50
List of Tables ........ 51

# 1 Features

The 8Gbit DDR3(L) SDRAM offers the following key features:

- Density : 8G bits
- Organization :
- 128M words x 8 bits x 8 banks
- 64M words x 16 bits x 8 banks &
- Package :
- 78-ball FBGA(x8)
- 96-ball FBGA(x16)
- Two 1Gbit x 4 dies stacked(x8)
- Two 512Mbit x 8 dies stacked (x16)
- Lead-free (RoHS compliant) and Halogen-free
- Power supply : VDD, VDDQ = 1.35V±0.075V

Backward-compatible to VDD , VDDQ = 1.5V ±0.075V

- Data rate : 1600Mbps/1866Mbps
- 2KB page size
- Row address: A0 to A15
- Column address: A0 to A9, A11（x8）
- Eight internal banks for concurrent operation
- Burst lengths (BL) : 8 and 4 with Burst Chop (BC)
- Burst type (BT) :
- Sequential (8, 4 with BC)
- Interleave (8, 4 with BC)
- CAS Latency (CL) : 5, 6, 7, 8, 9, 10, 11, 13
- CAS Write Latency (CWL) : 5, 6, 7, 8 ,9
- Precharge : auto precharge option for each burst access
- Driver strength : RZQ/7, RZQ/6 (RZQ = 240 Ω)
- Refresh : auto-refresh, self-refresh
- Refresh cycles :
- Average refresh period

  7.8us at 0℃≤Tc≤85℃

  3.9us at 85℃≤Tc≤95℃
- Operating case temperature range

  Comercial Tc = 0°C to +95°C

  Industrial Tc = -40°C to +95°C
- Double-data-rate architecture; two data transfers per clock cycle
- The high-speed data transfer is realized by the 8 bits prefetch pipe- lined architecture
- Bi-directional differential data strobe (DQS and DQS/) is transmitted/ received with data for capturing data at the receiver
- DQS is edge-aligned with data for READs; center-aligned with data

  for WRITEs
- Differential clock inputs (CK and CK)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Data mask (DM) for write data
- Posted CAS by programmable additive latency for better command and data bus efficiency
- On-Die Termination (ODT) for better signal quality
- Synchronous ODT
- Dynamic ODT
- Asynchronous ODT
- Multi Purpose Register (MPR) for pre-defined pattern read out
- ZQ calibration for DQ drive and ODT
- RESET/ pin for Power-up sequence and reset function
- SRT range : Normal/extended
- ASR support
- PASR support
- Programmable Output driver impedance control

# 2 Product List

**Table 1** shows all possible products within the 8Gbit DDR3(L) SDRAM component generation.

**Table 1 - Ordering Information for 8Gbit DDR3(L) Component**

| UniIC Part Number | Max.Clock frequency | CAS-RCD-RP latencies | Speed Sort Name | Package |
|---|---|---|---|---|
| **8Gbit DDR3(L) SDRAM Components in × 8 Organization (1024M × 8)** | | | | |
| **Commercial Temperature Rang(0℃~+95℃)** | | | | |
| SCB13H8G802BF-13K | 800MHz | 11-11-11 | DDR3L–1600K | PG-FBGA-78 |
| SCB13H8G802BF-11M | 933 MHz | 13-13-13 | DDR3L–1866M | PG-FBGA-78 |
| **Industrial Temperature Rang(-40°C ~ +95°C)** | | | | |
| SCB13H8G802BF-13KI | 800MHz | 11-11-11 | DDR3L–1600K | PG-FBGA-78 |
| SCB13H8G802BF-11MI | 933 MHz | 13-13-13 | DDR3L–1866M | PG-FBGA-78 |
| **Commercial Temperature Rang(0℃~+95℃)** | | | | |
| SCB15H8G802BF-13K | 800MHz | 11-11-11 | DDR3–1600K | PG-FBGA-78 |
| SCB15H8G802BF-11M | 933 MHz | 13-13-13 | DDR3–1866M | PG-FBGA-78 |
| **Industrial Temperature Rang(-40°C ~ +95°C)** | | | | |
| SCB15H8G802BF-13KI | 800MHz | 11-11-11 | DDR3–1600K | PG-FBGA-78 |
| SCB15H8G802BF-11MI | 933 MHz | 13-13-13 | DDR3–1866M | PG-FBGA-78 |
| **8Gbit DDR3(L) SDRAM Components in × 16 Organization (512M × 16)** | | | | |
| **Commercial Temperature Rang(0℃~+95℃)** | | | | |
| SCB13H8G162BF-13K | 800MHz | 11-11-11 | DDR3L–1600K | PG-FBGA-96 |
| SCB13H8G162BF-11M | 933 MHz | 13-13-13 | DDR3L–1866M | PG-FBGA-96 |
| **Industrial Temperature Rang(-40°C ~ +95°C)** | | | | |
| SCB13H8G162BF-13KI | 800MHz | 11-11-11 | DDR3L–1600K | PG-FBGA-96 |
| SCB13H8G162BF-11MI | 933 MHz | 13-13-13 | DDR3L–1866M | PG-FBGA-96 |
| **Commercial Temperature Rang(0℃~+95℃)** | | | | |
| SCB15H8G162BF-13K | 800MHz | 11-11-11 | DDR3–1600K | PG-FBGA-96 |
| SCB15H8G162BF-11M | 933 MHz | 13-13-13 | DDR3–1866M | PG-FBGA-96 |
| **Industrial Temperature Rang(-40°C ~ +95°C)** | | | | |
| SCB15H8G162BF-13KI | 800MHz | 11-11-11 | DDR3–1600K | PG-FBGA-96 |
| SCB15H8G162BF-11MI | 933 MHz | 13-13-13 | DDR3–1866M | PG-FBGA-96 |

# 3 Ball configuration

**Figure 1 - Ball out for 1024 Mb ×8 Components (FBGA-78)**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | |
|---|---|---|---|---|---|---|---|---|---|---|
| A | $V_{SS}$ | $V_{DD}$ | NC | | | | NC | $V_{SS}$ | $V_{DD}$ | A |
| B | $V_{SS}$ | $V_{SSQ}$ | DQ0 | | | | DM | $V_{SSQ}$ | $V_{DDQ}$ | B |
| C | $V_{DDQ}$ | DQ2 | DQS | | | | DQ1 | DQ3 | $V_{SSQ}$ | C |
| D | $V_{SSQ}$ | DQ6 | $\overline{DQS}$ | | | | $V_{DD}$ | $V_{SS}$ | $V_{SSQ}$ | D |
| E | $V_{REFDQ}$ | $V_{DDQ}$ | DQ4 | | | | DQ7 | DQ5 | $V_{DDQ}$ | E |
| F | NC | $V_{SS}$ | $\overline{RAS}$ | | | | CK | $V_{SS}$ | NC | F |
| G | ODT | $V_{DD}$ | $\overline{CAS}$ | | | | $\overline{CK}$ | $V_{DD}$ | CKE | G |
| H | NC | $\overline{CS}$ | $\overline{WE}$ | | | | A10/AP | ZQ | NC | H |
| J | $V_{SS}$ | BA0 | BA2 | | | | A15 | $V_{REFCA}$ | $V_{SS}$ | J |
| K | $V_{DD}$ | A3 | A0 | | | | A12/$\overline{BC}$ | BA1 | $V_{DD}$ | K |
| L | $V_{SS}$ | A5 | A2 | | | | A1 | A4 | $V_{SS}$ | L |
| M | $V_{DD}$ | A7 | A9 | | | | A11 | A6 | $V_{DD}$ | M |
| N | $V_{SS}$ | $\overline{RESET}$ | A13 | | | | A14 | A8 | $V_{SS}$ | N |

Ball Locations (x8)

● Populated ball

+ Ball not populated

**Top view**

(See the balls through the package)

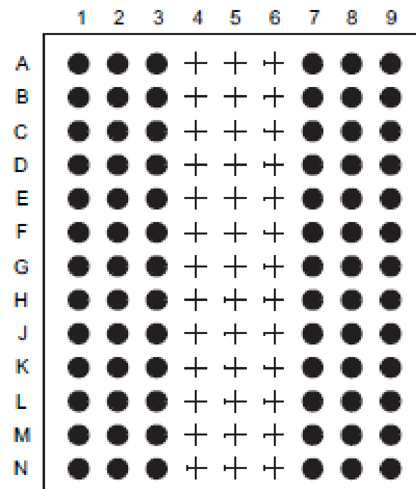


**Figure 2 - Ball out for 512 Mb ×16 Components (FBGA-96)**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | |
|---|---|---|---|---|---|---|---|---|---|---|
| A | $V_{DDQ}$ | DQU5 | DQU7 | | | | DQU4 | $V_{DDQ}$ | $V_{SS}$ | A |
| B | $V_{SSQ}$ | $V_{DD}$ | $V_{SS}$ | | | | $\overline{DQSU}$ | DQU6 | $V_{SSQ}$ | B |
| C | $V_{DDQ}$ | DQU3 | DQU1 | | | | DQSU | DQU2 | $V_{DDQ}$ | C |
| D | $V_{SSQ}$ | $V_{DDQ}$ | DMU | | | | DQU0 | $V_{SSQ}$ | $V_{DD}$ | D |
| E | $V_{SS}$ | $V_{SSQ}$ | DQL0 | | | | DML | $V_{SSQ}$ | $V_{DDQ}$ | E |
| F | $V_{DDQ}$ | DQL2 | DQSL | | | | DQL1 | DQL3 | $V_{SSQ}$ | F |
| G | $V_{SSQ}$ | DQL6 | $\overline{DQSL}$ | | | | $V_{DD}$ | $V_{SS}$ | $V_{SSQ}$ | G |
| H | $V_{REFDQ}$ | $V_{DDQ}$ | DQL4 | | | | DQL7 | DQL5 | $V_{DDQ}$ | H |
| J | NC | $V_{SS}$ | $\overline{RAS}$ | | | | CK | $V_{SS}$ | NC | J |
| K | ODT | $V_{DD}$ | $\overline{CAS}$ | | | | $\overline{CK}$ | $V_{DD}$ | CKE | K |
| L | NC | $\overline{CS}$ | $\overline{WE}$ | | | | A10/AP | ZQ | NC | L |
| M | $V_{SS}$ | BA0 | BA2 | | | | A15 | $V_{REFCA}$ | $V_{SS}$ | M |
| N | $V_{DD}$ | A3 | A0 | | | | A12/$\overline{BC}$ | BA1 | $V_{DD}$ | N |
| P | $V_{SS}$ | A5 | A2 | | | | A1 | A4 | $V_{SS}$ | P |
| R | $V_{DD}$ | A7 | A9 | | | | A11 | A6 | $V_{DD}$ | R |
| T | $V_{SS}$ | $\overline{RESET}$ | A13 | | | | A14 | A8 | $V_{SS}$ | T |

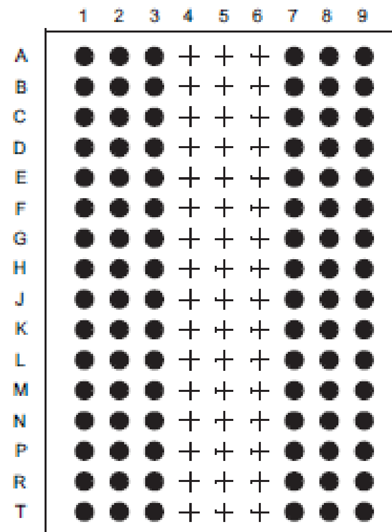
Ball Locations (x16)

● Populated ball

\+ Ball not populated

**Top view**

(See the balls through the package)



# 4 Ball Description

**Table 2 - Ball out for 512 Mb ×16 Components (FBGA-96)**

| Pin | Type | Function |
|---|---|---|
| CK, $\overline{\text{CK}}$ | Input | **Clock :** CK and $\overline{\text{CK}}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK. Output (read) data is referenced to the crossings of CK and CK |
| CKE | Input | **Clock Enable :** CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self Refresh oper- ation (all banks idle), or Active Power-Down (Row Active in any bank). CKE is asynchronous for self refresh exit. After $V_{REFCA}$ has become stable during the power on and initialization sequence, it must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{\text{CK}}$, ODT and CKE are disabled during power- down. Input buffers, excluding CKE, are disabled during Self -Refresh. |
| $\overline{\text{CS}}$ | Input | **Chip Select :** All commands are masked when $\overline{\text{CS}}$ is registered HIGH. $\overline{\text{CS}}$ provides for external Rank selection on systems with multiple Ranks. CS is considered part of the command code. |
| ODT | Input | **On Die Termination :** ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is only applied to each DQ, DQS, DQS and DM. The ODT pin will be ignored if the Mode Register (MR1) is programmed to disable ODT. |
| $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$ | Input | **Command Inputs :** $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ (along with $\overline{\text{CS}}$) define the command being entered. |
| DM | Input | **Input Data Mask :** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. |
| BA0 - BA2 | Input | **Bank Address Inputs :** BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle. |
| A0 - A15 | Input | **Address Inputs :** Provided the row address for Active commands and the column address for Read / Write commands to select one location out of the memory array in the respective bank. (A10/AP and A12/BC have additional functions, see below)<br>The address inputs also provide the op-code during Mode Register Set commands. |
| A10 / AP | Input | **Autoprecharge :** A10 is sampled during Read/Write commands to determine whether Autoprecharge should be per-formed to the accessed bank after the Read/Write operation. (HIGH:Autoprecharge; LOW: No Autoprecharge)A10 is sampled during a Precharge command to determine whether the Pre- charge applies to one bank (A10 LOW) or all banks (A10 HIGH). if only one bank is to be precharged, the bank is selected by bank addresses. |
| A12 / $\overline{\text{BC}}$ | Input | **Burst Chop :** A12 is sampled during Read and Write commands to determine if burst chop(on-the-fly) will be per-formed. (HIGH : no burst chop, LOW : burst chopped). See command truth table for details. |
| $\overline{\text{RESET}}$ | Input | **Active Low Asynchronous Reset :** Reset is active when RESET is LOW, and inactive when RESET is HIGH. RESET must be HIGH during normal operation. RESET is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD, i.e. 1.20V for DC high and 0.30V for DC low. |
| DQ | Input/ Output | **Data Input/ Output :** Bi-directional data bus. |
| DQS, $\overline{\text{DQS}}$ | Input/ Output | **Data Strobe :** Output with read data, input with write data. Edge-aligned with read data, centered in write data. The data strobe DQS is paired with differential signals DQS, respectively, to provide differ- ential pair signaling to the system during reads and writes. DDR3 SDRAM supports differential data strobe only and does not support single-ended. |
| NC | | No Connect: No internal electrical connection is present. |

| Pin | Type | Function |
|---|---|---|
| VDDQ | Supply | DQ power supply: 1.35V ,1.283 - 1.45V operational; compatible to 1.5+/- 0.075V operation |
| VSSQ | Supply | DQ Ground |
| VDD | Supply | Power Supply: 1.5V ,1.283 - 1.45V operational; compatible to 1.5+/- 0.075V operation |
| VSS | Supply | Ground |
| VREFDQ | Supply | Reference Voltage for DQ |
| VREFCA | Supply | Reference Voltage for CA |
| ZQ | Supply | Reference Pin for ZQ calibration |
| Note: Input only pins ( BA0-BA2, A0-A15, RAS, CAS, WE, CS, CKE, ODT and RESET ) do not supply termination | | |

# 5 Functional Description

## 5.1 Truth Tables

The truth tables list the input signal values at a given clock edge which represent a command or state transition expected to be executed by the DDR3L SDRAM. **Table 3** lists all valid commands to the DDR3L SDRAM. For a detailed description of the various power mode entries and exits please refer to **Table 4**. In addition, the DM functionality is described in **Table 5**.

**Table 3 - Command Truth Table**

| Function | Abbr. | CKE | | /CS | /RAS | /CAS | /WE | BA2 - BA0 | A13-A15 | A12\|/BC | A10\|AP | A11, A9-A0 | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Prev. Cycle | Curr. Cycle | | | | | | | | | | |
| Mode Register Set | MRS | H | H | L | L | L | L | BA | OP Code | | | | 1)2)3)4)5) |
| Refresh | REF | H | H | L | L | L | H | V | V | V | V | V | 1)2)3)4)5) |
| Self-Refresh Entry | SRE | H | L | L | L | L | H | V | V | V | V | V | 1)2)3)4)5)6)7)8) |
| Self-Refresh Exit | SRX | L | H | H | V | V | V | V | V | V | V | V | 1)2)3)4)5)6)7)8)9) |
| | | | | L | H | H | H | | | | | | |
| Single Bank Precharge | PRE | H | H | L | L | H | L | BA | V | V | L | V | 1)2)3)4)5) |
| Precharge all Banks | PREA | H | H | L | L | H | L | V | V | V | H | V | 1)2)3)4)5) |
| Active | ACT | H | H | L | L | H | H | BA | RA (Row Address) | | | | 1)2)3)4)5) |
| Write (BL8MRS or BC4MRS) | WR | H | H | L | H | L | L | BA | V | V | L | CA | 1)2)3)4)5)10) |
| Write (BC4OTF) | WRS4 | H | H | L | H | L | L | BA | V | L | L | CA | 1)2)3)4)5)10) |
| Write (BL8OTF) | WRS8 | H | H | L | H | L | L | BA | V | H | L | CA | 1)2)3)4)5)10) |
| Write w/AP (BL8MRS or BC4MRS) | WRA | H | H | L | H | L | L | BA | v | V | H | CA | 1)2)3)4)5)10) |
| Write w/AP (BC4OTF) | WRAS4 | H | H | L | H | L | L | BA | V | L | H | CA | 1)2)3)4)5)10) |
| Write w/AP (BL8OTF) | WRAS8 | H | H | L | H | L | L | BA | V | H | H | CA | 1)2)3)4)5)10) |
| Read (BL8MRS or BC4MRS) | RD | H | H | L | H | L | H | BA | V | V | L | CA | 1)2)3)4)5)10) |
| Read (BC4OTF) | RDS4 | H | H | L | H | L | H | BA | V | L | L | CA | 1)2)3)4)5)10) |
| Read (BL8OTF) | RDS8 | H | H | L | H | L | H | BA | V | H | L | CA | 1)2)3)4)5)10) |
| Read w/AP (BL8MRS or BC4MRS) | RDA | H | H | L | H | L | H | BA | V | V | H | CA | 1)2)3)4)5)10) |
| Read w/AP (BC4OTF) | RDAS4 | H | H | L | H | L | H | BA | V | L | H | CA | 1)2)3)4)5)10) |
| Read w/AP (BL8OTF) | RDAS8 | H | H | L | H | L | H | BA | V | H | H | CA | 1)2)3)4)5)10) |
| No Operation | NOP | H | H | L | H | H | H | V | V | V | V | V | 1)2)3)4)5)11) |

| Function | Abbr. | CKE | | CS | RAS | CAS | WE | BA2 - BA0 | A13 A14 A15 | A12\| /BC | A10/ AP | A11, A9-A0 | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Prev. Cycle | Curr. Cycle | | | | | | | | | | |
| Device Deselect | DES | H | H | H | X | X | X | X | X | X | X | X | 1)2)3)4)5)12) |
| Power Down Entry | PDE | H | L | L | H | H | H | V | V | V | V | V | 1)2)3)4)5)8)13) |
| | | | | H | V | V | V | | | | | | |
| Power Down Exit | PDX | L | H | L | H | H | H | V | V | V | V | V | 1)2)3)4)5)8)13) |
| | | | | H | V | V | V | | | | | | |
| ZQ Calibration Short | ZQCS | H | H | L | H | H | L | X | X | X | L | X | 1)2)3)4)5) |
| ZQ Calibration Long | ZQCL | H | H | L | H | H | L | X | X | X | H | X | 1)2)3)4)5) |

1) BA = Bank Address, RA = Row Address, CA = Column Address, BC = Burst Chop, AP = Auto Precharge, X = Don't care, V = valid
2) All DDR3L SDRAM commands are defined by states of /CS, /RAS, /CAS, /WE and CKE at the rising edge of the clock. The higher order address bits of BA, RA and CA are device density and IO configuration (×4, ×8, ×16) dependent.
3) /RESET is a low active signal which will be used only for asynchronous reset. It must be maintained High during any function.
4) Bank addresses (BA) determine which bank is to be operated upon. For MRS, BA selects a Mode Register.
5) V means H or L (but a defined logic level) and X means either "defined or undefined (like floating) logic level".
6) The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh
7) $V_{REF}$ (both $V_{REFCA}$ and $V_{REFDQ}$) must be maintained during Self Refresh operation.
8) Refer to **"Clock Enable (CKE) Truth Table for Synchronous Transitions" on Page 12** for more detail with CKE transition.
9) Self refresh exit is asynchronous.
10) Burst reads or writes cannot be terminated or interrupted and Fixed/on-the-Fly BL will be defined by MRS.
11) The No Operation (NOP) command should be used in cases when the DDR3L SDRAM is in an idle or a wait state. The purpose of the NOP command is to prevent the DDR3L SDRAM from registering any unwanted commands between operations. A NOP command will not terminate a previous operation that is still executing, such as a read or write burst.
12) The Deselect command (DES) performs the same function as a No Operation command.
13) The Power Down Mode does not perform any refresh operation.

### Table 4 - Clock Enable (CKE) Truth Table for Synchronous Transitions

| Current State [1] | CKE(N-1)[2] Previous Cycle | CKE(N)[2] Current Cycle | Command (N)[3] /RAS, /CAS, /WE, /CS | Action (N)[3] | Note |
|---|---|---|---|---|---|
| Power Down | L | L | X | Maintain Power Down | 4)5)6)7)8)9) |
| | L | H | DES or NOP | Power Down Exit | 4)5)6)7)8)10) |
| Self Refresh | L | L | X | Maintain Self Refresh | 4)5)6)7)9)11) |
| | L | H | DES or NOP | Self Refresh Exit | 4)5)6)7)11)12)13) |
| Bank(s) Active | H | L | DES or NOP | Active Power Down Entry | 4)5)6)7)8)10)14) |
| Reading | H | L | DES or NOP | Power Down Entry | 4)5)6)7)8)10)14)15) |
| Writing | H | L | DES or NOP | Power Down Entry | 4)5)6)7)8)10)14)15) |
| Precharging | H | L | DES or NOP | Power Down Entry | 4)5)6)7)8)10)14)15) |
| Refreshing | H | L | DES or NOP | Precharge Power Down Entry | 4)5)6)7)10) |
| All Banks Idle | H | L | DES or NOP | Precharge Power Down Entry | 4)5)6)7)10)8)14)16) |
| | H | L | REF | Self Refresh Entry | 4)5)6)7)14)16)17) |
| Any other state | Refer to **"Command Truth Table" on Page 10** for more detail with all command signals | | | | 4)5)6)7)18) |

1) Current state is defined as the state of the DDR3L SDRAM immediately prior to clock edge N.
2) CKE(N) is the logic state of CKE at clock edge N; CKE (N-1) was the state of CKE at the previous clock edge.
3) COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N),ODT is not included here.
4) All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
5) The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
6) CKE must be registered with the same value on $t_{CKE.MIN}$ consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the $t_{CKE.MIN}$ clocks of registeration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of $t_{IS} + t_{CKE.MIN} + t_{IH}$.
7) DES and NOP are defined in **"Command Truth Table" on Page 10**.
8) The Power Down does not perform any refresh operations
9) X means Don't care (including floating around $V_{REFCA}$) in Self Refresh and Power Down. It also applies to address pins.
10) Valid commands for Power Down Entry and Exit are NOP and DES only
11) $V_{REF}$ (both $V_{REFCA}$ and $V_{REFDQ}$) must be maintained during Self Refresh operation.
12) On Self Refresh Exit DES or NOP commands must be issued on every clock edge occurring during the $t_{XS}$ period. Read, or ODT commands may be issued only after $t_{XSDLL}$ is satisfied.
13) Valid commands for Self Refresh Exit are NOP and DES only.
14) Self Refresh can not be entered while Read or Write operations are in progress.
15) If all banks are closed at the conclusion of a read, write or precharge command then Precharge Power-down is entered, otherwise Active Power-down is entered.
16) 'Idle state' is defined as all banks are closed ($t_{RP}$, $t_{DAL}$, etc. satisfied), no data bursts are in progress, CKE is High, and all timings from previous operations are satisfied ($t_{MRD}$, $t_{MOD}$, $t_{RFC}$, $t_{ZQ.INIT}$, $t_{ZQ.OPER}$, $t_{ZQCS}$, etc.) as well as all Self-Refresh exit and Power-Down Exit parameters are satisfied ($t_{XS}$, $t_{XP}$, $t_{XPDLL}$, etc.).
17) Self Refresh mode can only be entered from the All Banks Idle state.
18) Must be a legal command as defined in **"Command Truth Table" on Page 10**.

### Table 5 - Data Mask (DM) Truth Table

| Name (Function) | DM | DQs |
|---|---|---|
| Write Enable | L | Valid |
| Write Inhibit | H | X |

## 5.2 Mode Register 0 (MR0)

The mode register MR0 stores the data for controlling various operating modes of DDR3L SDRAM. It controls burst length, read burst type, CAS latency, test mode, DLL reset, WR (write recovery time for auto-precharge) and DLL control for precharge Power-Down, which includes various vendor specific options to make DDR3L SDRAM useful for various applications. The mode register is written by asserting Low on /CS, /RAS, /CAS, /WE, BA0, BA1, and BA2, while controlling the states of address pins according to **Table 6**.

| BA2 | BA1 | BA0 | A15-A13 | A12 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **0** | **0** | **0** | **0**[1)] | **PPD** | **WR** | | | **DLL** | **TM** | **CL** | | | **RBT** | **CL** | **BL** | |

**Table 6 - MR0 Mode register Definition (BA[2:0]=000B)**

| Field | Bits[1)] | Description |
|---|---|---|
| BL | A[1:0] | **Burst Length (BL) and Control Method**<br>Number of sequential bits per DQ related to one Read/Write command.<br>$00_B$ **BL8MRS** mode with fixed burst length of 8. A12 \| /BC at Read or Write command time is Don't care at read or write command time.<br>$01_B$ **BLOTF** on-the-fly (OTF) enabled using A12 \| /BC at Read or Write command time. When A12 \| /BC is High during Read or Write command time a burst length of 8 is selected (BL8OTF mode). When A12 \| /BC is Low, a burst chop of 4 is selected (BC4OTF mode). Auto-Precharge can be enabled or disabled.<br>$10_B$ **BC4MRS** mode with fixed burst chop of 4 with $t_{CCD} = 4 \times n_{CK}$. A12 \| /BC is Don't care at Read or Write command time.<br>$11_B$ **TBD** Reserved |
| RBT | A3 | **Read Burst Type**<br>$0_B$ Nibble Sequential<br>$1_B$ Interleaved |
| CL | A[6:4,2] | **CAS Latency (CL)**<br>CAS Latency is the delay, in clock cycles, between the internal Read command and the availability of the first bit of output data.<br>*Note: For more information on the supported CL and AL settings based on the operating clock frequency, refer to **"Speed Bins" on Page 33**.*<br>*Note: All other bit combinations are reserved.*<br>$0000_B$ RESERVED<br>$0010_B$ 5<br>$0100_B$ 6<br>$0110_B$ 7<br>$1000_B$ 8<br>$1010_B$ 9<br>$1100_B$ 10<br>$1110_B$ 11 |

| Field | Bits[1)] | Description |
|---|---|---|
| TM | A7 | **Test Mode**<br>The normal operating mode is selected by MR0(bit A7 = 0) and all other bits set to the desired values shown in this table. Programming bit A7 to a 1 places the DDR3L SDRAM into a test mode that is only used by the SDRAM manufacturer and should NOT be used. No operations or functionality is guaranteed if A7 = 1.<br>$0_B$ Normal Mode<br>$1_B$ Vendor specific test mode |
| DLLres | A8 | **DLL Reset**<br>The internal DLL Reset bit is self-clearing, meaning it returns back to the value of 0 after the DLL reset function has been issued. Once the DLL is enabled, a subsequent DLL Reset should be applied. Any time the DLL reset function is used, $t_{DLLK}$ must be met before any functions that require the DLL can be used (i.e. Read commands or synchronous ODT operations).<br>$0_B$ No DLL Reset<br>$1_B$ DLL Reset triggered |
| WR | A[11:9] | **Write Recovery for Auto-Precharge**<br>Number of clock cycles for write recovery during Auto-Precharge. $WR_{MIN}$ in clock cycles is calculated by dividing $t_{WR.MIN}$ (in ns) by the actual $t_{CK.AVG}$ (in ns) and rounding up to the next integer: WR.MIN [$n_{CK}$] = Roundup($t_{WR.MIN}$[ns] / $t_{CK.AVG}$[ns]). The WR value in the mode register must be programmed to be equal or larger than WR.MIN. The resulting WR value is also used with $t_{RP}$ to determine $t_{DAL}$. Since WR of 9 and 11 is not implemented in DDR3L and the above formula results in these values, higher values have to be programmed.<br>$000_B$ Reserved<br>$001_B$ 5<br>$010_B$ 6<br>$011_B$ 7<br>$100_B$ 8<br>$101_B$ 10<br>$110_B$ 12<br>$111_B$ Reserved |
| PPD | A12 | **Precharge Power-Down DLL Control**<br>Active Power-Down will always be with DLL-on. Bit A12 will have no effect in this case. For Precharge Power-Down, bit A12 in MR0 is used to select the DLL usage as shown below.<br>$0_B$ **Slow Exit.** DLL is frozen during precharge Power-down.Read and synchronous ODT commands are only allowed after $t_{XPDLL}$.<br>$1_B$ **Fast Exit.** DLL remains on during precharge Power-down.Any command can be applied after $t_{XP}$, provided that other timing parameters are satisfied. |

1) A13, A14 and A15 - even if not available on a specific device - must be programmed to $0_B$.

## 5.3 Mode Register 1 (MR1)

The Mode Register MR1 stores the data for enabling or disabling the DLL, output driver strength, $R_{TT}$_Nom impedance, additive latency (AL), Write leveling enable and Qoff (output disable). The Mode Register MR1 is written by asserting Low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, High on BA0 and Low on BA1and BA2, while controlling the states of address pins according to **Table 7.**

| BA2 | BA1 | BA0 | A15-A13 | A12 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **0** | **0** | **1** | **0**[1)] | **Qoff** | **0** | **0** | **RTT_ nom** | **0** | **Level** | **RTT_ nom** | **DIC** | **AL** | | **RTT_ nom** | **DIC** | **DLL** |

**Table 7 - MR1 Mode Register Definition (BA[2:0]=001$_B$)**

| Field | Bits[1)] | Description |
|---|---|---|
| DLLdis | A0 | **DLL Disable**<br>The DLL must be enabled for normal operation. DLL enable is required during power up initialization, after reset and upon returning to normal operation after having the DLL disabled. During normal operation (DLL-on) with MR1(A0 = 0), the DLL is automatically disabled when entering Self-Refresh operation and is automatically re-enabled and reset upon exit of Self-Refresh operation. Any time the DLL is enabled, a DLL reset must be issued afterwards. Any time the DLL is reset, $t_{DLLK}$ clock cycles must occur before a Read or synchronous ODT command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the $t_{DQSCK}$, $t_{AON}$, $t_{AOF}$ or $t_{ADC}$ parameters. During $t_{DLLK}$, CKE must continuously be registered high. DDR3L SDRAM does not require DLL for any Write operation.<br>$0_B$ DLL is enabled<br>$1_B$ DLL is disabled |
| DIC | A[5, 1] | **Output Driver Impedance Control**<br>*Note: All other bit combinations are reserved.*<br>00: RZQ/6<br>$01_B$ Nominal Drive Strength RON34 = RQZ/7 (nominal 34.3 Ω, with nominal RZQ = 240 Ω) |
| $R_{TT_NOM}$ | A[9, 6, 2] | **Nominal Termination Resistance of ODT**<br>**Notes**<br>1. *If $R_{TT_NOM}$ is used during Writes, only the values $R_{ZQ}$/2, $R_{ZQ}$/4 and $R_{ZQ}$/6 are allowed.*<br>2. *In Write leveling Mode (MR1[bit7] = 1) with MR1[bit12] = 1, all $R_{TT}$_Nom settings are allowed; in Write Leveling Mode (MR1[bit7] = 1) with MR1[bit12] = 0, only $R_{TT_NOM}$ settings of $R_{ZQ}$/2, $R_{ZQ}$/4 and $R_{ZQ}$/6 are allowed.*<br>3. *All other bit combinations are reserved.*<br>$000_B$ ODT disabled, $R_{TT_NOM}$ = off, Dynamic ODT mode disabled<br>$001_B$ RTT60 = RZQ / 4 (nominal 60 Ω with nominal RZQ = 240 Ω)<br>$010_B$ RTT120 = RZQ / 2 (nominal 120 Ω with nominal RZQ = 240 Ω<br>$011_B$ RTT40 = RZQ / 6 (nominal 40 Ω with nominal RZQ = 240 Ω)<br>$100_B$ RTT20 = RZQ / 12 (nominal 20 Ω with nominal RZQ = 240 Ω)<br>$101_B$ RTT30 = RZQ / 8 (nominal 30 Ω with nominal RZQ = 240 Ω) |

| Field | Bits[1)] | Description |
|---|---|---|
| AL | A[4, 3] | **Additive Latency (AL)**<br>Any read or write command is held for the time of Additive Latency (AL) before it is issued as internal read or write command.<br><br>**Notes**<br>*1. AL has a value of CL - 1 or CL - 2 as per the CL value programmed in the MR0 register.*<br>$00_B$ AL = 0 (AL disabled)<br>$01_B$ AL = CL - 1<br>$10_B$ AL = CL - 2<br>$11_B$ Reserved |
| Write Leveling enable | A7 | **Write Leveling Mode**<br>$0_B$ **Write Leveling Mode** Disabled, Normal operation mode<br>$1_B$ **Write Leveling Mode** Enabled |
| TDQS enable | A11 | 0: Disabled<br>1: Enabled |
| Qoff | A12 | **Output Disable**<br>Under normal operation, the SDRAM outputs are enabled during read operation and write leveling for driving data (Qoff bit in the MR1 is set to $0_B$). When the Qoff bit is set to $1_B$, the SDRAM outputs (DQ, DQS, /DQS) will be disabled - also during write leveling. Disabling the SDRAM outputs allows users to run write leveling on multiple ranks and to measure $I_{DD}$ currents during Read operations, without including the output.<br>$0_B$ Output buffer enabled<br>$1_B$ Output buffer disabled |

1) A13, A14, A15 - even if not available on a specific device - must be programmed to $0_B$.

# 5.4 Mode Register 2 (MR2)

The Mode Register MR2 stores the data for controlling refresh related features, $R_{TT_WR}$ impedance, and CAS write latency. The Mode Register MR2 is written by asserting Low on CS, RAS, CAS, WE, High on BA1 and Low on BA0 and BA2, while controlling the states of address signals according to **Table 8**.

| BA2 | BA1 | BA0 | A15-A13 | A12 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **0** | **1** | **0** | **0**[1)] | **0** | **0** | **Rtt_WR** | | **0** | **SRT** | **ASR** | **CWL** | | | **PASR** | | |

**Table 8 - MR2 Mode Register Definition (BA[2:0]=010$_B$)**

| **Field** | **Bits**[1)] | **Description** |
|---|---|---|
| PASR | A[2:0] | **Partial Array Self Refresh (PASR)**<br>If PASR (Partial Array Self Refresh) is enabled, data located in areas of the array beyond the specified self refresh location may get lost if self refresh is entered. During non-self-refresh operation, data integrity will be maintained if $t_{REFI}$ conditions are met.<br>$000_B$ Full array (Banks $000_B$ - $111_B$)<br>$001_B$ Half Array(Banks $000_B$ - $011_B$)<br>$010_B$ Quarter Array(Banks $000_B$ - $001_B$)<br>$011_B$ 1/8th array (Banks $000_B$ )<br>$100_B$ 3/4 array(Banks $010_B$ - $111_B$)<br>$101_B$ Half array(Banks $100_B$ - $111_B$)<br>$110_B$ Quarter array(Banks $110_B$ - $111_B$)<br>$111_B$ 1/8th array(Banks $111_B$ ) |
| CWL | A[5:3] | **CAS Write Latency (CWL)**<br>Number of clock cycles from internal write command to first write data in.<br>*Note: All other bit combinations are reserved.*<br>$000_B$ 5 (3.3 ns $\geq t_{CK.AVG} \geq$ 2.5 ns)<br>$001_B$ 6 (2.5 ns > $t_{CK.AVG} \geq$ 1.875 ns)<br>$010_B$ 7 (1.875 ns > $t_{CK.AVG} \geq$ 1.5 ns)<br>$011_B$ 8 (1.5 ns > $t_{CK.AVG} \geq$ 1.25 ns)<br>*Note: Besides CWL limitations on $t_{CK.AVG}$, there are also $t_{AA.MIN/MAX}$ restrictions that need to be observed. For details, please refer to **Chapter 8**, **Speed Bins**.* |
| RFU | A6 | **0: Manual SR reference (SRT)**<br>**1: ASR enable (Optional)**. |

| Field | Bits[1)] | Description |
|---|---|---|
| SRT | A7 | **Self-Refresh Temperature Range (SRT)**<br>The SRT bit must be programmed to indicate $T_{OPER}$ during subsequent self refresh operation.<br>$0_B$ Normal operating temperature range<br>$1_B$ Extended operating temperature range |
| $R_{TT_WR}$ | A[10:9] | **Dynamic ODT mode and $R_{TT_WR}$ Pre-selection**<br><br>**Notes**<br>*1. All other bit combinations are reserved.*<br>*2. The $R_{TT_WR}$ value can be applied during writes even when $R_{TT_NOM}$ is disabled. During write leveling, Dynamic ODT is not available.*<br>$00_B$ Dynamic ODT mode disabled<br>$01_B$ Dynamic ODT mode enabled with $R_{TT_WR}$ = RZQ/4 = 60 Ω<br>$10_B$ Dynamic ODT mode enabled with $R_{TT_WR}$ = RZQ/2 = 120Ω |

1) A13, A14, A15 - even if not available on a specific device - must be programmed to $0_B$.

## 5.5 Mode Register 3 (MR3)

The Mode Register MR3 controls Multi-purpose registers and optional On-die thermal sensor (ODTS) feature. The Mode Register MR3 is written by asserting Low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, High on BA1 and BA0, and Low on BA2 while controlling the states of address signals according to **Table 9**

| BA2 | BA1 | BA0 | A15-A13 | A12 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **0** | **1** | **1** | **0**[1] | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **MPR** | **MPR loc** | |

**Table 9 - MR3 Mode Register Definition (BA[2:0]=$011_B$)**

| **Field** | **Bits**[1] | **Description** |
|---|---|---|
| MPR loc | A[1:0] | **Multi Purpose Register Location**<br>$00_B$ Pre-defined data pattern for read synchronization<br>$01_B$ RFU<br>$10_B$ RFU<br>$11_B$ ODTS On-Die Thermal sensor readout (optional) |
| MPR | A2 | **Multi Purpose Register Enable**<br>*Note: When MPR is disabled, MR3 A[1:0] will be ignored.*<br>$0_B$ MPR disabled, normal memory operation<br>$1_B$ Dataflow from the Multi Purpose register MPR |

1) A13, A14 and A15 - even if not available on a specific device - must be programmed to $0_B$.

## 5.6 Burst Order

Accesses within a given burst may be interleaved or nibble sequential depending on the programmed bit A3 in the mode register MR0.

Regarding read commands, the lower 3 column address bits CA[2:0] at read command time determine the start address for the read burst.

Regarding write commands, the burst order is always fixed. For writes with a burst length of 8, the inputs on the lower 3 column address bits CA[2:0] are ignored during the write command. For writes with a burst being chopped to 4, the input on column address 2 (CA[2]) determines if the lower or upper four burst bits are selected. In this case, the inputs on the lower 2 column address bits CA[1:0] are ignored during the write command.The following table shows burst order versus burst start address for reads and writes of bursts of 8 as well as of bursts of 4 operation (burst chop).

**Table 10 - Bit Order during Burst**

| Burst Length | READ/ WRITE | Starting Column Address | Burst Type = Sequential (Decimal) | Burst Type = Interleaved (Decimal) | Notes |
|---|---|---|---|---|---|
| 4 (chop) | READ | 0 0 0 | 0, 1, 2, 3, Z, Z, Z, Z | 0, 1, 2, 3, Z, Z, Z, Z | 1, 2 |
| | | 0 0 1 | 1, 2, 3, 0, Z, Z, Z, Z | 1, 0, 3, 2, Z, Z, Z, Z | 1, 2 |
| | | 0 1 0 | 2, 3, 0, 1, Z, Z, Z, Z | 2, 3, 0, 1, Z, Z, Z, Z | 1, 2 |
| | | 0 1 1 | 3, 0, 1, 2, Z, Z, Z, Z | 3, 2, 1, 0, Z, Z, Z, Z | 1, 2 |
| | | 1 0 0 | 4, 5, 6, 7, Z, Z, Z, Z | 4, 5, 6, 7, Z, Z, Z, Z | 1, 2 |
| | | 1 0 1 | 5, 6, 7, 4, Z, Z, Z, Z | 5, 4, 7, 6, Z, Z, Z, Z | 1, 2 |
| | | 1 1 0 | 6, 7, 4, 5, Z, Z, Z, Z | 6, 7, 4, 5, Z, Z, Z, Z | 1, 2 |
| | | 1 1 1 | 7, 4, 5, 6, Z, Z, Z, Z | 7, 6, 5, 4, Z, Z, Z, Z | 1, 2 |
| | WRITE | 0 V V | 0, 1, 2, 3, X, X, X, X | 0, 1, 2, 3, X, X, X, X | 1, 3, 4 |
| | | 1 V V | 4, 5, 6, 7, X, X, X, X | 4, 5, 6, 7, X, X, X, X | 1, 3, 4 |
| 8 (fixed) | READ | 0 0 0 | 0, 1, 2, 3, 4, 5, 6, 7 | 0, 1, 2, 3, 4, 5, 6, 7 | 1 |
| | | 0 0 1 | 1, 2, 3, 0, 5, 6, 7, 4 | 1, 0, 3, 2, 5, 4, 7, 6 | 1 |
| | | 0 1 0 | 2, 3, 0, 1, 6, 7, 4, 5 | 2, 3, 0, 1, 6, 7, 4, 5 | 1 |
| | | 0 1 1 | 3, 0, 1, 2, 7, 4, 5, 6 | 3, 2, 1, 0, 7, 6, 5, 4 | 1 |
| | | 1 0 0 | 4, 5, 6, 7, 0, 1, 2, 3 | 4, 5, 6, 7, 0, 1, 2, 3 | 1 |
| | | 1 0 1 | 5, 6, 7, 4, 1, 2, 3, 0 | 5, 4, 7, 6, 1, 0, 3, 2 | 1 |
| | | 1 1 0 | 6, 7, 4, 5, 2, 3, 0, 1 | 6, 7, 4, 5, 2, 3, 0, 1 | 1 |
| | | 1 1 1 | 7, 4, 5, 6, 3, 0, 1, 2 | 7, 6, 5, 4, 3, 2, 1, 0 | 1 |
| | WRITE | V V V | 0, 1, 2, 3, 4, 5, 6, 7 | 0, 1, 2, 3, 4, 5, 6, 7 | 1, 3 |

Notes: 1. Internal READ and WRITE operations start at the same point in time for BC4 as they do for BL8.
2. Z = Data and strobe output drivers are in tri-state.
3. V = A valid logic level (0 or 1), but the respective input buffer ignores level-on input pins.
4. X = "Don't Care."

# 6 Operating Conditions and Interface Specification

## 6.1 Absolute Maximum Ratings

**Table 11 - Absolute Maximum Ratings**

| Parameter | Symbol | Rating | | Unit | Note |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| Voltage on $V_{DD}$ ball relative to $V_{SS}$ | $V_{DD}$ | –0.4 | +1.975 | V | 1) |
| Voltage on $V_{DDQ}$ ball relative to $V_{SS}$ | $V_{DDQ}$ | –0.4 | +1.975 | V | |
| Voltage on any ball relative to $V_{SS}$ | $V_{IN}$, $V_{OUT}$ | –0.4 | +1.975 | V | |
| Storage Temperature | $T_{STG}$ | –55 | +150 | °C | |

1) $V_{DD}$ and $V_{DDQ}$ must be within 300mV of each other at all times. $V_{REF}$ must not be greater than 0.6 x $V_{DDQ}$. When $V_{DD}$ and $V_{DDQ}$ are less than 500 mV, $V_{REF}$ may be equal or less than 300 mV.

# 6.2 Operating Conditions

**Table 12 - SDRAM Component Operating Temperature Range**

| Parameter | Symbol | Rating | | Unit | Note |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| Operating Temperature Range | $T_c$ | 0 | 85 | °C | 1)2)3)4) |
| | | 85 | 95 | °C | 1)2)3)4) |

1) MAX operating case temperature Tc is measured in the center of the package, as shown below.
2) A thermal solution must be designed to ensure that the device does not exceed the maximum TC during operation.
3) Device functionality is not guaranteed if the device exceeds maximum TC during operation.
4) If TC exceeds 85°C, the DRAM must be refreshed externally at 2x refresh, which is a 3.9μs interval refresh rate. The use of self refresh temperature (SRT) or automatic self refresh (ASR), must be enabled.

**Table 13 - DC Operating Conditions**

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | 1.283 | 1.35 | 1.45 | V | 1-7 |
| Supply Voltage for Output | $V_{DDQ}$ | 1.283 | 1.35 | 1.45 | V | 1-7 |
| Reference Voltage for DQ, DM inputs | $V_{REFDQ.DC}$ | 0.49 x $V_{DD}$ | 0.5 x $V_{DD}$ | 0.51 x $V_{DD}$ | V | 8)9) |
| Reference Voltage for ADD, CMD inputs | $V_{REFCA.DC}$ | 0.49 x $V_{DD}$ | 0.5 x $V_{DD}$ | 0.51 x $V_{DD}$ | V | 9)10) |
| External Calibration Resistor connected from ZQ ball to ground | $R_{ZQ}$ | 237.6 | 240.0 | 242.4 | Ω | 11) |

1) $V_{DD}$ and $V_{DDQ}$ must track one another. $V_{DDQ}$ must be ≤ $V_{DD}$. $V_{SS}$ = $V_{SSQ}$.
2) $V_{DD}$ and $V_{DDQ}$ may include AC noise of ±50mV (250 kHz to 20 MHz) in addition to the DC (0 Hz to 250 kHz) specifications. $V_{DD}$ and $V_{DDQ}$ must be at same level for valid AC timing parameters.
3) Maximum DC value may not be greater than 1.425V. The DC value is the linear average of $V_{DD}$/$V_{DDQ}$(t) over a very long period of time (for example, 1 second)
4) Under these supply voltages, the device operates to this DDR3L specification
5) If the maximum limit is exceeded, input levels shall be governed by DDR3specifications.
6) Under 1.5V operation, this DDR3L device operates in accordance with the DDR3 specifi-cations under the same speed timings as defined for this device.
7) Once initialized for DDR3L operation, DDR3 operation may only be used if the device is in reset while $V_{DD}$ and $V_{DDQ}$ are changed for DDR3 operation (see VDD Voltage Switch-ing .
8) $V_{REFCA(DC)}$ is expected to be approximately 0.5 × $V_{DD}$ and to track variations in the DC level. Externally generated peak noise (non-common mode) on $V_{REFCA}$ may not exceed ±1% × $V_{DD}$ around the $V_{REFCA(DC)}$ value. Peak-to-peak AC noise on $V_{REFCA}$ should not ex-ceed ±2% of $V_{REFCA(DC)}$.
9) DC values are determined to be less than 20 MHz in frequency. DRAM must meet specifi-cations if the DRAM induces additionalAC noise greater than 20 MHz in frequency
10) $V_{REFDQ(DC)}$ is expected to be approximately 0.5 × $V_{DD}$ and to track variations in the DC level. Externally generated peak noise (non-common mode) on $V_{REFDQ}$ maynot exceed ±1% × $V_{DD}$ around the $V_{REFDQ(DC)}$ value. Peak-to-peak AC noise on $V_{REFDQ}$ should not ex-ceed ±2% of $V_{REFDQ(DC)}$.
11) The external calibration resistor $R_{ZQ}$ can be time-shared among DRAMs in multi-rank DIMMs.

**Table 14 - Input and Output Leakage Currents**

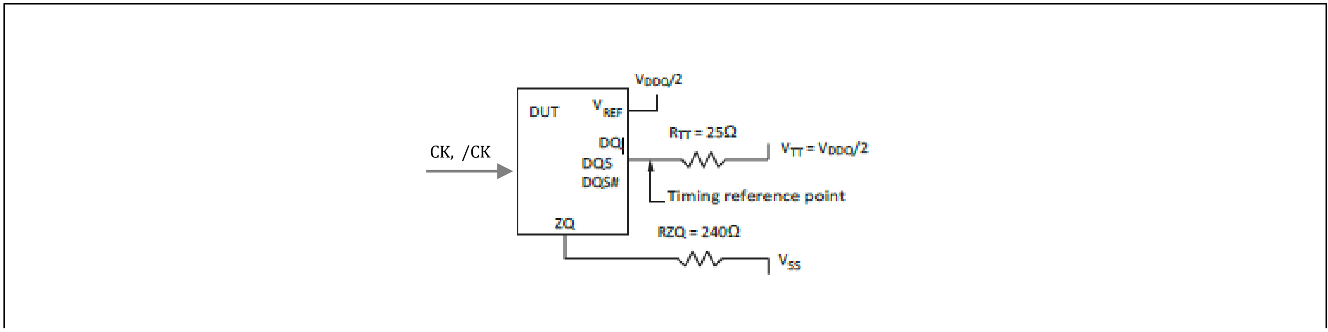
| Parameter | Symbol | Condition | Rating | | Unit | Note |
|---|---|---|---|---|---|---|
| | | | Min. | Max. | | |
| Input Leakage Current | $I_{IL}$ | Any input 0 V < $V_{IN}$ < $V_{DD}$ | –2 | +2 | μA | 1)2) |
| Output Leakage Current | $I_{OL}$ | 0V < $V_{OUT}$ < $V_{DDQ}$ | –5 | +5 | μA | 2)3) |

1) All other pins not under test = 0 V.
2) Values are shown per ball.
3) DQ's, DQS, /DQS and ODT are disabled.

## 6.3 Interface Test Conditions

**Figure 4** represents the effective reference load of 25 Ω used in defining the relevant timing parameters of the device as well as for output slew rate measurements. It is not intended as either a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

**Figure 3 - Reference Load for AC Timings and Output Slew Rates**




The Timing Reference Points are the idealized input and output nodes / terminals on the outside of the packaged SDRAM device as they would appear in a schematic or an IBIS model.

The output timing reference voltage level for single ended signals is the cross point with $V_{TT}$.

The output timing reference voltage level for differential signals is the cross point of the true (e.g. DQS) and the complement (e.g. /DQS) signal.

## 6.4 Voltage Levels

### 6.4.1 DC and AC Logic Input Levels

**Single-Ended Signals**

Table 15 shows the input levels for single-ended input signals.

**Table 15 - DC and AC Input Levels for Single-Ended Command, Address and Control Signals**

| Parameter | Symbol | DDR3L-1600,-1866 | | Unit | Note |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| DC input logic high | $V_{IH.CA.DC}$ | $V_{REF}$ + 0.100 | $V_{DD}$ | V | 1) |
| DC input logic low | $V_{IL.CA.DC}$ | $V_{SS}$ | $V_{REF}$ - 0.100 | V | 1) |
| AC input logic high | $V_{IH.CA.AC}$ | $V_{REF}$ + 0.175 | See 2) | V | 1) |
| AC input logic low | $V_{IL.CA.AC}$ | See 2) | $V_{REF}$ - 0.175 | V | 1) |

1) For input only pins except RESET: $V_{REF} = V_{REF.CA}$
2) See Chapter 6.9, Overshoot and Undershoot Specification.

**Table 16 - DC and AC Input Levels for Single-Ended DQ and DM Signals**

| Parameter | Symbol | DDR3L-1600,-1866 | | Unit | Note |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| DC input logic high | $V_{IH.DQ.DC}$ | $V_{REF}$ + 0.100 | $V_{DD}$ | V | 1) |
| DC input logic low | $V_{IL.DQ.DC}$ | $V_{SS}$ | $V_{REF}$ - 0.100 | V | 1) |
| AC input logic high | $V_{IH.DQ.AC}$ | $V_{REF}$ + 0.150 | See 2) | V | 1) 3) |
| AC input logic low | $V_{IL.DQ.AC}$ | See 2) | $V_{REF}$ - 0.150 | V | 1) 3) |

1) For DQ and DM: $V_{REF} = V_{REFDQ}$, for input only signals except RESET: $V_{REF} = V_{REFCA}$
2) See Chapter 6.9, Overshoot and Undershoot Specification.
3) Single ended swing requirement for DQS, /DQS is 350 mV (peak to peak). Differential swing requirement for DQS, /DQS is 700 mV (peak to peak).

**Differential Swing Requirement for Differential Signals**

Table 18 shows the input levels for differential input signals.

**Table 17 - Differential swing requirement for clock (CK - /CK) and strobe (DQS - /DQS)**

| Parameter | Symbol | DDR3L-1600,-1866 | | Unit | Note |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| Differential input high | $V_{IH.DIFF}$ | +0.18 | See 1) | V | 2) |
| Differential input low | $V_{IL.DIFF}$ | See 1) | –0.18 | V | 2) |
| Differential input high AC | $V_{IH.DIFF.AC}$ | 2 x ($V_{IH.AC}$ - $V_{REF}$) 3) | See 1) | V | 4) |
| Differential input low AC | $V_{IL.DIFF.AC}$ | See 1) | 2 x ($V_{REF}$ - $V_{IL.AC}$) 5) | V | 4) |

1) These values are not defined, however they single-ended signals CK, /CK, DQS, /DQS need to be within the respective limits ( $V_{IH.DC.MAX}$, $V_{IL.DC.MIN}$ ) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to Chapter 6.9 .
2) Used to define a differential signal slew-rate.
3) Clock: use $V_{IH.CA.AC}$ for $V_{IH.AC}$. Strobe: use $V_{IH.DQ.AC}$ for $V_{IH.AC}$.
4) For CK - /CK use $V_{IH}$/$V_{IL.AC}$ of ADD/CMD and $V_{REFCA}$; for DQS - /DQS use $V_{IH}$/$V_{IL.AC}$ of DQs and $V_{REFDQ}$; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.
5) Clock: use $V_{IL.CA.AC}$ for $V_{IL.AC}$. Strobe: use $V_{IL.DQ.AC}$ for $V_{IL.AC}$.

**Table 18 - Allowed Time Before Ringback (tDVAC) for CK - /CK and DQS - /DQS**

| Slew Rate [V/ns] | $t_{DVAC}$ [ps]@ \|$V_{IH/IL.DIFF.AC}$\| | | $t_{DVAC}$ [ps]@ \|$V_{IH/IL.DIFF.AC}$\| | | |
|---|---|---|---|---|---|
| | DDR3L-1600 | | DDR3L-1866 | | |
| | 320mv | 270mv | 270mv | 260mv | 250mv |
| > 4.0 | 189 | 201 | 163 | 176 | 168 |
| 4.0 | 189 | 201 | 163 | 176 | 168 |
| 3.0 | 162 | 179 | 140 | 154 | 147 |
| 2.0 | 109 | 134 | 95 | 111 | 105 |
| 1.8 | 91 | 119 | 80 | 97 | 91 |
| 1.6 | 69 | 100 | 62 | 78 | 74 |
| 1.4 | 40 | 76 | 37 | 55 | 52 |
| 1.2 | Note1 | 44 | 5 | 24 | 22 |
| 1.0 | Note1 | | | | |
| <1.0 | Note1 | | | | |

Note:1.Rising input signal shall become equal to or grater than $V_{IH.AC}$ level and failing input signal shall become equal to or less than $V_{IL.AC}$ level.

**Single-Ended Requirements for Differential Signals**

Each individual component of a differential signal (CK, DQS, /CK, /DQS,) has also to comply with certain requirements for single-ended signals.

CK and /CK have to approximately reach $V_{SEH.MIN}$ / $V_{SEL.MAX}$ (approximately equal to the ac-levels ($V_{IH.AC}$ / $V_{IL.AC}$) for ADD/CMD signals) in every half-cycle

DQS, /DQS have to reach $V_{SEH.MIN}$ / $V_{SEL.MAX}$ (approximately the ac-levels ( $V_{IH.AC}$ / $V_{IL.AC}$ ) for DQ signals) in every half-cycle preceeding and following a valid transition.

Note that the applicable ac-levels for ADD/CMD and DQs might be different per speed-bin etc. E.g. if $V_{IH150.AC}$ / $V_{IL150.AC}$

is used for ADD/CMD signals, then these ac-levels apply also for the single-ended signals CK and /CK.

Note that while ADD/CMD and DQ signal requirements are with respect to $V_{ref}$, the single-ended components of differential signals have a requirement with respect to $V_{DD}$/2; this is nominally the same. The transition of single-ended signals through the ac-levels is used to measure setup time.

For single-ended components of differential signals the requirement to reach $V_{SEL.MAX}$, $V_{SEH.MIN}$ has no bearing on timing, but adds a restriction on the common mode charateristics of these signals.

**Table 19 - Each Single-Ended Levels for CK, DQS, /DQS, /CK,**

| Parameter | Symbol | DDR3L-1600,-1866 | | Unit | Note |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| Single-ended highlevel for strobes | $V_{SEH}$ | (VDD/2) + 160 | $V_{DDQ}$ | mV | 1,2 |
| Single-ended high-level for CK, /CK | $V_{SEH}$ | (VDD/2) + 160 | $V_{DD}$ | mV | |
| Single-ended low-level for strobes | $V_{SEL}$ | $V_{SSQ}$ | (VDD/2) -0.175 | mV | |
| Single-ended low-level for CK, /CK | $V_{SEL}$ | $V_{SS}$ | (VDD/2) - 0.175 | mV | |

Note:
1. For CK, CK use VIH/VIL(AC) of address/command; for strobes (DQS, DQS) use VIH/VIL(AC) of DQs.
2. VIH(AC)/VIL(AC) for DQs is based on VREFDQ; VIH(AC)/VIL(AC) for address/command is based on VREFCA; if a reduced AC-high or AC-low level is used for a signal group, then the reduced level applies also here.

**Table 20 - Cross Point Voltage for Differential Input Signals (CK, DQS)**

| Symbol | Parameter | DDR3L-1600,-1866 | | Unit | Note |
|---|---|---|---|---|---|
| | | Min | Max | | |
| $V_{IX}$ | Differential Input Cross Point Voltage relative to VDD/2 for CK, /CK | $V_{REF(DC)}$ –150 | $V_{REF(DC)}$+150 | mV | 1)2)3) |
| $V_{IX}$ | Differential Input Cross Point Voltage relative to VDD/2 for DQS, DQS | $V_{REF(DC)}$–150 | $V_{REF(DC)}$+150 | mV | 1)2)3)1) |

1. Minimum DC limit is relative to single-ended signals; overshoot specifications are appli-cable
2. The typical value of $V_{IX(AC)}$ is expected to be about 0.5 × $V_{DD}$ of the transmitting device, and $V_{IX(AC)}$ is expected to track variations in $V_{DD}$. $V_{IX(AC)}$ indicates the voltage at which differential input signals must cross.
3. $V_{IX}$ must provide 25mV (single-ended) of the voltages separation.

## 6.4.2 DC and AC Output Measurements Levels

**Table 21 - DC and AC Output Levels for Single-Ended Signals**

| Parameter | Symbol | Value | Unit | Note |
|---|---|---|---|---|
| DC output high measurement level (for output impedance measurement) | $V_{OH.DC}$ | 0.8 x $V_{DDQ}$ | V | 1)2)3) |
| DC output mid measurement level (for output impedance measurement) | $V_{OM.DC}$ | 0.5 x $V_{DDQ}$ | V | 1)2)3) |
| DC output low measurement level (for output impedance measurement) | $V_{OL.DC}$ | 0.2 x $V_{DDQ}$ | V | 1)2)3) |
| AC output high measurement level (for output slew rate) | $V_{OH.AC}$ | $V_{TT}$ + 0.1 x $V_{DDQ}$ | V | 1)2)3)4) |
| AC output low measurement level (for output slew rate) | $V_{OL.AC}$ | $V_{TT}$ - 0.1 x $V_{DDQ}$ | V | 1)2)3)4) |

1) RZQ of 240Ω ±1% with RZQ/7 enabled (default 34Ω driver) and is applicable after prop-er ZQ calibration has been performed at a stable temperature and voltage (VDDQ= VDD; VSSQ= VSS).
2) VTT= VDDQ/2.
3) LV curve linearity. Do not use AC test load.
4) See Slew Rate Definitions for Single-Ended Output Signals for output slew-rate.

**Table 22 - AC Output Levels for Differential Signals**

| Parameter | Symbol | Value | | Unit | Note |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| AC differential output high measurement level (for output slew rate) | $V_{OH.DIFF.AC}$ | +0.2 x $V_{DDQ}$ | | V | 1) 2) |
| AC differential output low measurement level (for output slew rate) | $V_{OL.DIFF.AC}$ | –0.2 x $V_{DDQ}$ | | V | 1) 2) |
| Deviation of the output cross point voltage from the termination voltage | $V_{OX}$ | -100 | 100 | mV | 3) |

1) RZQ of 240Ω ±1% with RZQ/7 enabled (default 34Ω driver) and is applicable after prop-er ZQ calibration has been performed at a stable temperature and voltage ( $V_{DDQ}$= $V_{DD}$; $V_{SSQ}$= $V_{SS}$).
2) The test load configuration.
3) For a differential slew rate between the list values, the $V_{OX(AC)}$ value may be obtained by linear interpolation.

## 6.5 Output Slew Rates

**Table 23 - Output Slew Rates**

| Parameter | Symbol | DDR3L–1600,-1866 | | Unit | Note |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| Single-ended Output Slew Rate | SRQse | 1.75 | 6 | V / ns | 1)2)3)4) |
| Differential Output Slew Rate | SRQdiff | 3.5 | 12 | V / ns | |

1) RZQ of 240Ω ±1% with RZQ/7 enabled (default 34Ω driver) and is applicable after prop-er ZQ calibration has been performed at a stable temperature and voltage (VDDQ= VDD; VSSQ= VSS)..
2) VTT= VDDQ/2.
3) The test load configuration.
4) The 6 V/ns maximum is applicable for a single DQ signal when it is switching either from HIGH to LOW or LOW to HIGH while the remaining DQ signals in the same byte lane are either all static or all switching in the opposite direction. For all other DQ signal switch-ing combinations, the maximum limit of 6 V/ns is reduced to 5 V/ns.

UnilC

## 6.6 ODT DC Impedance and Mid-Level Characteristics

**Table 24** provides the ODT DC impedance and mid-level characteristics.

**Table 24 - ODT DC Impedance and Mid-Level Characteristics**

| Symbol | Description | $V_{OUT}$ Condition | Min. | Nom. | Max. | Unit | Note |
|---|---|---|---|---|---|---|---|
| $R_{TT120}$ | $R_{TT}$ effective = 120 Ω | $V_{IL.AC}$ and $V_{IH.AC}$ | 0.9 | 1.0 | 1.65 | $R_{ZQ}/2$ | 1)2)3)4) |
| $R_{TT60}$ | $R_{TT}$ effective = 60 Ω | | 0.9 | 1.0 | 1.65 | $R_{ZQ}/4$ | 1)2)3)4) |
| $R_{TT40}$ | $R_{TT}$ effective = 40 Ω | | 0.9 | 1.0 | 1.65 | $R_{ZQ}/6$ | 1)2)3)4) |
| $R_{TT30}$ | $R_{TT}$ effective = 30 Ω | | 0.9 | 1.0 | 1.65 | $R_{ZQ}/8$ | 1)2)3)4) |
| $R_{TT20}$ | $R_{TT}$ effective = 20 Ω | | 0.9 | 1.0 | 1.65 | $R_{ZQ}/12$ | 1)2)3)4) |
| $\Delta V_M$ | Deviation of $V_M$ with respect to $V_{DDQ}$ / 2 | floating | –5 | - | +5 | % | 1)2)3)4)5) |

1) With $R_{ZQ}$ = 240 Ω.
2) Measurement definition for $R_{TT}$ : Apply $V_{IH.AC}$ and $V_{IL.AC}$ to test ball separately, then measure current $I$ ($V_{IH.AC}$) and $I$ ($V_{IL.AC}$) respectively. $R_{TT} = [V_{IH.AC} - V_{IL.AC}] / [I(V_{IH.AC}) - I(V_{IL.AC})]$
3) The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see the **ODT DC Impedance Sensitivity on Temperature and Voltage Drifts**.
4) The tolerance limits are specified under the condition that $V_{DDQ} = V_{DD}$ and that $V_{SSQ} = V_{SS}$.
5) Measurement Definition for $\Delta V_M$: Measure voltage ($V_M$) at test ball (midpoint) with no load: $\Delta V_M = (2 \times V_M / V_{DDQ} - 1) \times 100\%$

## 6.7 ODT DC Impedance Sensitivity on Temperature and Voltage Drifts

If temperature and/or voltage change after calibration, the tolerance limits widen for $R_{TT}$ according to the following tables. The following definitions are used:

$\Delta T = T - T$ (at calibration)

$\Delta V = V_{DDQ} - V_{DDQ}$ (at calibration)

$V_{DD} = V_{DDQ}$

**Table 25 - ODT DC Impedance after proper IO Calibration and Voltage/Temperature Drift**

| Symbol | Value | | Unit | Note |
|---|---|---|---|---|
| | Min. | Max. | | |
| $R_{TT}$ | 0.9 - d$R_{TT}$dT x \|ΔT\| - d$R_{TT}$dV x \|ΔV\| | 1.6 + d$R_{TT}$dT x \|ΔT\| + d$R_{TT}$dV x \|ΔV\| | $R_{ZQ}$ / $TISF_{RTT}$ | 1) |

**Table 26 - OTD DC Impedance Sensitivity Parameters**

| Symbol | Value | | Unit | Note |
|---|---|---|---|---|
| | Min. | Max. | | |
| $dR_{TT}dT$ | 0 | 1.5 | %/°C | 1) |
| $dR_{TT}dV$ | 0 | 0.15 | %/mV | |

# 6.8 Interface Capacitance

Definition and values for interface capacitances are provided in the following table.

**Table 27 - Interface Capacitance Values**

| Parameter | Symbol | DDR3L–1600 | | DDR3L–1866 | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | | |
| Input/Output Capacitance (DQ,DM,DQS,/DQQS) | $C_{IO}$ | 1.4 | 2.2 | 1.4 | 2.1 | pF | 2 |
| Input Capacitance (CK and /CK) | $C_{CK}$ | 0.8 | 1.4 | 0.8 | 1.3 | pF | |
| Input Capacitance Delta (CK and /CK) | $C_{DCK}$ | 0 | 0.15 | 0 | 0.15 | pF | |
| Input/Output Capacitance delta (DQS and /DQS) | $C_{DDQS}$ | 0 | 0.15 | 0 | 0.15 | pF | 3 |
| Input Capacitance (CK and /CK) (All other input-only pins) | $C_I$ | 0.75 | 1.2 | 0.75 | 1.2 | pF | 5 |
| Input Capacitance delta (All control input-only pins) | $C_{DI_CTRL}$ | -0.4 | 0.2 | -0.4 | 0.2 | pF | 6 |
| Input Capacitance delta (All ADD and CMD input-only pins) | $C_{DI_ADD_CMD}$ | –0.4 | 0.4 | –0.4 | 0.4 | pF | 7 |
| Input/Output Capacitance delta (DQ,DM,DQS,/DQQS) | $C_{DIO}$ | -0.5 | 0.3 | -0.5 | 0.3 | pF | 4 |
| Input/output capacitance of ZQ pin | $C_{ZQ}$ | – | 3 | – | 3 | pF | |
| Reset pin capacitance | $CRE$ | – | 3.0 | – | 3.0 | pF | |

1. $V_{DD}$ = 1.35V (1.283–1.45V), $V_{DDQ} = V_{DD}$, $V_{REF} = V_{SS}$, $f$ = 100 MHz, $T_C$ = 25°C. $V_{OUT(DC)} = 0.5 \times V_{DDQ}$, $V_{OUT}$ = 0.1V (peak-to-peak).
2. DM input is grouped with I/O pins, reflecting the fact that they are matched in loading.
3. Includes .$C_{DDQS}$ is for DQS vs. DQS# separately.
4. $C_{DIO} = C_{IO(DQ)} - 0.5 \times (C_{IO(DQS)} + C_{IO(DQS\#)})$.
5. Excludes CK, CKB; CTRL = ODT, CSB, and CKE; CMD = RASB, CASB, and WEB; ADDR = A[*n*:0], BA[2:0].
6. $C_{DI_CTRL} = C_{I(CTRL)} - 0.5 \times (C_{CK(CK)} + C_{CK(CKB)})$.
7. $C_{DI_CMD_ADDR} = C_{I(CMD_ADDR)} - 0.5 \times (C_{CK(CK)} + C_{CK(CKB)})$.

## 6.9 Overshoot and Undershoot Specification

**Table 28 - AC Overshoot / Undershoot Specification for Address and Control Signals**

| Parameter | DDR3L-1600 | DDR3L-1866 | DDR3L-1866 | Unit | Note |
|---|---|---|---|---|---|
| Maximum peak amplitude allowed for overshoot area | 0.4 | 0.4 | 0.4 | V | 1) |
| Maximum peak amplitude allowed for undershoot area | 0.4 | 0.4 | 0.4 | V | 1) |
| Maximum overshoot area above $V_{DD}$ | 0.33 | 0.28 | 0.25 | V /ns | 1) |
| Maximum undershoot area below $V_{SS}$ | 0.33 | 0.28 | 0.25 | V / ns | 1) |

1) Applies for the following signals: A[15:0], BA[3:0], /CS, /RAS, /CAS, /WE, CKE and ODT

**Figure 4 - AC Overshoot / Undershoot Definitions for Address and Control Signals**

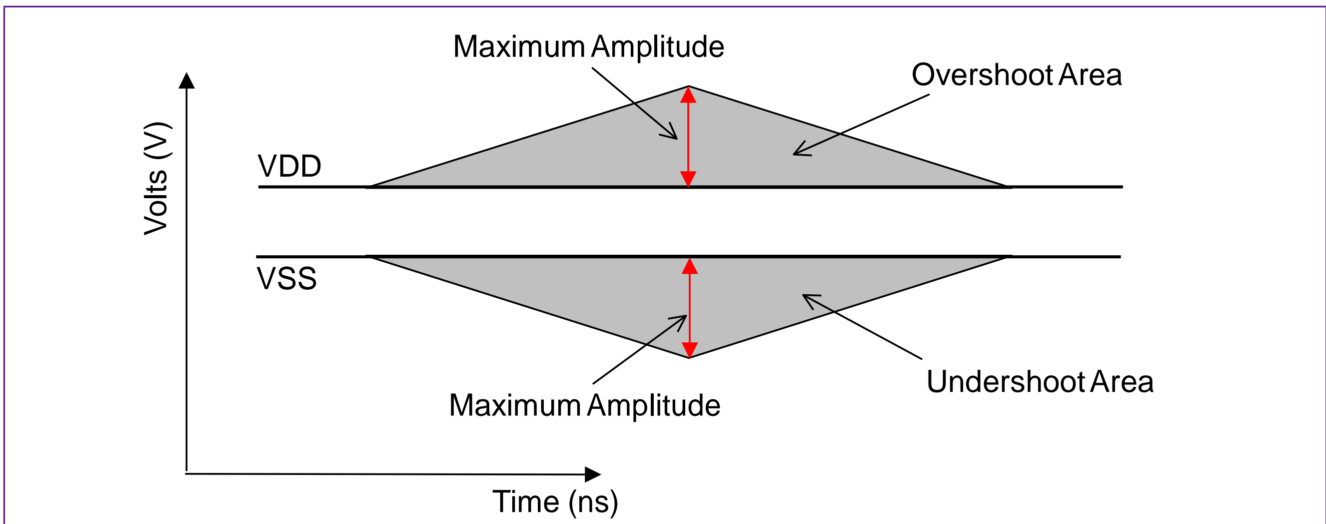
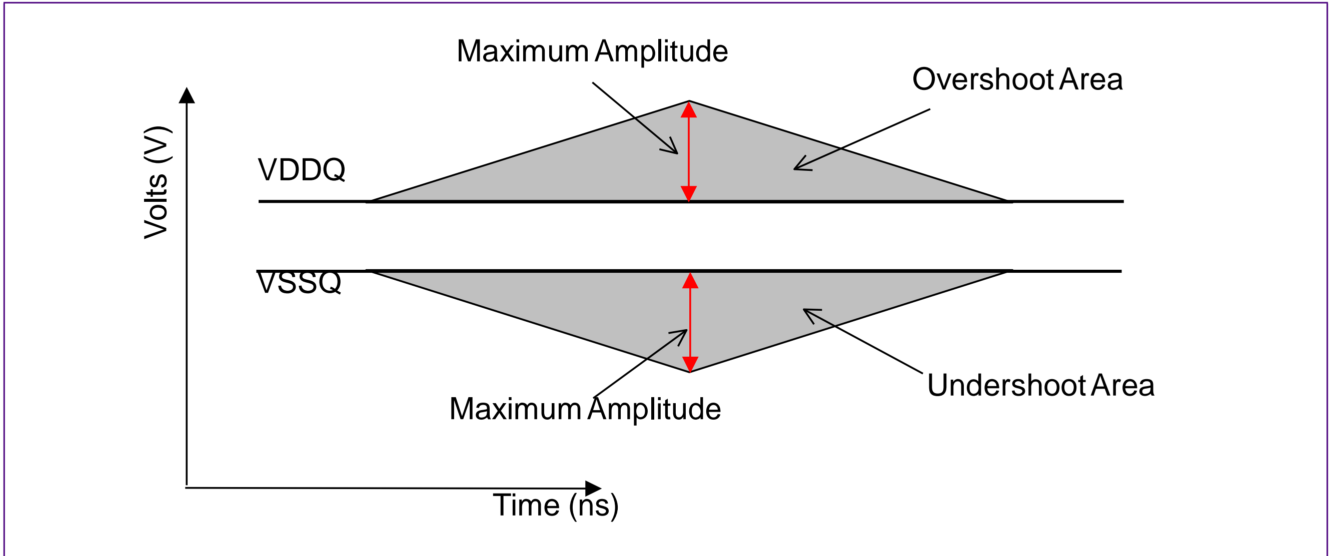



**Table 29 - AC Overshoot / Undershoot Specification for Clock, Data, Strobe and Mask Signals**

| Parameter | DDR3L-1600 | DDR3L-1866 | Unit | Note |
|---|---|---|---|---|
| Maximum peak amplitude allowed for overshoot area | 0.4 | 0.4 | V | 1) |
| Maximum peak amplitude allowed for undershoot area | 0.4 | 0.4 | V | 1) |
| Maximum overshoot area above $V_{DDQ}$ | 0.13 | 0.11 | V /ns | 1) |
| Maximum undershoot area below $V_{SSQ}$ | 0.13 | 0.11 | V / ns | 1) |

1) Applies for CK, /CK, DQ, DQS, /DQS & DM

**Figure 5 - AC Overshoot / Undershoot Definitions for Clock, Data, Strobe and Mask Signals**



# 7 Electrical Specifications

**Table 30 - IDD & IDDQ Specification**

| Symbol | 1.35V(x8) | | 1.35V(x16) | | 1.5V(x8) | | 1.5V(x16) | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | 1866 | 1600 | 1866 | 1600 | 1866 | 1600 | 1866 | 1600 | Mhz |
| IDD0 | 96 | 94 | 96 | 94 | 96 | 94 | 96 | 94 | mA |
| IDD1 | 125 | 122 | 125 | 122 | 125 | 122 | 125 | 122 | mA |
| IDD2P0 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | mA |
| IDD2P1 | 30 | 28 | 30 | 28 | 30 | 28 | 30 | 28 | mA |
| IDD2N | 50 | 48 | 50 | 48 | 50 | 48 | 50 | 48 | mA |
| IDD2NT | 58 | 56 | 58 | 56 | 58 | 56 | 58 | 56 | mA |
| IDD2Q | 50 | 48 | 50 | 48 | 50 | 48 | 50 | 48 | mA |
| IDD3P | 54 | 52 | 54 | 52 | 54 | 52 | 54 | 52 | mA |
| IDD3N | 62 | 60 | 62 | 60 | 62 | 60 | 62 | 60 | mA |
| IDD4R | 200 | 190 | 200 | 190 | 200 | 190 | 200 | 190 | mA |
| IDD4W | 360 | 350 | 360 | 350 | 360 | 350 | 360 | 350 | mA |
| IDD5B | 477 | 470 | 477 | 470 | 477 | 470 | 477 | 470 | mA |
| IDD6 | 24 | 24 | 24 | 24 | 24 | 24 | 24 | 24 | mA |
| IDD6ET | 32 | 32 | 32 | 32 | 32 | 32 | 32 | 32 | mA |
| IDD7 | 270 | 260 | 270 | 260 | 270 | 260 | 270 | 260 | mA |
| IDD8 | 20 | 20 | 20 | 20 | 20 | 20 | 20 | 20 | mA |

# 8 Speed Bin

**Table 31 - DDR3(L)-1600 Speed Bins**

| Speed Bin | | | | DDR3(L)-1600 | | Unit | Notes |
|---|---|---|---|---|---|---|---|
| CL-nRCD-nRP | | | | 11-11-11 | | | |
| Parameter | | | Symbol | Min | Max | | |
| Internal read command to first data | | | tAA | 13.75 (13.125) | 20 | ns | 8 |
| Active to read or write delay time | | | tRCD | 13.75 (13.125) | - | ns | 8 |
| Precharge command period | | | tRP | 13.75 (13.125) | - | ns | 8 |
| Active to active/auto-refresh command time | | | tRC | 48.75 (48.125) | - | ns | 8 |
| Active to precharge command period | | | tRAS | 35 | 9 * tREFI | ns | 7 |
| Average Clock Cycle Time | CL = 5 | CWL = 5 | tCK(avg) | 3.0 | 3.3 | ns | 1,2,3,5 |
| | | CWL = 6,7 | tCK(avg) | Reserved | Reserved | ns | 4 |
| | CL = 6 | CWL = 5 | tCK(avg) | 2.5 | 3.3 | ns | 1,2,3,5 |
| | | CWL = 6 | tCK(avg) | Reserved | Reserved | ns | 4 |
| | | CWL = 7 | tCK(avg) | Reserved | Reserved | ns | 4 |
| | CL = 7 | CWL = 5 | tCK(avg) | Reserved | Reserved | ns | 4 |
| | | CWL = 6 | tCK(avg) | 1.875 | < 2.5 | ns | 1,2,3,5 |
| | | CWL = 7 | tCK(avg) | Reserved | Reserved | ns | 4 |
| | CL = 8 | CWL = 5 | tCK(avg) | Reserved | Reserved | ns | 4 |
| | | CWL = 6 | tCK(avg) | 1.875 | < 2.5 | ns | 1,2,3,5 |
| | | CWL = 7 | tCK(avg) | Reserved | Reserved | ns | 4 |
| | CL = 9 | CWL = 5, 6 | tCK(avg) | Reserved | Reserved | ns | 4 |
| | | CWL = 7 | tCK(avg) | 1.5 | < 1.875 | ns | 1,2,3,5 |
| | CL = 10 | CWL = 5, 6 | tCK(avg) | Reserved | Reserved | ns | 4 |
| | | CWL = 7 | tCK(avg) | 1.5 | < 1.875 | ns | 1,2,3,5 |
| | | CWL = 8 | tCK(avg) | Reserved | Reserved | ns | 4 |
| | CL = 11 | CWL = 5, 6,7 | tCK(avg) | Reserved | Reserved | ns | 4 |
| | | CWL = 8 | tCK(avg) | 1.25 | < 1.5 | ns | 1,2,3 |
| Supported CL setting | | | | 5, 6, 7, 8, 9, 10,11 | | nCK | |
| Supported CWL setting | | | | 5, 6, 7, 8 | | nCK | |

**Table 32 - DDR3(L)-1866 Speed Bins**

| Speed Bin | | | | DDR3(L)-1866 | | Unit | Notes |
|---|---|---|---|---|---|---|---|
| CL-nRCD-nRP | | | | 13-13-13 | | | |
| Parameter | | | Symbol | Min | Max | | |
| Internal read command to first data | | | tAA | 13.91 (13.125) | 20 | ns | 9 |
| Active to read or write delay time | | | tRCD | 13.91 (13.125) | - | ns | 9 |
| Precharge command period | | | tRP | 13.91 (13.125) | - | ns | 9 |
| Active to active/auto-refresh command time | | | tRC | 47.91 (47.125) | - | ns | 9 |
| Active to precharge command period | | | tRAS | 34 | 9 * tREFI | ns | 7 |
| Average Clock Cycle Time | CL = 5 | CWL = 5 | tCK(avg) | 3.0 | 3.3 | ns | 1,2,3,6 |
| | | CWL = 6,7 | tCK(avg) | Reserved | Reserved | ns | 4 |
| | CL = 6 | CWL = 5 | tCK(avg) | 2.5 | 3.3 | ns | 1,2,3,6 |
| | | CWL = 6 | tCK(avg) | Reserved | Reserved | ns | 4 |
| | | CWL = 7 | tCK(avg) | Reserved | Reserved | ns | 4 |
| | CL = 7 | CWL = 5 | tCK(avg) | Reserved | Reserved | ns | 4 |
| | | CWL = 6 | tCK(avg) | 1.875 | 2.5 | ns | 1,2,3,6 |
| | | CWL = 7 | tCK(avg) | Reserved | Reserved | ns | 1,2,3,6 |
| | CL = 8 | CWL = 5 | tCK(avg) | Reserved | Reserved | ns | 4 |
| | | CWL = 6 | tCK(avg) | 1.875 | 2.5 | ns | 1,2,3,6 |
| | | CWL = 7 | tCK(avg) | Reserved | Reserved | ns | 4 |
| | CL = 9 | CWL = 5, 6 | tCK(avg) | Reserved | Reserved | ns | 4 |
| | | CWL = 7 | tCK(avg) | 1.5 | 1.875 | ns | 1,2,3,6 |
| | CL = 10 | CWL = 5, 6 | tCK(avg) | Reserved | Reserved | ns | 4 |
| | | CWL = 7 | tCK(avg) | 1.5 | 1.875 | ns | 1,2,3,6 |
| | | CWL = 8 | tCK(avg) | Reserved | Reserved | ns | 4 |
| | CL = 11 | CWL = 5, 6,7 | tCK(avg) | Reserved | Reserved | ns | 4 |
| | | CWL = 8 | tCK(avg) | 1.25 | 1.5 | ns | 1,2,3,6 |
| | CL = 12 | CWL = 5, 6,7,8 | tCK(avg) | Reserved | Reserved | ns | 4 |
| | | CWL = 9 | tCK(avg) | Reserved | Reserved | ns | 4 |
| | CL = 13 | CWL = 5, 6,7,8 | tCK(avg) | Reserved | Reserved | ns | 4 |
| | | CWL = 9 | tCK(avg) | 1.07 | 1.25 | ns | 1,2,3 |
| Supported CL setting | | | | 5, 6, 7, 8, 9, 10,11,13 | | nCK | |
| Supported CWL setting | | | | 5, 6, 7, 8, 9 | | nCK | |

Note :

1. The CL setting and CWL setting result in tCK(avg) Min and tCK(avg) Max requirements. When making a selection of tCK(avg), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. tCK(avg) Min limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK(avg) value (2.5, 1.875, 1.5, or 1.25 ns) when calculating CL [nCK] = tAA [ns] / tCK(avg) [ns], rounding up to the next "Supported CL".
3. tCK(avg) Max limits: Calculate tCK(avg) = tAA Max / CL Selected and round the resulting tCK(avg) down to the next valid speed bin (i.e. 3.3ns or 2.5ns or 1.875 ns or 1.25 ns). This result is tCK(avg) Max corresponding to CL selected.
4. "Reserved" settings are not allowed. User must program a different value.
5. Any DDR3-1600 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to production tests but verified by design/characterization.
6. Any DDR3-1866 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to production tests but verified by design/characterization.
7. tREFI depends on operating case temperature (Tc).
8. For devices supporting optional downshift to CL=7 and CL=9, tAA/tRCD/tRP min must be 13.125 ns or lower. SPD settings must be programmed to match. For example, DDR3-1600(CL11) devices supporting downshift to DDR3-1333(CL9) or DDR3-1066(CL7) should program 13.125 ns in SPD bytes for tAAmin (Byte16), tRCDmin (Byte 18), and tRPmin (Byte 20). DDR3-1866(CL13) devices supporting downshift to DDR3-1600(CL11) or DDR3-1333(CL9) or DDR3-1066(CL7) should program 13.125 ns in SPD bytes for tAAmin (Byte16), tRCDmin (Byte 18), and tRPmin (Byte 20). DDR3-1600 devices supporting down binning to DDR3- 1333 or DDR3-1066 should program 13.125ns in SPD byte for tAAmin (Byte 16), tRCDmin (Byte 18) and tRPmin (Byte 20). Once tRP (Byte 20) is programmed to 13.125ns, tRCmin (Byte 21,23) also should be programmed accod- ingly. For example, 49.125ns, (tRASmin + tRPmin = 36ns + 13.125ns) for DDR3-1333 and 48.125ns (tRASmin + tRPmin = 35ns + 13.125ns) for DDR3-1600.
9. For devices supporting optional down binning to CL=11, CL=9 and CL=7, tAA/tRCD/tRPmin must be 13.125ns. SPD setting must be programed to match. For example, DDR3-1866 devices supporting down binning to DDR3-1600 or DDR3-1333 or 1066 should program 13.125ns in SPD bytes for tAAmin(byte16), tRCDmin(Byte18) and tRP-min (byte20). Once tRP (Byte20) is programmed to 13.125ns, tRCmin (Byte21,23) also should be programmed accord- ingly. For example, 47.125ns (tRASmin + tRPmin = 34ns + 13.125ns)

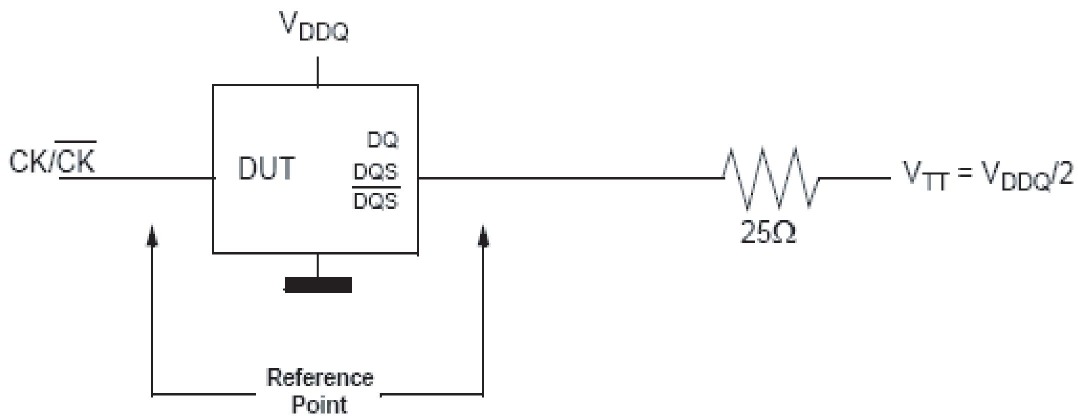
# 9 Electrical Characteristics & Timing

## 9.1 Reference Load for AC Timing and Output Slew Rate

**Figure 6** represents the effective reference load of 25 Ω used in defining the relevant timing parameters of the device as well as for output slew rate measurements.

It is not intended as either a precise representation any particular system environment or a depiction of the actual load pre-sented by a production tester. Sys-tem designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

**Figure 6 - Reference Load for AC Timings and Output Slew Rates**



## 9.2 Timing Parameters by Speed Grade

**Table 33 - AC Timing parameters**

| Parameter | Symbol | DDR3-1600 | | Unit | Note |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Average clock cycle time | $t_{CK}$(avg) | 1250 | 3333 | ps | |
| Minimum clock cycle time (DLL-off mode) | $t_{CK}$ (DLL-off) | 8 | - | ns | 6 |
| Average CK high level width | $t_{CH}$(avg) | 0.47 | 0.53 | $t_{CK}$(avg) | |
| Average CK low level width | $t_{CL}$(avg) | 0.47 | 0.53 | $t_{CK}$(avg) | |
| Active Bank A to Active Bank B command period | $t_{RRD}$ | 7.5 | - | ns | |
| | | 4 | - | nCK | |
| Four activate window | $t_{FAW}$ | 40 | - | ns | |
| Address and Control input hold time (VIH/VIL (DC100) levels) | $t_{IH}$(base) DC100 | 120 | - | ps | 16 |
| Address and Control input setup time (VIH/VIL (AC175) levels) | $t_{IS}$(base) AC175 | 45 | - | ps | 16 |
| Address and Control input setup time (VIH/VIL (AC150) levels) | $t_{IS}$(base) AC150 | 170 | - | ps | 16,24 |
| DQ and DM input hold time (VIH/VIL (DC100) levels) | $t_{DH}$(base) DC100 | 45 | - | ps | 17 |
| DQ and DM input setup time (VIH/VIL (AC175) levels) | $t_{DS}$(base) AC175 | - | - | ps | 17 |
| DQ and DM input setup time (VIH/VIL (AC150) levels) | $t_{DS}$(base) AC150 | 10 | - | ps | 17 |
| Control and Address Input pulse width for each input | $t_{IPW}$ | 560 | - | ps | 25 |
| DQ and DM Input pulse width for each input | $t_{DIPW}$ | 360 | - | ps | 25 |
| DQ high impedance time | $t_{HZ}$(DQ) | - | 225 | ps | 13,14 |
| DQ low impedance time | $t_{LZ}$(DQ) | -450 | 225 | ps | 13,14 |
| DQS, $\overline{DQS}$ high impedance time (RL + BL/2 reference) | $t_{HZ}$(DQS) | - | 225 | ps | 13,14 |
| DQS, $\overline{DQS}$ low impedance time (RL - 1 reference) | $t_{LZ}$(DQS) | -450 | 225 | ps | 13,14 |
| DQS, $\overline{DQS}$ to DQ Skew, per group, per access | $t_{DQSQ}$ | - | 100 | ps | 12,13 |
| $\overline{CAS}$ to $\overline{CAS}$ command delay | $t_{CCD}$ | 4 | - | nCK | |
| DQ output hold time from DQS, $\overline{DQS}$ | $t_{QH}$ | 0.38 | - | $t_{CK}$(avg) | 12,13 |
| DQS, $\overline{DQS}$ rising edge output access time from rising CK, CK | $t_{DQSCK}$ | -225 | 225 | ps | 12,13 |
| DQS latching rising transitions to associated clock edges | $t_{DQSS}$ | -0.27 | 0.27 | $t_{CK}$(avg) | |
| DQS falling edge hold time from rising CK | $t_{DSH}$ | 0.18 | - | $t_{CK}$(avg) | 29 |
| DQS falling edge setup time to rising CK | $t_{DSS}$ | 0.18 | - | $t_{CK}$(avg) | 29 |

| Parameter | Symbol | DDR3-1600 | | Unit | Note |
|---|---|---|---|---|---|
| | | Min | Max | | |
| DQS input high pulse width | $t_{DQSH}$ | 0.45 | 0.55 | $t_{CK}$(avg) | 27,28 |
| DQS input low pulse width | $t_{DQSL}$ | 0.45 | 0.55 | $t_{CK}$(avg) | 26,28 |
| DQS output high time | $t_{QSH}$ | 0.40 | - | $t_{CK}$(avg) | 12,13 |
| DQS output low time | $t_{QSL}$ | 0.40 | - | $t_{CK}$(avg) | 12,13 |
| Mode register set command cycle time | $t_{MRD}$ | 4 | - | nCK | |
| Mode register set command update delay | $t_{MOD}$ | 15 | - | ns | |
| | | 12 | - | nCK | |
| Read preamble time | $t_{RPRE}$ | 0.9 | - | $t_{CK}$(avg) | 13,19 |
| Read postamble time | $t_{RPST}$ | 0.3 | - | $t_{CK}$(avg) | 11,13 |
| Write preamble time | $t_{WPRE}$ | 0.9 | - | $t_{CK}$(avg) | 1 |
| Write postamble time | $t_{WPST}$ | 0.3 | - | $t_{CK}$(avg) | 1 |
| Write recovery time | $t_{WR}$ | 15 | - | ns | |
| Auto precharge write recovery + Precharge time | $t_{DAL}$(min) | WR + roundup [tRP / tCK(avg)] | | nCK | |
| Multi-purpose register recovery time | $t_{MPRR}$ | 1 | - | nCK | 22 |
| Internal write to read command delay | $t_{WTR}$ | 7.5 | - | ns | 18 |
| | | 4 | - | nCK | 18 |
| Internal read to precharge command delay | $t_{RTP}$ | 7.5 | - | ns | |
| | | 4 | - | nCK | |
| Minimum CKE low width for Self-refresh entry to exit timing | $t_{CKESR}$ | $t_{CKE}$(min) +1nCK | - | | |
| Valid clock requirement after Self- refresh entry or Power-down entry | $t_{CKSRE}$ | 10 | - | ns | |
| | | 5 | - | nCK | |
| Valid clock requirement before Self- refresh exit or Power-down exit | $t_{CKSRX}$ | 10 | - | ns | |
| | | 5 | - | nCK | |
| Exit Self-refresh to commands not requiring a locked DLL | $t_{XS}$ | $t_{RFC}$(min) +10 | - | ns | |
| | | 5 | - | nCK | |
| Exit Self-refresh to commands requiring a locked DLL | $t_{XSDLL}$ | $t_{DLLK}$ (min) | - | nCK | |
| Auto-refresh to Active/Auto-refresh command time | $t_{RFC}$ | 350 | - | ns | |
| Average Periodic Refresh Interval 0°C $\le$ Tc $\le$ +85°C | $t_{REFI}$ | - | 7.8 | μs | |
| Average Periodic Refresh Interval +85°C < Tc $\le$ +95°C | $t_{REFI}$ | - | 3.9 | μs | |
| CKE minimum high and low pulse width | $t_{CKE}$ | 5 | - | ns | |
| | | 3 | - | nCK | |
| Exit reset from CKE high to a valid command | $t_{XPR}$ | $t_{RFC}$(min) +10 | - | ns | |
| | | 5 | - | nCK | |
| DLL locking time | $t_{DLLK}$ | 512 | - | nCK | |

| Parameter | Symbol | DDR3-1600 | | Unit | Note |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Power-down entry to exit time | $t_{PD}$ | $t_{CKE}$(min) | 9*$t_{REFI}$ | | 15 |
| Exit precharge power-down with DLL frozen to commands requiring a locked DLL | $t_{XPDLL}$ | 24 | - | ns | 2 |
| | | 10 | - | nCK | 2 |
| Exit power-down with DLL on to any valid command; Exit precharge power-down with DLL frozen to commands not requiring a locked DLL | $t_{XP}$ | 6 | - | ns | |
| | | 3 | - | nCK | |
| Command pass disable delay | $t_{CPDED}$ | 1 | - | nCK | |
| Timing of ACT command to Power-down entry | $t_{ACTPDEN}$ | 1 | - | nCK | 20 |
| Timing of PRE command to Power-down entry | $t_{PRPDEN}$ | 1 | - | nCK | 20 |
| Timing of RD/RDA command to Power-down entry | $t_{RDPDEN}$ | RL+4+1 | - | nCK | |
| Timing of WR command to Power-down entry (BL8OTF, BL8MRS, BL4OTF) | $t_{WRPDEN}$ (min) | WL + 4 + [tWR/tCK(avg)] | | nCK | 9 |
| Timing of WR command to Power-down entry (BC4MRS) | $t_{WRPDEN}$ (min) | WL + 2 + [tWR/tCK(avg)] | | nCK | 9 |
| Timing of WRA command to Power-down entry (BL8OTF, BL8MRS, BL4OTF) | $t_{WRAPDEN}$ | WL+4 +WR+1 | - | nCK | 10 |
| Timing of WRA command to Power-down entry (BC4MRS) | $t_{WRAPDEN}$ | WL+2 +WR+1 | - | nCK | 10 |
| Timing of REF command to Power-down entry | $t_{REFPDEN}$ | 1 | - | nCK | 20,21 |
| Timing of MRS command to Power-down entry | $t_{MRSPDEN}$ | $t_{MOD}$ (min) | - | | |
| RTT turn-on | $t_{AON}$ | -250 | 250 | ps | 7 |
| Asynchronous RTT turn-on delay (Power-down with DLL frozen) | $t_{AONPD}$ | 2 | 8.5 | ns | |
| RTT_Nom and RTT_WR turn-off time from ODTLoff reference | $t_{AOF}$ | 0.3 | 0.7 | $t_{CK}$(avg) | 8 |
| Asynchronous RTT turn-off delay (Power-down with DLL frozen) | $t_{AOFPD}$ | 2 | 8.5 | ns | |
| ODT high time without write command or with write command and BC4 | ODTH4 | 4 | - | nCK | |
| ODT high time with Write command and BL8 | ODTH8 | 6 | - | nCK | |
| RTT dynamic change skew | $t_{ADC}$ | 0.3 | 0.7 | $t_{CK}$(avg) | |
| Power-up and reset calibration time | $t_{ZQinit}$ | 512 | - | nCK | |
| Normal operation full calibration time | $t_{ZQoper}$ | 256 | - | nCK | |
| Normal operation short calibration time | $t_{ZQCS}$ | 64 | - | nCK | 23 |
| First DQS pulse rising edge after write leveling mode is programmed | $t_{WLMRD}$ | 40 | - | nCK | 3 |

| Parameter | Symbol | DDR3-1600 | | Unit | Note |
|---|---|---|---|---|---|
| | | Min | Max | | |
| DQS, $\overline{\text{DQS}}$ delay after write leveling mode is programmed | $t_{WLDQSEN}$ | 25 | - | nCK | 3 |
| Write leveling setup time from rising CK, CK crossing to rising DQS, DQS crossing | $t_{WLS}$ | 165 | - | ps | |
| Write leveling hold time from rising DQS, DQS crossing to rising CK, CK crossing | $t_{WLH}$ | 165 | - | ps | |
| Write leveling output delay | $t_{WLO}$ | 0 | 7.5 | ns | |
| Write leveling output error | $t_{WLOE}$ | 0 | 2 | ns | |
| Absolute clock period | $t_{CK}$(abs) | tCK(avg)min + tJIT(per)min | tCK(avg)max + tJIT(per)max | ps | |
| Absolute clock high pulse width | $t_{CH}$(abs) | 0.43 | - | $t_{CK}$(avg) | 30 |
| Absolute clock low pulse width | $t_{CL}$(abs) | 0.43 | - | $t_{CK}$(avg) | 31 |
| Clock period jitter | $t_{JIT}$(per) | -70 | 70 | ps | |
| Clock period jitter during DLL locking period | $t_{JIT}$(per,lck) | -60 | 60 | ps | |
| Cycle to cycle period jitter | $t_{JIT}$(cc) | - | 140 | ps | |
| Cycle to cycle period jitter during DLL locking period | $t_{JIT}$(cc,lck) | - | 120 | ps | |
| Cumulative error across 2 cycles | $t_{ERR}$(2per) | -103 | 103 | ps | |
| Cumulative error across 3 cycles | $t_{ERR}$(3per) | -122 | 122 | ps | |
| Cumulative error across 4 cycles | $t_{ERR}$(4per) | -136 | 136 | ps | |
| Cumulative error across 5 cycles | $t_{ERR}$(5per) | -147 | 147 | ps | |
| Cumulative error across 6 cycles | $t_{ERR}$(6per) | -155 | 155 | ps | |
| Cumulative error across 7 cycles | $t_{ERR}$(7per) | -163 | 163 | ps | |
| Cumulative error across 8 cycles | $t_{ERR}$(8per) | -169 | 169 | ps | |
| Cumulative error across 9 cycles | $t_{ERR}$(9per) | -175 | 175 | ps | |
| Cumulative error across 10 cycles | $t_{ERR}$(10per) | -180 | 180 | ps | |
| Cumulative error across 11 cycles | $t_{ERR}$(11per) | -184 | 184 | ps | |
| Cumulative error across 12 cycles | $t_{ERR}$(12per) | -188 | 188 | ps | |
| Cumulative error across n = 13,14,...49,50 cycles | $t_{ERR}$(nper) | $t_{ERR}$(nper)min = (1 + 0.68ln(n))*$t_{JIT}$(per)min<br>$t_{ERR}$(nper)max = (1 + 0.68ln(n))*$t_{JIT}$(per)max | | ps | 32 |

| Parameter | Symbol | DDR3-1866 | | Unit | Note |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Average clock cycle time | $t_{CK}$(avg) | Please refer Speed Bins | | ps | |
| Minimum clock cycle time (DLL-off mode) | $t_{CK}$ (DLL-off) | 8 | - | ns | 6 |
| Average CK high level width | $t_{CH}$(avg) | 0.47 | 0.53 | $t_{CK}$(avg) | |
| Average CK low level width | $t_{CL}$(avg) | 0.47 | 0.53 | $t_{CK}$(avg) | |
| Active Bank A to Active Bank B command period | $t_{RRD}$ | 6 | - | ns | |
| | | 4 | - | nCK | |
| Four activate window | $t_{FAW}$ | 35 | - | ns | |
| Address and Control input hold time (VIH/VIL (DC100) levels) | $t_{IH}$(base) DC100 | 100 | - | ps | 16 |
| Address and Control input setup time (VIH/VIL (AC125) levels) | $t_{IS}$(base) AC125 | 150 | - | ps | 16 |
| Address and Control input setup time (VIH/VIL (AC135) levels) | $t_{IS}$(base) AC135 | 65 | - | ps | 16 |
| DQ and DM input hold time (VIH/VIL (DC100) levels) | $t_{DH}$(base) DC100 | 70 | - | ps | 17 |
| DQ and DM input setup time (VIH/VIL (AC135) levels) | $t_{DS}$(base) AC135 | 68 | - | ps | 17 |
| Control and Address Input pulse width for each input | $t_{IPW}$ | 535 | - | ps | 25 |
| DQ and DM Input pulse width for each input | $t_{DIPW}$ | 320 | - | ps | 25 |
| DQ high impedance time | $t_{HZ}$(DQ) | - | 195 | ps | 13,14 |
| DQ low impedance time | $t_{LZ}$(DQ) | -390 | 195 | ps | 13,14 |
| DQS, $\overline{DQS}$ high impedance time (RL + BL/2 reference) | $t_{HZ}$(DQS) | - | 195 | ps | 13,14 |
| DQS, $\overline{DQS}$ low impedance time (RL - 1 reference) | $t_{LZ}$(DQS) | -390 | 195 | ps | 13,14 |
| DQS, $\overline{DQS}$ to DQ Skew, per group, per access | $t_{DQSQ}$ | - | 85 | ps | 12,13 |
| $\overline{CAS}$ to $\overline{CAS}$ command delay | $t_{CCD}$ | 4 | - | nCK | |
| DQ output hold time from DQS, $\overline{DQS}$ | $t_{QH}$ | 0.38 | - | $t_{CK}$(avg) | 12,13 |
| DQS, $\overline{DQS}$ rising edge output access time from rising CK, $\overline{CK}$ | $t_{DQSCK}$ | -195 | 195 | ps | 12,13 |
| DQS latching rising transitions to associated clock edges | $t_{DQSS}$ | -0.27 | 0.27 | $t_{CK}$(avg) | |
| DQS falling edge hold time from rising CK | $t_{DSH}$ | 0.18 | - | $t_{CK}$(avg) | 29 |
| DQS falling edge setup time to rising CK | $t_{DSS}$ | 0.18 | - | $t_{CK}$(avg) | 29 |
| DQS input high pulse width | $t_{DQSH}$ | 0.45 | 0.55 | $t_{CK}$(avg) | 27,28 |

| Parameter | Symbol | DDR3-1866 | | Unit | Note |
|---|---|---|---|---|---|
| | | Min | Max | | |
| DQS input low pulse width | $t_{DQSL}$ | 0.45 | 0.55 | $t_{CK}$(avg) | 26,28 |
| DQS output high time | $t_{QSH}$ | 0.40 | - | $t_{CK}$(avg) | 12,13 |
| DQS output low time | $t_{QSL}$ | 0.40 | - | $t_{CK}$(avg) | 12,13 |
| Mode register set command cycle time | $t_{MRD}$ | 4 | - | nCK | |
| Mode register set command update delay | $t_{MOD}$ | 15 | - | ns | |
| | | 12 | - | nCK | |
| Read preamble time | $t_{RPRE}$ | 0.9 | - | $t_{CK}$(avg) | 13,19 |
| Read postamble time | $t_{RPST}$ | 0.3 | - | $t_{CK}$(avg) | 11,13 |
| Write preamble time | $t_{WPRE}$ | 0.9 | - | $t_{CK}$(avg) | 1 |
| Write postamble time | $t_{WPST}$ | 0.3 | - | $t_{CK}$(avg) | 1 |
| Write recovery time | $t_{WR}$ | 15 | - | ns | |
| Auto precharge write recovery + Precharge time | $t_{DAL}$(min) | WR + roundup [tRP / tCK(avg)] | | nCK | |
| Multi-purpose register recovery time | $t_{MPRR}$ | 1 | - | nCK | 22 |
| Internal write to read command delay | $t_{WTR}$ | 7.5 | - | ns | 18 |
| | | 4 | - | nCK | 18 |
| Internal read to precharge command delay | $t_{RTP}$ | 7.5 | - | ns | |
| | | 4 | - | nCK | |
| Minimum CKE low width for Self-refresh entry to exit timing | $t_{CKESR}$ | $t_{CKE}$(min) +1nCK | - | | |
| Valid clock requirement after Self- refresh entry or Power-down entry | $t_{CKSRE}$ | 10 | - | ns | |
| | | 5 | - | nCK | |
| Valid clock requirement before Self- refresh exit or Power-down exit | $t_{CKSRX}$ | 10 | - | ns | |
| | | 5 | - | nCK | |
| Exit Self-refresh to commands not requiring a locked DLL | $t_{XS}$ | $t_{RFC}$(min) +10 | - | ns | |
| | | 5 | - | nCK | |
| Exit Self-refresh to commands requiring a locked DLL | $t_{XSDLL}$ | $t_{DLLK}$ (min) | - | nCK | |
| Auto-refresh to Active/Auto-refresh command time | $t_{RFC}$ | 350 | - | ns | |
| Average Periodic Refresh Interval 0°C $\le$ Tc $\le$ +85°C | $t_{REFI}$ | - | 7.8 | µs | |
| Average Periodic Refresh Interval +85°C < Tc $\le$ +95°C | $t_{REFI}$ | - | 3.9 | µs | |
| CKE minimum high and low pulse width | $t_{CKE}$ | 5 | - | ns | |
| | | 3 | - | nCK | |
| Exit reset from CKE high to a valid command | $t_{XPR}$ | $t_{RFC}$(min) +10 | - | ns | |
| | | 5 | - | nCK | |

| Parameter | Symbol | DDR3-1866 | | Unit | Note |
|---|---|---|---|---|---|
| | | Min | Max | | |
| DLL locking time | $t_{DLLK}$ | 512 | - | nCK | |
| Power-down entry to exit time | $t_{PD}$ | $t_{CKE}$(min) | 9*$t_{REFI}$ | | 15 |
| Exit precharge power-down with DLL frozen to commands requiring a locked DLL | $t_{XPDLL}$ | 24 | - | ns | 2 |
| | | 10 | - | nCK | 2 |
| Exit power-down with DLL on to any valid command; Exit precharge power-down with DLL frozen to commands not requiring a locked DLL | $t_{XP}$ | 6 | - | ns | |
| | | 3 | - | nCK | |
| Command pass disable delay | $t_{CPDED}$ | 2 | - | nCK | |
| Timing of ACT command to Power-down entry | $t_{ACTPDEN}$ | 1 | - | nCK | 20 |
| Timing of PRE command to Power-down entry | $t_{PRPDEN}$ | 1 | - | nCK | 20 |
| Timing of RD/RDA command to Power-down entry | $t_{RDPDEN}$ | RL+4+1 | - | nCK | |
| Timing of WR command to Power-down entry (BL8OTF, BL8MRS, BL4OTF) | $t_{WRPDEN}$ (min) | WL + 4 + [tWR/tCK(avg)] | | nCK | 9 |
| Timing of WR command to Power-down entry (BC4MRS) | $t_{WRPDEN}$ (min) | WL + 2 + [tWR/tCK(avg)] | | nCK | 9 |
| Timing of WRA command to Power-down entry (BL8OTF, BL8MRS, BL4OTF) | $t_{WRAPDEN}$ | WL+4 +WR+1 | - | nCK | 10 |
| Timing of WRA command to Power-down entry (BC4MRS) | $t_{WRAPDEN}$ | WL+2 +WR+1 | - | nCK | 10 |
| Timing of REF command to Power-down entry | $t_{REFPDEN}$ | 1 | - | nCK | 20,21 |
| Timing of MRS command to Power-down entry | $t_{MRSPDEN}$ | $t_{MOD}$ (min) | - | | |
| RTT turn-on | $t_{AON}$ | -195 | 195 | ps | 7 |
| Asynchronous RTT turn-on delay (Power-down with DLL frozen) | $t_{AONPD}$ | 2 | 8.5 | ns | |
| RTT_Nom and RTT_WR turn-off time from ODTLoff reference | $t_{AOF}$ | 0.3 | 0.7 | $t_{CK}$(avg) | 8 |
| Asynchronous RTT turn-off delay (Power-down with DLL frozen) | $t_{AOFPD}$ | 2 | 8.5 | ns | |
| ODT high time without write command or with write command and BC4 | ODTH4 | 4 | - | nCK | |
| ODT high time with Write command and BL8 | ODTH8 | 6 | - | nCK | |
| RTT dynamic change skew | $t_{ADC}$ | 0.3 | 0.7 | $t_{CK}$(avg) | |
| Power-up and reset calibration time | $t_{ZQinit}$ | 512 | - | nCK | |
| Normal operation full calibration time | $t_{ZQoper}$ | 256 | - | nCK | |
| Normal operation short calibration time | $t_{ZQCS}$ | 64 | - | nCK | 23 |

| Parameter | Symbol | DDR3-1866 | | Unit | Note |
|---|---|---|---|---|---|
| | | Min | Max | | |
| First DQS pulse rising edge after write leveling mode is programmed | $t_{WLMRD}$ | 40 | - | nCK | 3 |
| DQS, $\overline{DQS}$ delay after write leveling mode is programmed | $t_{WLDQSEN}$ | 25 | - | nCK | 3 |
| Write leveling setup time from rising CK, CK crossing to rising DQS, DQS crossing | $t_{WLS}$ | 140 | - | ps | |
| Write leveling hold time from rising DQS, DQS crossing to rising CK, CK crossing | $t_{WLH}$ | 140 | - | ps | |
| Write leveling output delay | $t_{WLO}$ | 0 | 7.5 | ns | |
| Write leveling output error | $t_{WLOE}$ | 0 | 2 | ns | |
| Absolute clock period | $t_{CK}$(abs) | tCK(avg)min + tJIT(per)min | tCK(avg)max + tJIT(per)max | ps | |
| Absolute clock high pulse width | $t_{CH}$(abs) | 0.43 | - | $t_{CK}$(avg) | 30 |
| Absolute clock low pulse width | $t_{CL}$(abs) | 0.43 | - | $t_{CK}$(avg) | 31 |
| Clock period jitter | $t_{JIT}$(per) | -60 | 60 | ps | |
| Clock period jitter during DLL locking period | $t_{JIT}$(per,lck) | -50 | 50 | ps | |
| Cycle to cycle period jitter | $t_{JIT}$(cc) | - | 120 | ps | |
| Cycle to cycle period jitter during DLL locking period | $t_{JIT}$(cc,lck) | - | 100 | ps | |
| Cumulative error across 2 cycles | $t_{ERR}$(2per) | -88 | 88 | ps | |
| Cumulative error across 3 cycles | $t_{ERR}$(3per) | -105 | 105 | ps | |
| Cumulative error across 4 cycles | $t_{ERR}$(4per) | -117 | 117 | ps | |
| Cumulative error across 5 cycles | $t_{ERR}$(5per) | -126 | 126 | ps | |
| Cumulative error across 6 cycles | $t_{ERR}$(6per) | -133 | 133 | ps | |
| Cumulative error across 7 cycles | $t_{ERR}$(7per) | -139 | 139 | ps | |
| Cumulative error across 8 cycles | $t_{ERR}$(8per) | -145 | 145 | ps | |
| Cumulative error across 9 cycles | $t_{ERR}$(9per) | -150 | 150 | ps | |
| Cumulative error across 10 cycles | $t_{ERR}$(10per) | -154 | 154 | ps | |
| Cumulative error across 11 cycles | $t_{ERR}$(11per) | -158 | 158 | ps | |
| Cumulative error across 12 cycles | $t_{ERR}$(12per) | -161 | 161 | ps | |
| Cumulative error across n = 13,14,...49,50 cycles | $t_{ERR}$(nper) | $t_{ERR}$(nper)min = (1 + 0.68ln(n))*$t_{JIT}$(per)min $t_{ERR}$(nper)max = (1 + 0.68ln(n))*$t_{JIT}$(per)max | | ps | 32 |

Note:

1. Actual value dependant upon measurement level definitions which are TBD.
2. Commands requiring a locked DLL are: READ (and READA) and synchronous ODT commands.
3. The max values are system dependent.
4. WR as programmed in mode register.
5. Value must be rounded-up to next higher integer value.
6. There is no maximum cycle time limit besides the need to satisfy the refresh interval, tREFI.
7. ODT turn on time (min.) is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time (max.) is when the ODT resistance is fully on. Both are measured from ODTLon.
8. ODT turn-off time (min.) is when the device starts to turn-off ODT resistance. ODT turn-off time (max.) is when the bus is in high impedance. Both are measured from ODTLoff.
9. tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR / tCK to the next integer.
10. WR in clock cycles as programmed in MR0.
11. The maximum read postamble is bound by tDQSCK(min) plus tQSH(min) on the left side and tHZ(DQS)max on the right side.
12. Output timing deratings are relative to the SDRAM input clock. When the device is operated with input clock jitter, this parameter needs to be derated by TBD.
13. Value is only valid for RON34.
14. Single ended signal parameter. Refer to the section of tLZ(DQS), tLZ(DQ), tHZ(DQS), tHZ(DQ) Notes for definition and measurement method.
15. tREFI depends on operating case temperature (Tc).
16. tIS(base) and tIH(base) values are for 1V/ns command/addresss single-ended slew rate and 2V/ns CK, CK differential slew rate, Note for DQ and DM signals, VREF(DC) = VREFDQ(DC). For input only pins except RESET, VREF(DC) = VREFCA(DC). See Address / Command Setup, Hold and Derating section.
17. tDS(base) and tDH(base) values are for 1V/ns DQ single-ended slew rate and 2V/ns DQS, DQS differential slew rate. Note for DQ and DM signals,VREF(DC)= VREFDQ(DC). For input only pins except RESET, VREF(DC) = VREFCA(DC). See Data Setup, Hold and and Slew Rate Derating section.
18. Start of internal write transaction is defined as follows ;

    For BL8 (fixed by MRS and on-the-fly) : Rising clock edge 4 clock cycles after WL.

    For BC4 (on-the-fly) : Rising clock edge 4 clock cycles after WL.

    For BC4 (fixed by MRS) : Rising clock edge 2 clock cycles after WL.
19. The maximum read preamble is bound by tLZDQS(min) on the left side and tDQSCK(max) on the right side.
20. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operation.
21. Although CKE is allowed to be registered LOW after a REFRESH command once tREFPDEN(min) is satisfied, there are cases where additional time such as tXPDLL(min) is also required.
22. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
23. One ZQCS command can effectively correct a minimum of 0.5 % (ZQCorrection) of RON and RTT impedance error within 64 nCK for all speed bins assuming the maximum sensitivities specified in the “Output Driver Voltage and Temperature Sensitivity” and “ODT Voltage and Temperature Sensitivity” tables. The appropriate interval between ZQCS commands can be determined from these tables and other application specific parameters.

    One method for calculating the interval between ZQCS commands, given the temperature (Tdriftrate) and voltage (Vdriftrate) drift rates that the SDRAM is subject to in the application, is illustrated. The interval could be defined by the following formula:

    $$\frac{ZQCorrection}{(TSens \times Tdriftrate) + (VSens \times Vdriftrate)}$$

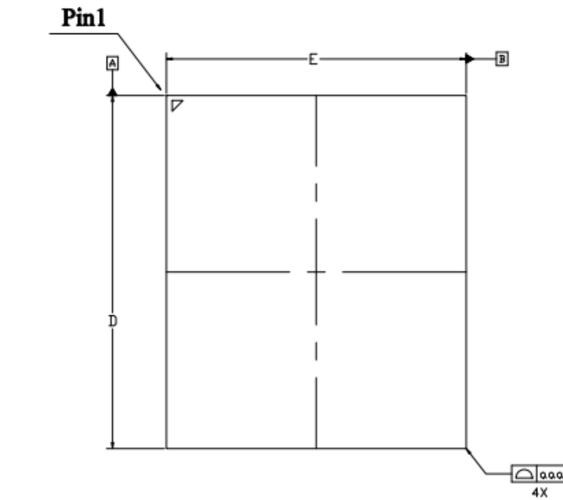
    where TSens = max(dRTTdT, dRONdTM) and VSens = max(dRTTdV, dRONdVM) define the SDRAM temperature and voltage sensitivities.
24. The tIS(base) AC150 specifications are adjusted from the tIS(base) specification by adding an additional 100 ps of derating to accommodate for the lower alternate threshold of 150 mV and another 25 ps to account for the earlier reference point [(175 mv - 150 mV) / 1 V/ns].
25. Pulse width of a input signal is defined as the width between the first crossing of VREF(DC) and the consecutive crossing of VREF(DC).
26. tDQSL describes the instantaneous differential input low pulse width on DQS - DQS, as measured from one falling edge

to the next consecutive rising edge.

27. tDQSH describes the instantaneous differential input high pulse width on DQS - DQS, as measured from one rising edge to the next consecutive falling edge.
28. tDQSH,act + tDQSL,act = 1 tCK,act ; with tXYZ,act being the actual measured value of the respective timing parameter in the application.
29. tDSH,act + tDSS,act = 1 tCK,act ; with tXYZ,act being the actual measured value of the respective timing parameter in the application.
30. tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.
31. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.
32. n = from 13 cycles to 50 cycles. This row defines 38 parameters.

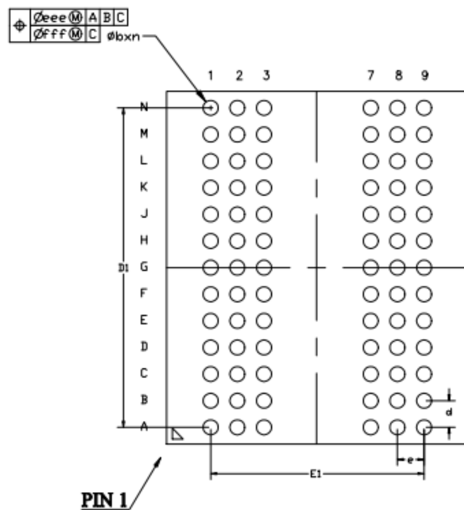
# 10 Package Outlines

**Figure 7** and

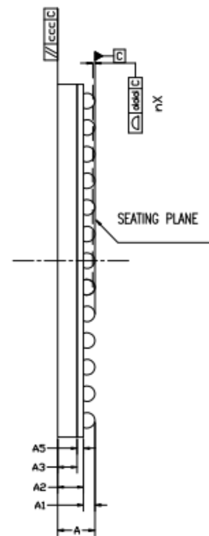



TOP VIEW

| | Symble | Dimension in mm | | | Dimension in inch | | |
|---|---|---|---|---|---|---|---|
| | | Min | Normal | Max | Min | Normal | Max |
| TOTAL THICKNESS | A | --- | 1.120 | 1.200 | --- | 0.0441 | 0.0472 |
| STAND OFF | A1 | 0.300 | 0.340 | 0.380 | 0.0118 | 0.0134 | 0.0150 |
| SBT+MOLD THICKNESS | A2 | 0.740 | 0.780 | 0.820 | 0.0291 | 0.0307 | 0.0323 |
| MOLD THICKNESS | A3 | 0.560 | 0.590 | 0.620 | 0.0220 | 0.0232 | 0.0244 |
| SUBSTRATE THICKNESS | A5 | 0.160 | 0.190 | 0.220 | 0.0063 | 0.0075 | 0.0087 |
| BALL WIDTH | Φb | 0.430 | 0.480 | 0.530 | 0.0169 | 0.0189 | 0.0209 |
| BALL PITCH | d | 0.800 | | | 0.0315 | | |
| | e | 0.800 | | | 0.0315 | | |
| BALL COUNT | n | 78 | | | | | |
| BODY SIZE | D | 10.500 | 10.600 | 10.700 | 0.4134 | 0.4173 | 0.4213 |
| | E | 8.900 | 9.000 | 9.100 | 0.3504 | 0.3543 | 0.3583 |
| EDGE BALL CENTER TO CENTER | D1 | 9.500 | 9.600 | 9.700 | 0.3740 | 0.3780 | 0.3819 |
| | E1 | 6.300 | 6.400 | 6.500 | 0.2480 | 0.2520 | 0.2559 |
| PKG EDGE TOLERANCE | aaa | 0.100 | | | 0.0039 | | |
| MOLD FLATNESS | ccc | 0.100 | | | 0.0039 | | |
| COPLANARITY | ddd | 0.080 | | | 0.0031 | | |
| BALL OFFSET(PACKAGE) | eee | 0.150 | | | 0.0059 | | |
| BALL OFFSET(BALL) | fff | 0.050 | | | 0.0020 | | |
| JEDEC | | MO-242(REF) | | | | | |



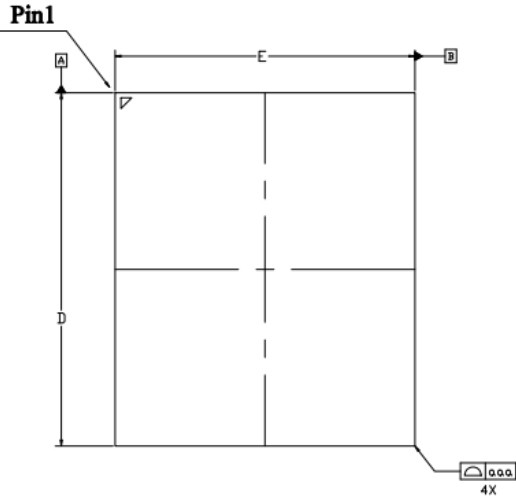

BOTTOM VIEW




SIDE VIEW

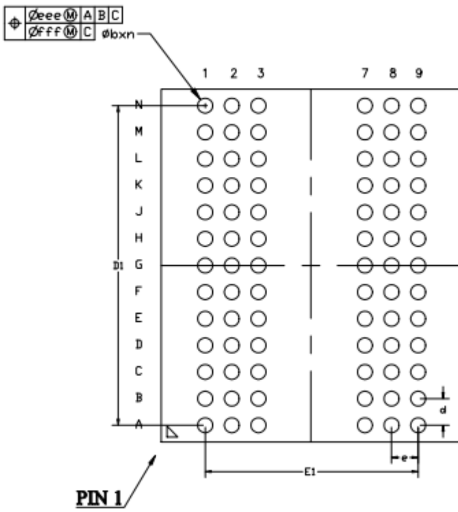
Figure 8 reflects the current status of the outline dimensions of the DDR3(L) packages for x8 & x16 configuration 8Gbit components.

**Figure 7 - Package outline x8**

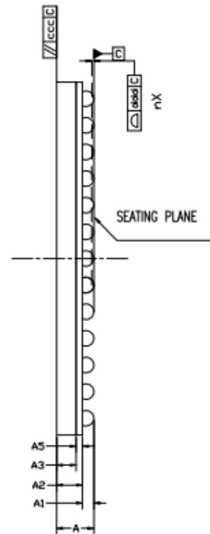



TOP VIEW

| | Symble | Dimension in mm | | | Dimension in inch | | |
|---|---|---|---|---|---|---|---|
| | | Min | Normal | Max | Min | Normal | Max |
| TOTAL THICKNESS | A | --- | 1.120 | 1.200 | --- | 0.0441 | 0.0472 |
| STAND OFF | A1 | 0.300 | 0.340 | 0.380 | 0.0118 | 0.0134 | 0.0150 |
| SBT+MOLD THICKNESS | A2 | 0.740 | 0.780 | 0.820 | 0.0291 | 0.0307 | 0.0323 |
| MOLD THICKNESS | A3 | 0.560 | 0.590 | 0.620 | 0.0220 | 0.0232 | 0.0244 |
| SUBSTRATE THICKNESS | A5 | 0.160 | 0.190 | 0.220 | 0.0063 | 0.0075 | 0.0087 |
| BALL WIDTH | Φb | 0.430 | 0.480 | 0.530 | 0.0169 | 0.0189 | 0.0209 |
| BALL PITCH | d | 0.800 | | | 0.0315 | | |
| | e | 0.800 | | | 0.0315 | | |
| BALL COUNT | n | 78 | | | | | |
| BODY SIZE | D | 10.500 | 10.600 | 10.700 | 0.4134 | 0.4173 | 0.4213 |
| | E | 8.900 | 9.000 | 9.100 | 0.3504 | 0.3543 | 0.3583 |
| EDGE BALL CENTER TO CENTER | D1 | 9.500 | 9.600 | 9.700 | 0.3740 | 0.3780 | 0.3819 |
| | E1 | 6.300 | 6.400 | 6.500 | 0.2480 | 0.2520 | 0.2559 |
| PKG EDGE TOLERANCE | aaa | 0.100 | | | 0.0039 | | |
| MOLD FLATNESS | ccc | 0.100 | | | 0.0039 | | |
| COPLANARITY | ddd | 0.080 | | | 0.0031 | | |
| BALL OFFSET(PACKAGE) | eee | 0.150 | | | 0.0059 | | |
| BALL OFFSET(BALL) | fff | 0.050 | | | 0.0020 | | |
| JEDEC | | MO-242(REF) | | | | | |

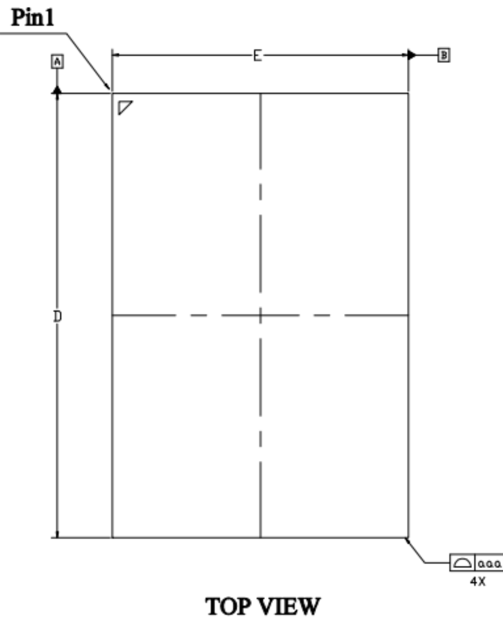



BOTTOM VIEW

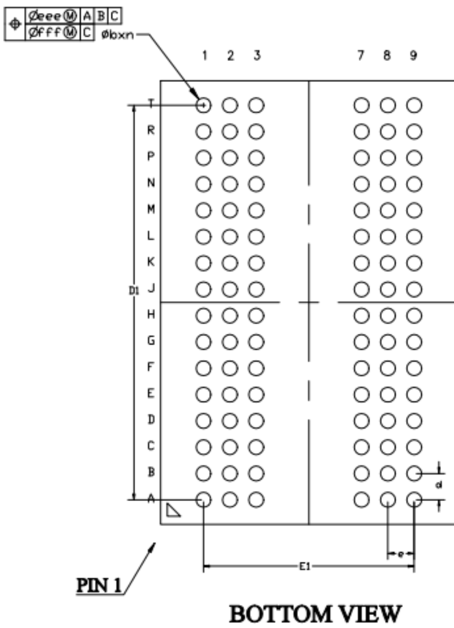


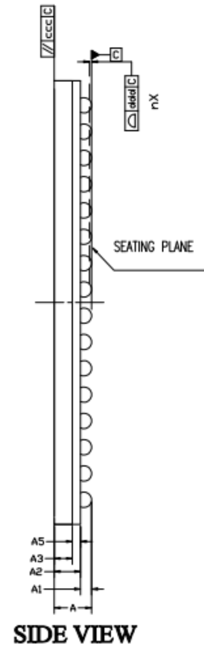

SIDE VIEW

**Figure 8 - Package outline x16**




| | Symble | Dimension in mm | | | Dimension in inch | | |
|---|---|---|---|---|---|---|---|
| | | Min | Normal | Max | Min | Normal | Max |
| TOTAL THICKNESS | A | --- | 1.12 | 1.20 | --- | 0.0441 | 0.0472 |
| STAND OFF | A1 | 0.30 | 0.34 | 0.38 | 0.0118 | 0.0134 | 0.0150 |
| SBT+MOLD THICKNESS | A2 | 0.74 | 0.78 | 0.82 | 0.0291 | 0.0307 | 0.0323 |
| MOLD THICKNESS | A3 | 0.560 | 0.59 | 0.620 | 0.0220 | 0.0232 | 0.0244 |
| SUBSTRATE THICKNESS | A5 | 0.165 | 0.19 | 0.215 | 0.0065 | 0.0075 | 0.0085 |
| BALL WIDTH | Φb | 0.43 | 0.48 | 0.53 | 0.0169 | 0.0189 | 0.0209 |
| BALL PITCH | d | | 0.80 | | | 0.0315 | |
| | e | | 0.80 | | | 0.0315 | |
| BALL COUNT | n | | | | 96 | | |
| BODY SIZE | D | 13.40 | 13.50 | 13.60 | 0.5276 | 0.5315 | 0.5354 |
| | E | 8.90 | 9.00 | 9.10 | 0.3504 | 0.3543 | 0.3583 |
| EDGE BALL CENTER TO CENTER | D1 | 11.90 | 12.00 | 12.10 | 0.4685 | 0.4724 | 0.4764 |
| | E1 | 6.30 | 6.40 | 6.50 | 0.2480 | 0.2520 | 0.2559 |
| PKG EDGE TOLERANCE | aaa | | 0.10 | | | 0.0039 | |
| MOLD FLATNESS | ccc | | 0.10 | | | 0.0039 | |
| COPLANARITY | ddd | | 0.08 | | | 0.0031 | |
| BALL OFFSET(PACKAGE) | eee | | 0.15 | | | 0.0059 | |
| BALL OFFSET(BALL) | fff | | 0.05 | | | 0.0020 | |
| JEDEC | | | | | MO-242(REF) | | |



# 11 Product Type Nomenclature

For reference the UniIC SDRAM component nomenclature is enclosed in this chapter

**Table 34 - DDR3(L) Memory Components**

| Field | Description | Values | Coding |
|---|---|---|---|
| 1 | UniIC Component Prefix | SCB | UniIC |
| 2 | Voltage | 13(15) | VDD, VDDQ=1.35V(1.5V) |
| 3 | DRAM Technology | H | DDR3 |
| 4 | Density | 8G | 8 Gbit |
| 5 | Number of I/Os | 80 | X8 |
| 6 | Number of dies | 2 | 2die |
| 7 | Product Variant | 0 .. 9 | – |
| 8 | Die Revision | A | First |
| | | B | Second |
| | | C | Third |
| 9 | Package, | F | FBGA |
| 10 | Power | – | Standard power product |
| | | L | Low power product |
| 11 | Speed Grade | 13K | CL–tRCD–tRP = 11-11-11 |
| | | 11M | CL–tRCD–tRP =13-13-13 |

# List of Figures

Figure 1 - Ball out for 1024 Mb ×8 Components (FBGA-78) ........ 6
Figure 2 - Ball out for 512 Mb ×16 Components (FBGA-96) ........ 7
Figure 3 - Reference Load for AC Timings and Output Slew Rates ........ 23
Figure 4 - AC Overshoot / Undershoot Definitions for Address and Control Signals ........ 30
Figure 5 - AC Overshoot / Undershoot Definitions for Clock, Data, Strobe and Mask Signals ........ 31
Figure 6 - Reference Load for AC Timings and Output Slew Rates ........ 36
Figure 7 - Package outline x8 ........ 47
Figure 8 - Package outline x16 ........ 48

# List of Tables

Table 1 - Ordering Information for 8Gbit DDR3(L) Component ..... 5
Table 2 - Ball out for 512 Mb ×16 Components (FBGA-96) ..... 8
Table 3 - Command Truth Table ..... 10
Table 4 - Clock Enable (CKE) Truth Table for Synchronous Transitions ..... 12
Table 5 - Data Mask (DM) Truth Table ..... 12
Table 6 - MR0 Mode register Definition (BA[2:0]=000B) ..... 13
Table 7 - MR1 Mode Register Definition (BA[2:0]=001B) ..... 15
Table 8 - MR2 Mode Register Definition (BA[2:0]=010B) ..... 17
Table 9 - MR3 Mode Register Definition (BA[2:0]=011B) ..... 19
Table 10 - Bit Order during Burst ..... 20
Table 11 - Absolute Maximum Ratings ..... 21
Table 12 - SDRAM Component Operating Temperature Range ..... 22
Table 13 - DC Operating Conditions ..... 22
Table 14 - Input and Output Leakage Currents ..... 22
Table 15 - DC and AC Input Levels for Single-Ended Command, Address and Control Signals ..... 24
Table 16 - DC and AC Input Levels for Single-Ended DQ and DM Signals ..... 24
Table 17 - Differential swing requirement for clock (CK - /CK) and strobe (DQS - /DQS) ..... 25
Table 18 - Allowed Time Before Ringback (tDVAC) for CK - /CK and DQS - /DQS ..... 25
Table 19 - Each Single-Ended Levels for CK, DQS, /DQS, /CK, ..... 26
Table 20 - Cross Point Voltage for Differential Input Signals (CK, DQS) ..... 26
Table 21 - DC and AC Output Levels for Single-Ended Signals ..... 26
Table 22 - AC Output Levels for Differential Signals ..... 27
Table 23 - Output Slew Rates ..... 27
Table 24 - ODT DC Impedance and Mid-Level Characteristics ..... 28
Table 25 - ODT DC Impedance after proper IO Calibration and Voltage/Temperature Drift ..... 28
Table 26 - OTD DC Impedance Sensitivity Parameters ..... 29
Table 27 - Interface Capacitance Values ..... 29
Table 28 - AC Overshoot / Undershoot Specification for Address and Control Signals ..... 30
Table 29 - AC Overshoot / Undershoot Specification for Clock, Data, Strobe and Mask Signals ..... 30
Table 30 - IDD & IDDQ Specification ..... 32
Table 31 - DDR3(L)-1600 Speed Bins ..... 33
Table 32 - DDR3(L)-1866 Speed Bins ..... 34
Table 33 - AC Timing parameters ..... 37
Table 34 - DDR3(L) Memory Components ..... 49

**Edition 2020-12**
**Published by**
**Xi'an UniIC Semiconductors CO., Ltd.**

**Xi'an: 4th Floor, Building A,**
**No. 38 Gaoxin 6th Road,**
**Xian High-tech Industries Development Zone**
**Xi'an, Shaanxi 710075, P. R. China**
**Tel: +86-29-88318000**
**Fax: +86-29-88453299**

**info@unisemicon.com**

**© UniIC 2020.**
**All Rights Reserved.**

**Legal Disclaimer**

THE INFORMATION GIVEN IN THIS INTERNET DATA SHEET SHALL IN NO EVENT BE REGARDED AS A GUARANTEE OF CONDITIONS OR CHARACTERISTICS. WITH RESPECT TO ANY EXAMPLES OR HINTS GIVEN HEREIN, ANY TYPICAL VALUES STATED HEREIN AND/OR ANY INFORMATION REGARDING THE APPLICATION OF THE DEVICE, UNIIC HEREBY DISCLAIMS ANY AND ALL WARRANTIES AND LIABILITIES OF ANY KIND, INCLUDING WITHOUT LIMITATION WARRANTIES OF NON-INFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS OF ANY THIRD PARTY.

**Information**

For further information on technology, delivery terms and conditions and prices please contact your nearest UniIC Office.

**Warnings**

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest UniIC Office.
UniIC Components may only be used in life-support devices or systems with the express written approval of UniIC, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

**www.unisemicon.com**