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SCB12Q8G800BF
SCB12Q8G160BF

8Gbit DDR4 SDRAM
EU RoHS Compliant Products

Data Sheet

Rev. B

Revision History		
Date	**Revision**	**Subjects (major changes since last revision)**
2024-5	A	First version release
2024-9	B	Updated Table 50-52 in Chapter 8.1 IDD Specifications. Updated Figure2.

Contents

1 Features

- Power supply: V_{DD} = V_{DDQ} = 1.2V (1.14V to 1.26V); V_{PP} = 2.5V (2.375V to 2.75V)
- JEDEC standard package:
  - 96-Ball FBGA (x16)
  - 78-Ball FBGA (x8)
- Array Configuration:
  - 8 Banks (x16) 2 groups of 4 banks
  - 16 Banks (x 8) 4 groups of 4 banks
- 8n-Bit prefetch architecture
- Burst Length (BL): 8 and 4 with Burst Chop (BC)
- Programmable CAS Latency (CL)
- Programmable CAS Write Latency (CWL)
- Internal generated V_{REF} for data inputs
- Data Mask (DM) for write data
- On-Die Termination (ODT): Support Nominal, Park and Dynamic ODT
- Interface: 1.2V Pseudo Open Drain (POD) IO
- Differential clock and data strobe inputs (CK_t ,CK_c; DQS_t, DQS_c)
- Per DRAM Addressability (PDA)
- Data Bus Inversion (DBI)
- Asynchronous reset for power up
- Maximum Power Saving Mode (MPSM)
- Precharge: Auto precharge option for each burst access
- Operating case temperature: -40°C≤ T_{CASE} ≤ 95°C
- Support auto-refresh and self-refresh mode
- Average Refresh Period:
  -7.8μs at -40°C ≤ T_{CASE} ≤ 85°C

  -3.9μs at 85°C < T_{CASE} ≤ 95°C
- Fine granularity refresh 2x, 4x mode for smaller t_{RFC}
- Programmable data strobe preambles
- Command Address (CA) Parity is supported
- Write Cyclic Redundancy Code (CRC) is supported
- Connectivity test mode (TEN) is supported
- Gear Down Mode
- Output driver calibration through ZQ pin (R_{ZQ}: 240ohm ± 1%)
- JEDEC JESD-79-4D compliant
- RoHS compliant

Note:

1. The functionality described and the timing specifications included in this datasheet are for the DLL Enabled mode of operation (normal operation), unless specifically stated otherwise.

1.1 Speed Bins

Table 1 - Speed Bins

Speed	DDR4-2400	DDR4-2666	DDR4-3200	Unit
	17-17-17	19-19-19	22-22-22	
$t_{CK\ (min)}$	0.833	0.75	0.625	ns
CAS Latency	17	19	22	nCK
$t_{RCD\ (min)}$	14.16	14.25	13.75	ns
$t_{RP\ (min)}$	14.16	14.25	13.75	ns
$t_{RAS\ (min)}$	32	32	32	ns
$t_{RC\ (min)}$	46.16	46.25	45.75	ns

1.2 Product List

Table 2 shows all possible products within the 8Gbit DDR4 SDRAM component generation.

Table 2 - Ordering Information for 8Gbit DDR4 Component

UniIC Part Number	Max. Clock frequency	CAS-RCD-RP latencies	Speed Sort Name	Package
8Gbit DDR4 SDRAM Components in × 8 Organization (1024 M × 8)				
Commercial Temperature Range (0°C- 95°C)				
SCB12Q8G800BF-07Q	1333 MHz	19-19-19	DDR4–2666V	PG-FBGA-78
SCB12Q8G800BF-06S	1600 MHz	22-22-22	DDR4–3200S	PG-FBGA-78
Industrial Temperature Range (-40°C- 95°C)				
SCB12Q8G800BF-07QI	1333 MHz	19-19-19	DDR4–2666V	PG-FBGA-78
SCB12Q8G800BF-06SI	1600 MHz	22-22-22	DDR4–3200S	PG-FBGA-78
8Gbit DDR4 SDRAM Components in × 16 Organization (512M × 16)				
Commercial Temperature Range (0°C- 95°C)				
SCB12Q8G160BF-07Q	1333 MHz	19-19-19	DDR4–2666V	PG-FBGA-96
SCB12Q8G160BF-06S	1600 MHz	22-22-22	DDR4–3200S	PG-FBGA-96
Industrial Temperature Range (-40°C- 95°C)				
SCB12Q8G160BF-07QI	1333 MHz	19-19-19	DDR4–2666V	PG-FBGA-96
SCB12Q8G160BF-06SI	1600 MHz	22-22-22	DDR4–3200S	PG-FBGA-96

1.3 Address Table

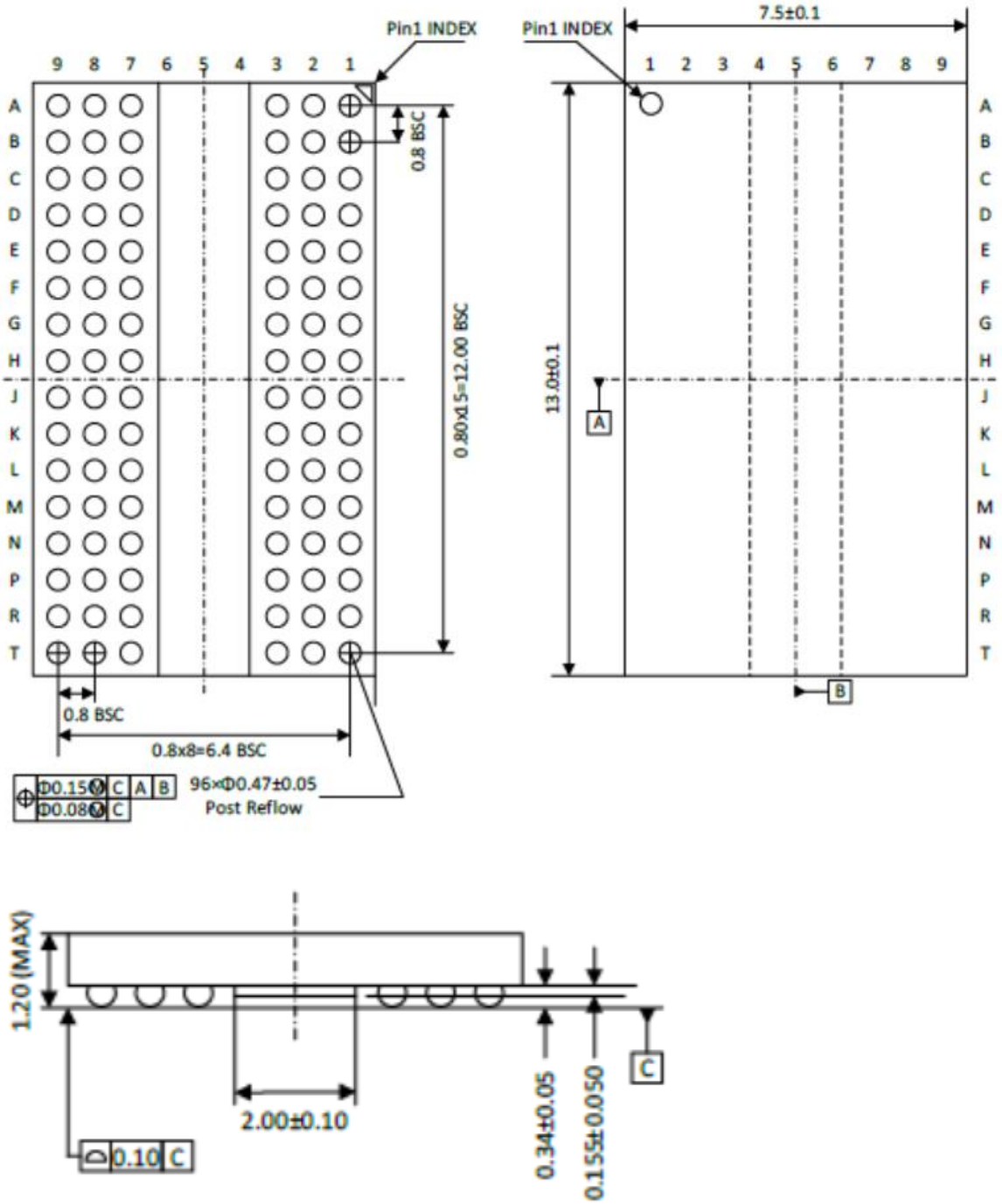
Table 3 – Address Table

Parameter	1024Mb × 8	512Mb × 16
Number of bank groups	4	2
Bank group address	BG[1:0]	BG0
Bank count per group	4	4
Bank address in bank group	BA[1:0]	BA[1:0]
Row Address	64K (A[15:0])	64K (A[15:0])
Column Address	1K(A[9:0])	1K(A[9:0])
Page Size	1KB	2KB

2 Package Information

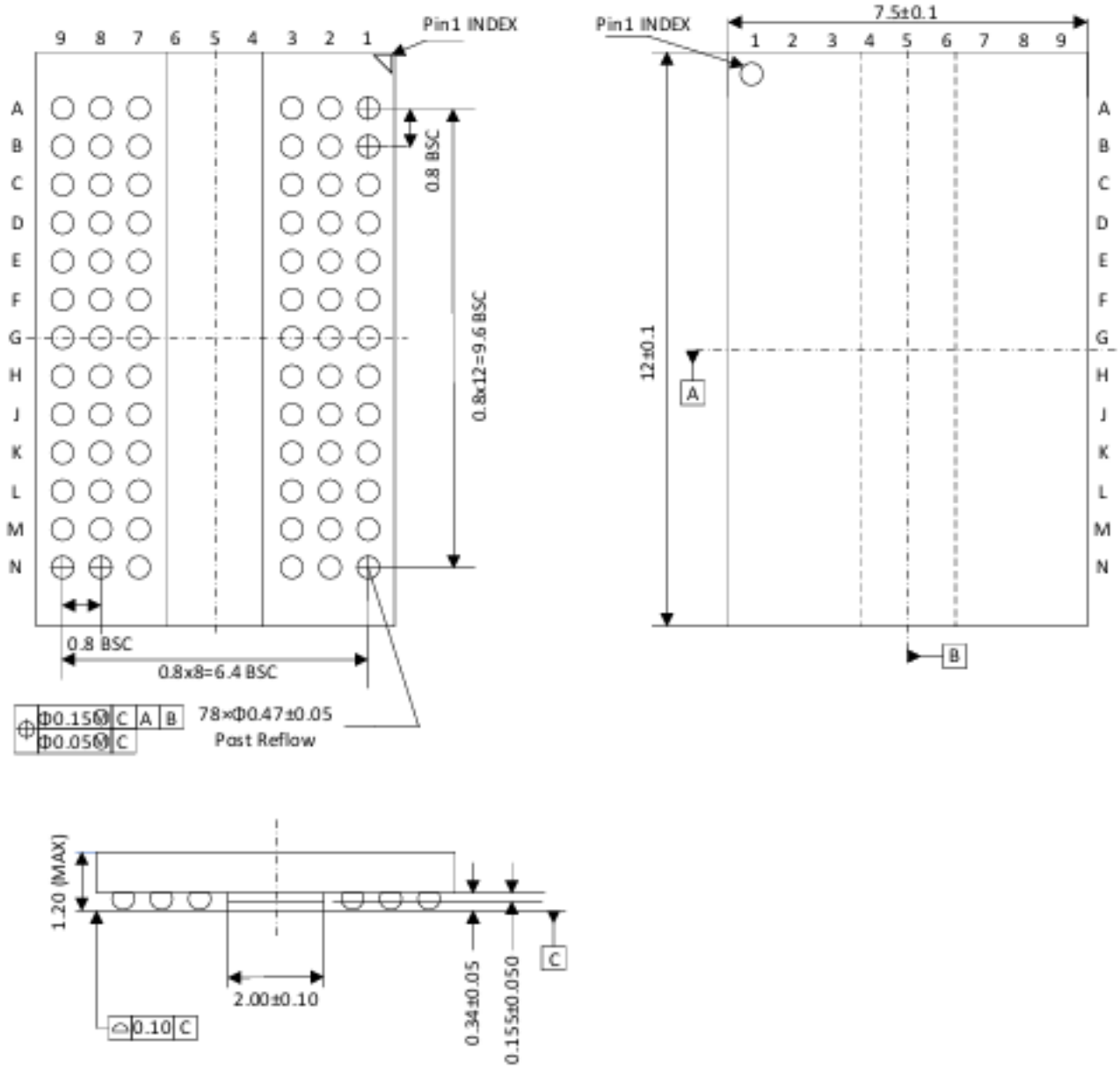
2.1 Package 96-Ball FBGA (x16)

Figure 1 Package 96-Ball FBGA(x16)



2.2 Package 78-Ball FBGA (x8)

Figure 2 Package 78-Ball FBGA(x8)



3 Ball Assignments

3.1 96-Ball FBGA (x16) Ball Assignments

Figure 3 Ball FBGA (x16) Ball Assignments

	1	2	3	4	5	6	7	8	9	
A	VDDQ	VSSQ	DQU0				DQSU_c	VSSQ	VDDQ	A
B	VPP	VSS	VDD				DQSU_t	DQU1	VDD	B
C	VDDQ	DQU4	DQU2				DQU3	DQU5	VSSQ	C
D	VDD	VSSQ	DQU6				DQU7	VSSQ	VDDQ	D
E	VSS	DMU_n/ DBIU_n	VSSQ				DML_n DBIL_n	VSSQ	VSS	E
F	VSSQ	VDDQ	DQSL_c				DQL1	VDDQ	ZQ	F
G	VDDQ	DQL0	DQSL_t				VDD	VSS	VDDQ	G
H	VSSQ	DQL4	DQL2				DQL3	DQL5	VSSQ	H
J	VDD	VDDQ	DQL6				DQL7	VDDQ	VDD	J
K	VSS	CKE	ODT				CK_t	CK_c	VSS	K
L	VDD	WE_n/ A14	ACT_n				CS_n	RAS_n/ A16	VDD	L
M	VREFCA	BG0	A10/ AP				A12/ BC_n	CAS_n/ A15	VSS	M
N	VSS	BA0	A4				A3	BA1	TEN	N
P	RESET_n	A6	A0				A1	A5	ALERT_n	P
R	VDD	A8	A2				A9	A7	VPP	R
T	VSS	A11	PAR				NC	A13	VDD	T

3.2 78-Ball FBGA (x8) Ball Assignments

Figure 4 78-Ball FBGA (x8) Ball Assignments

	1	2	3	4	5	6	7	8	9	
A	VDD	VSSQ	TDQS_c				DM_n, DBI_n TDQS_t	VSSQ	VSS	A
B	VPP	VDDQ	DQS_c				DQ1	VDDQ	ZQ	B
C	VDDQ	DQ0	DQS_t				VDD	VSS	VDDQ	C
D	VSSQ	DQ4	DQ2				DQ3	DQ5	VSSQ	D
E	VSS	VDDQ	DQ6				DQ7	VDDQ	VSS	E
F	VDD	NC	ODT				CK_t	CK_c	VDD	F
G	VSS	NC	CKE				CS_n	NC	TEN	G
H	VDD	WE_n A14	ACT_n				CAS_n A15	RAS_n A16	VSS	H
J	VREFCA	BG0	A10 AP				A12 BC_n	BG1	VDD	J
K	VSS	BA0	A4				A3	BA1	VSS	K
L	RESET_n	A6	A0				A1	A5	ALERT_n	L
M	VDD	A8	A2				A9	A7	VPP	M
N	VSS	A11	PAR				NC	A13	VDD	N

3.3 Ball Description

Table 4 – Ball Description

Symbol	Type	Function
CK_t, CK_c	Input	**Clock:** CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE	Input	**Clock Enable:** CKE HIGH activates, and CKE LOW deactivates, internal clock signals and device input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER- DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER-DOWN (row active in any bank). CKE is synchronous for self-refresh exit. After V_{REFCA} and Internal DQ V_{REF} have become stable during the power-on and initialization sequence, they must be maintained during all operations (including SELF REFRESH). CKE must be maintained HIGH throughout read and write accesses. Input buffers, excluding CK_t, CK_c, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during SELF REFRESH.
CS_n	Input	**Chip Select:** All commands are masked when CS_n is registered HIGH. CS_n provides for external rank selection on systems with multiple ranks. CS_n is considered part of the command code.
ODT	Input	**On Die Termination:** ODT (registered HIGH) enables R_{TT_NOM} termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c, DM_n/DBI_n/TDQS_t and TDQS_c (When TDQS is enabled via Mode Register A11 = 1 in MR1) signal for x8 configurations. For x16 configuration ODT is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, DMU_n, and DML_n signal. The ODT pin will be ignored if MR1 is programmed to disable R_{TT_NOM}.
ACT_n	Input	**Activation Command Input:** ACT_n defines the ACTIVATION command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/ A14 will be considered as Row Address A16, A15 and A14.
RAS_n/A16, CAS_n/A15, WE_n/A14	Input	**Command Inputs:** RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. These balls have multi function. For example, for activation with ACT_n LOW, those are Addressing like A16, A15 and A14 but for non-ACTIVATION command with ACT_n HIGH, those are command pins for READ, WRITE and other command defined in command truth table in JESD79-4D.
DM_n, DBI_n DMU_n/ DBIU_n DML_n/ DBIL_n	I/O	**Input Data Mask and Data Bus Inversion:** DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a write access. DM_n is sampled on both edges of DQS. DM is muxed with DBI function by Mode Register A10, A11, A12 setting in MR5. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH. TDQS is only supported in x8.
BG[1:0]	Input	**Bank Group Inputs:** BG[1:0] define the bank group to which an ACTIVE, READ, WRITE or PRECHARGE command is being applied. BG0 also determines which mode register is to be accessed during an MRS cycle. x4/x8 have BG0 and BG1, but x16 has only BG0.
BA[1:0]	Input	**Bank Address Inputs:** BA[1:0] define the bank to which an ACTIVE, READ, WRITE or PRECHARGE command is being applied. Bank address also determines which mode register is to be accessed during an MRS cycle.
A[17:0]	Input	**Address Inputs:** Provide the row address for ACTIVATE commands and the column address for READ/WRITE commands to select one location out of the memory array in the respective bank. (A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions, see other rows.) The address inputs also provide the op-code during MODE REGISTER SET commands.

Symbol	Type	Function
A10/AP	Input	**Auto-precharge:** A10 is sampled during READ/WRITE commands to determine whether Auto-precharge should be performed to the accessed bank after the READ/WRITE operation. (HIGH: Auto-precharge; LOW: No Auto-precharge). A10 is sampled during a PRECHARGE command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12/BC_n	Input	**Burst Chop:** A12/BC_n is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed. (HIGH: no burst chop; LOW: burst chopped). See "Command Truth Table" in JESD79-4D.
RESET_n	Input	**Active LOW Asynchronous Reset:** Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC HIGH and LOW at 80% and 20% of V_{DD}.
DQ DQL, DQU	I/O	**Data Input/Output:** Bi-directional data bus. If CRC is enabled via mode register, then CRC code is added at the end of data burst. Any DQ from DQ3 ~ DQ0 may indicate the internal V_{REF} level during test via mode register setting MR4 A4 = HIGH. During this mode, R_{TT} value should be set to High-Z. This measurement is for verification purposes and is NOT an external voltage supply pin.
DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c	I/O	**Data Strobe:** Output with READ data, input with WRITE data. Edge-aligned with READ data, centered-aligned with WRITE data. For x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS_t, DQSL_t and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.
TDQS_t, TDQS_c	Output	**Termination Data Strobe:** TDQS_t/TDQS_c is applicable for x8 DRAMs only. When enabled via mode register A11 = 1 in MR1, the DRAM will enable the same R_{TT} termination resistance function on TDQS_t/TDQS_c that is applied to DQS_t/DQS_c. When the TDQS function is disabled via mode register A11 = 0 in MR1, DM/DBI/TDQS pin will provide the Data Mask (DM) function or Data Bus Inversion (DBI) depending on MR5; A11, A12, A10 and TDQS_c is not used. x4/ x16 DRAMs must disable the TDQS function via mode register A11 = 0 in MR1.
PAR	Input	**Command and Address Parity Input:** DDR4 Supports Even Parity check in DRAMs with MR setting. Once it is enabled via Register in MR5, then DRAM calculates Parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG[1:0], BA[1:0], A[17:0]. Command and address inputs shall have parity check performed when commands are latched via the rising edge of CK_t and when CS_n is LOW.
ALERT_n	I/O	**Alert:** It has multi functions such as CRC error flag, command and address parity error flag as output signal. If there is error in CRC, then Alert_n goes LOW for the period time interval and goes back HIGH. If there is error in command address parity check, then ALERT_n goes LOW for relatively long period until on going DRAM internal recovery transaction to complete. During connectivity test mode, this pin works as an input. Using this signal or not is dependent on system. In case of not connected as signal, ALERT_n pin must be bounded to V_{DD} on board.
TEN	Input	**Connectivity Test Mode Enable:** TEN is active when HIGH and inactive when LOW. TEN must be LOW during normal operation. It is equired on x16 devices and optional input on x4/x8 with densities equal to or greater than 8Gb. HIGH in this pin will enable connectivity test mode operation along with other pins. It is a CMOS rail to rail signal with AC HIGH and LOW at 80% and 20% of V_{DD}. Using this signal or not is dependent on system. This pin may be DRAM internally pulled low through a weak pull-down resistor to V_{SS}.
NC	-	**No Connect:** No internal electrical connection is present.
V_{DDQ}	Supply	**DQ Power Supply:** 1.2V ± 0.06V

Symbol	Type	Function
V_{SSQ}	Supply	**DQ Ground**
V_{DD}	Supply	**Power Supply:** 1.2V ± 0.06V
V_{SS}	Supply	**Ground**
V_{PP}	Supply	**DRAM Activating Power Supply:** 2.5V (2.375V min, 2.75V max)
V_{REFCA}	Supply	**Reference Voltage for CA**
ZQ	Supply	**Reference Pin for ZQ Calibration**

4 Absolute Maximum Ratings

4.1 Absolute Maximum DC Ratings

Table 5 - Absolute Maximum DC Ratings

Symbol	Parameter	Min	Max	Unit	Note
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}	-0.3	1.5	V	1,3
V_{DDQ}	Voltage on V_{DDQ} pin relative to V_{SS}	-0.3	1.5	V	1,3
V_{PP}	Voltage on V_{PP} pin relative to V_{SS}	-0.3	3.0	V	4
V_{IN}, V_{OUT}	Voltage on any pin except V_{REFCA} relative to V_{SS}	-0.3	1.5	V	1,3,5
T_{STG}	Storage temperature	-55	100	°C	1,2

Note:

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. V_{DD} and V_{DDQ} must be within 300mV of each other at all times; and V_{REFCA} must not be greater than 0.6 * V_{DDQ}, When V_{DD} and V_{DDQ} are less than 500mV; V_{REF} may be equal to or less than 300mV.
4. V_{PP} must be equal to or greater than V_{DD}/V_{DDQ} at all times.
5. Overshoot area above 1.5V is specified in Section 6.3.5 and Section 6.3.6.

4.2 Recommended Supply Operating Conditions

Table 6 - Recommended Supply Operating Conditions

Symbol	Parameter	Ratings			Unit	Note
		Min	Typ.	Max		
V_{DD}	Supply voltage	1.14	1.2	1.26	V	1,2,3
V_{DDQ}	Supply voltage for output	1.14	1.2	1.26	V	1,2,3
V_{PP}	Wordline supply voltage	2.375	2.5	2.75	V	3

Note:

1. Under all conditions V_{DDQ} must be less than or equal to V_{DD}.
2. V_{DDQ} tracks with V_{DD}. AC parameters are measured with V_{DD} and V_{DDQ} tied together.
3. DC bandwidth is limited to 20MHz.

4.3 DRAM Component Operating Temperature Range

Table 7 - Operating Temperature Range

Symbol	Parameter	Rating	Unit	Note
T_{OPER}	Normal temperature range	0 ~ 85	°C	1,2
	Wide temperature	-40 ~ 85	°C	1,2
	Extended temperature range	85 ~ 95	°C	1,3
	Industrial temperature	-40~95	°C	1,2,3

Note:

1. Operating temperature T_{OPER} is the case surface temperature on the center/top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
2. The normal temperature range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 - 95°C under all operating conditions for the commercial offering; The wide temperature offerings allow the case temperature to go below 0°C to -40°C.
3. Some applications require operation of the DRAM in the extended temperature range between 85°C and 95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:

- REFRESH commands must be doubled in frequency, therefore reducing the refresh interval t_{REFI} to 3.9µs. It is also possible to specify a component with 1X refresh (t_{REFI} to 7.8µs) in the extended temperature range. Please refer to the DIMM SPD for option availability.
- If SELF REFRESH operation is required in the extended temperature range, then it is mandatory to either use the manual self refresh mode with extended temperature range capability (MR2 A6 = 0 and MR2 A7 = 1) or enable the optional auto self refresh mode (MR2 A6 = 1 and MR2 A7 = 1).

5 AC And DC Input Measurement Levels

5.1 AC and DC Logic Input Levels for Single-ended Signals

Table 8 - Single-ended AC and DC Input Levels for Command and Address

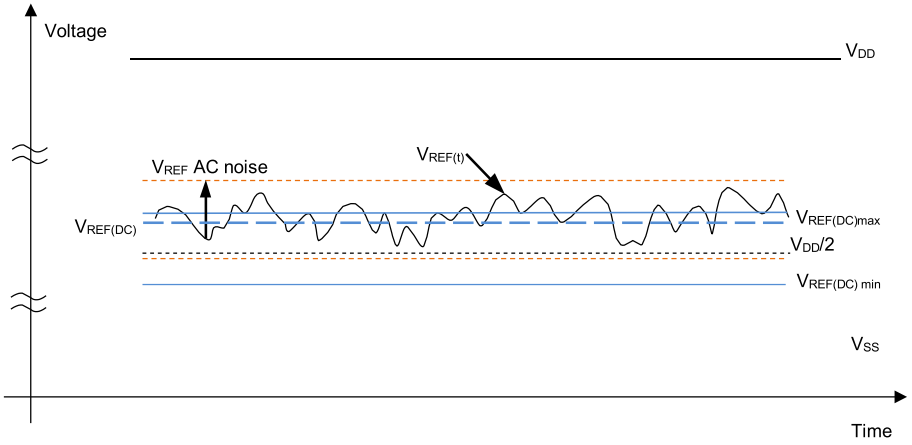
Symbol	Parameter	1600/1866/2133/2400		2666/2933/3200		Unit	Note
		Min	Max	Min	Max		
$V_{IH(DC75)}$	DC input logic HIGH	V_{REFCA} + 0.075	V_{DD}	-	-	V	-
$V_{IL(DC75)}$	DC input logic LOW	V_{SS}	V_{REFCA} - 0.075	-	-	V	-
$V_{IH(DC65)}$	DC input logic HIGH	-	-	V_{REFCA} + 0.065	V_{DD}	V	-
$V_{IL(DC65)}$	DC input logic LOW	-	-	V_{SS}	V_{REFCA} - 0.065	V	-
$V_{IH(AC100)}$	AC input logic HIGH	V_{REF} + 0.1	Note 2	-	-	V	1
$V_{IL(AC100)}$	AC input logic LOW	Note 2	V_{REF} - 0.1	-	-	V	1
$V_{IH(AC90)}$	AC input logic HIGH	-	-	V_{REF} + 0.09	Note 2	V	1
$V_{IL(AC90)}$	AC input logic LOW	-	-	Note 2	V_{REF} - 0.09	V	1
$V_{REFCA(DC)}$	Reference voltage for ADD, CMD inputs	0.49 * V_{DD}	0.51 * V_{DD}	0.49 * V_{DD}	0.51 * V_{DD}	V	2,3

Note:
1. See “Overshoot/Undershoot Specifications” in Section 6.3.4.
2. The AC peak noise on V_{REFCA} may not allow V_{REFCA} to deviate from $V_{REFCA(DC)}$ by more than ± 1%V_{DD} (for reference: approx. ± 12mV)
3. For reference: approx. V_{DD}/2 ± 12mV

5.2 AC and DC Logic Input Measurement Levels: V_{REF} Tolerances

The DC-tolerance limits and AC-noise limits for the reference voltages V_{REFCA} are illustrated in the Figure 2 below. It shows a valid reference voltage $V_{REF(t)}$ as a function of time. (V_{REF} stands for V_{REFCA}).
$V_{REF(DC)}$ is the linear average of $V_{REF(t)}$ over a very long period of time (for example, 1 second). This average has to meet the min/max requirements in Figure 2. Furthermore $V_{REF(t)}$ may temporarily deviate from $V_{REF(DC)}$ by no more than ± 1% V_{DD} for the AC-noise limit.

Figure 5 - Illustration of $V_{REF(DC)}$ Tolerance and V_{REF} AC-noise Limits

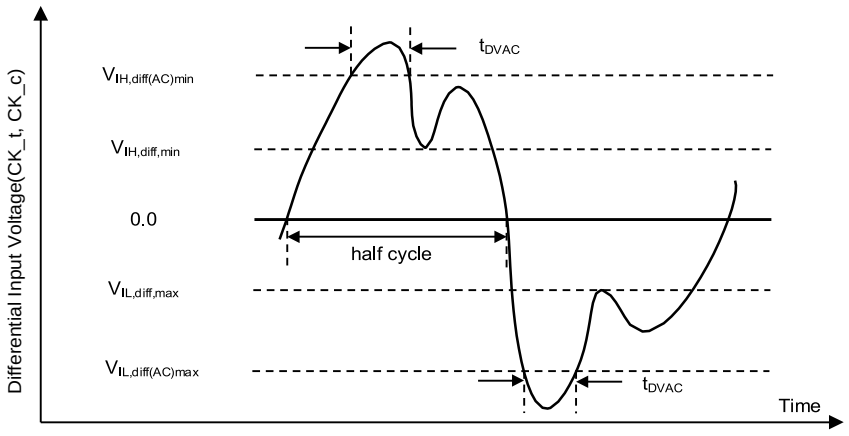


The voltage levels for setup and hold time measurements $V_{IH(AC)}$, $V_{IH(DC)}$, $V_{IL(AC)}$ and $V_{IL(DC)}$ are dependent on V_{REF}.
"V_{REF}" should be understood as $V_{REF(DC)}$.
This clarifies that DC-variations of V_{REF} affect the absolute voltage a signal has to reach to achieve a valid HIGH or LOW level, and therefore, the time to which setup and hold is measured. System timing and voltage budgets need to account for $V_{REF(DC)}$ deviations from the optimum position within the data-eye of the input signals.
This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with V_{REF} AC-noise. Timing and voltage effects due to AC-noise on V_{REF} up to the specified limit (± 1% of V_{DD}) are included in DRAM timings and their associated deratings.

5.3 AC and DC Logic Input Levels for Differential Signals

5.3.1 AC and DC Logic Input Levels for Differential Signals

Figure 6 - Definition of Differential AC-Swing and "Time above AC-Level" t_{DVAC}



Note:
1. Differential signal rising edge from $V_{IL,diff,max}$ to $V_{IH,diff(AC)min}$ must be monotonic slope.
2. Differential signal falling edge from $V_{IH,diff,min}$ to $V_{IL,diff(AC)max}$ must be monotonic slope.

5.3.2 Differential Swing Requirements for Clock (CK_t - CK_c)

Table 9 - Differential Input Levels Requirements for CK_t - CK_c

Symbol	Parameter	1600/1866/2133		2400/2666		2933		3200		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
$V_{IH,diff}$	Differential input high	+0.150	Note 3	+0.135	Note 3	125	Note 3	+0.110	Note 3	V	1
$V_{IL,diff}$	Differential input low	Note 3	-0.150	Note 3	-0.135	Note 3	-125	Note 3	-0.110	V	1
$V_{IH,diff(AC)}$	Differential input high (AC)	2 * ($V_{IH(AC)}$ - V_{REF})	Note 3	2 * ($V_{IH(AC)}$ - V_{REF})	Note 3	2 * ($V_{IH(AC)}$ - V_{REF})	Note 3	2 * ($V_{IH(AC)}$ - V_{REF})	Note 3	V	2
$V_{IL,diff(AC)}$	Differential input low (AC)	Note 3	2 * ($V_{IL(AC)}$ - V_{REF})	Note 3	2 * ($V_{IL(AC)}$ - V_{REF})	Note 3	2 * ($V_{IL(AC)}$ - V_{REF})	Note 3	2 * ($V_{IL(AC)}$ - V_{REF})	V	2

Note:
1. Used to define a differential signal slew-rate.
2. For CK_t - CK_c use $V_{IH(AC)}$/$V_{IL(AC)}$ of ADD/CMD and V_{REFCA}.
3. These values are not defined; however, the differential signals (CK_t - CK_c) need to be within the respective limits ($V_{IH(DC)max}$, $V_{IL(DC)min}$) for single-ended signals as well as the limitations for overshoot and undershoot.

Table 10 - Allowed Time before Ringback (t_{DVAC}) for CK_t - CK_c

Slew Rate [V/ns]	t_{DVAC} [ps] @ $\|V_{IHL,diff(AC)}\|$ = 200mV		t_{DVAC} [ps] @ $\|V_{IHL,diff(AC)}\|$ = TBDmV	
	Min	Max	Min	Max
>4.0	120	-	TBD	-
4.0	115	-	TBD	-
3.0	110	-	TBD	-
2.0	105	-	TBD	-
1.8	100	-	TBD	-
1.6	95	-	TBD	-
1.4	90	-	TBD	-
1.2	85	-	TBD	-
1.0	80	-	TBD	-
<1.0	80	-	TBD	-

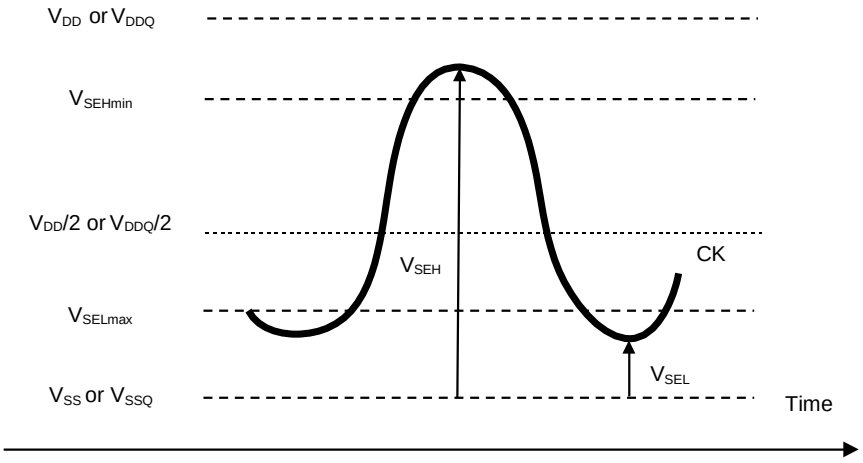
5.3.3 Differential Swing Requirements for Clock (CK_t - CK_c)

Each individual component of a differential signal (CK_t, CK_c) has also to comply with certain requirements for single-ended signals.

CK_t and CK_c have to approximately reach V_{SEHmin}/V_{SELmax} (approximately equal to the AC-levels ($V_{IH(AC)}/V_{IL(AC)}$) for ADD/CMD signals) in every half-cycle.

Note that the applicable AC-levels for ADD/CMD might be different per speed-bin etc. E.g., if different value than $V_{IH(AC100)}/V_{IL(AC100)}$ is used for ADD/CMD signals, then these AC-levels apply also for the single-ended signals CK_t and CK_c.

Figure 7 - Single-ended Requirement for differential signals



Note that, while ADD/CMD signal requirements are with respect to VREFCA, the single-ended components of differential signals have a requirement with respect to VDD/2, this is nominally the same. The transition of single-ended signals through the AC-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach VSELmax, VSEHmin has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

Table 11 - Single-ended Levels for CK_t, CK_c

Symbol	Parameter	1600/1866/2133		2400/2666		2933/3200		Unit	Note
		Min	Max	Min	Max	Min	Max		
V_{SEH}	Single-ended high-level for CK_t, CK_c	$V_{DD}/2$ + 0.100	Note 3	$V_{DD}/2$ + 0.095	Note 3	$V_{DD}/2$ + 0.085	Note 3	V	1,2
V_{SEL}	Single-ended low-level for CK_t, CK_c	Note 3	$V_{DD}/2$ - 0.100	Note 3	$V_{DD}/2$ - 0.095	Note 3	$V_{DD}/2$ - 0.085	V	1,2

Note:

1. For CK_t - CK_c use $V_{IH(AC)}/V_{IL(AC)}$ of ADD/CMD and V_{REFCA}.
2. $V_{IH(AC)}/V_{IL(AC)}$ for ADD/CMD is based on V_{REFCA}.
3. These values are not defined, however the single-ended signals CK_t, CK_c needs to be within the respective limits ($V_{IH\ (DC)max}$, $V_{IL(DC)min}$) for single-ended signals as well as the limitations for overshoot and undershoot.

5.3.4 Address, Command, and Control Overshoot/Undershoot Specifications

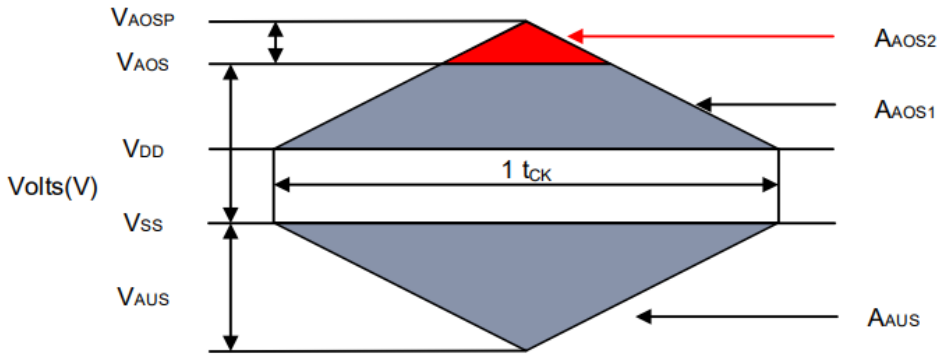
Table 12 - AC Overshoot/Undershoot Specification for Address, Command, and Control Pins

Parameter	Symbol	1600	1866	2133	2400	2666	2933	3200	Unit	Note
Maximum peak amplitude above V_{AOS}	V_{AOSP}	0.06							V	-
Upper boundary of overshoot area A_{AOS1}	V_{AOS}	V_{DD} + 0.24							V	1
Maximum peak amplitude allowed for undershoot area	V_{AUS}	0.30							V	-
Maximum overshoot area per 1 t_{CK} above V_{AOS}	A_{AOS2}	0.0083	0.0071	0.0062	0.0055	0.0055	0.0055	0.0055	V-ns	-
Maximum overshoot area per 1 t_{CK} between V_{DD} and V_{AOS}	A_{AOS1}	0.2550	0.2185	0.1914	0.1699	0.1699	0.1699	0.1699	V-ns	-
Maximum undershoot area per 1 t_{CK} below V_{SS}	A_{AUS}	0.2644	0.2265	0.1984	0.1762	0.1762	0.1762	0.1762	V-ns	-
(A0-A13, A17, BG0-BG1, BA0-BA1, ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, CS_n, CKE, ODT, C2-C0)										

Note:

1. The value of V_{AOS} matches V_{DD} absolute max as defined in Table 5 if V_{DD} equals V_{DD} max as defined inTable 6. If V_{DD} is above the recommended operating conditions, V_{AOS} remains at V_{DD} absolute max as defined in Table 5.

Figure 8 - Address, Command, and Control Overshoot and Undershoot Definition



5.3.5 Clock Overshoot/Undershoot Specifications

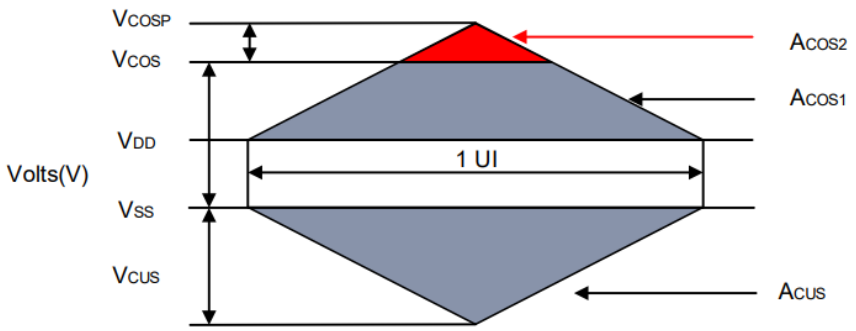
Table 13 - AC Overshoot/Undershoot Specification for Clock

Parameter	Symbol	1600	1866	2133	2400	2666	2933	3200	Unit	Note
Maximum peak amplitude above V_{COS}	V_{COSP}	0.06							V	-
Upper boundary of overshoot area A_{COS1}	V_{COS}	V_{DD} + 0.24							V	1
Maximum peak amplitude allowed for undershoot	V_{CUS}	0.30							V	-
Maximum overshoot area per 1 UI above V_{COS}	A_{COS2}	0.0038	0.0032	0.0028	0.0025	0.0025	0.0025	0.0025	V-ns	-
Maximum overshoot area per 1 UI between V_{DD} and V_{COS}	A_{COS1}	0.1125	0.0964	0.0844	0.0750	0.0750	0.0750	0.0750	V-ns	-
Maximum undershoot area per 1 UI below V_{SS}	A_{CUS}	0.1144	0.098	0.0858	0.0762	0.0762	0.0762	0.0762	V-ns	-
(CK_t, CK_c)										

Note:

3. The value of V_{COS} matches V_{DD} absolute max as defined in Table 6 if V_{DD} equals V_{DD} max as defined in Table 7. If V_{DD} is above the recommended operating conditions, V_{COS} remains at V_{DD} absolute max as defined in Table 7.

Figure 9 - Clock Overshoot and Undershoot Definition



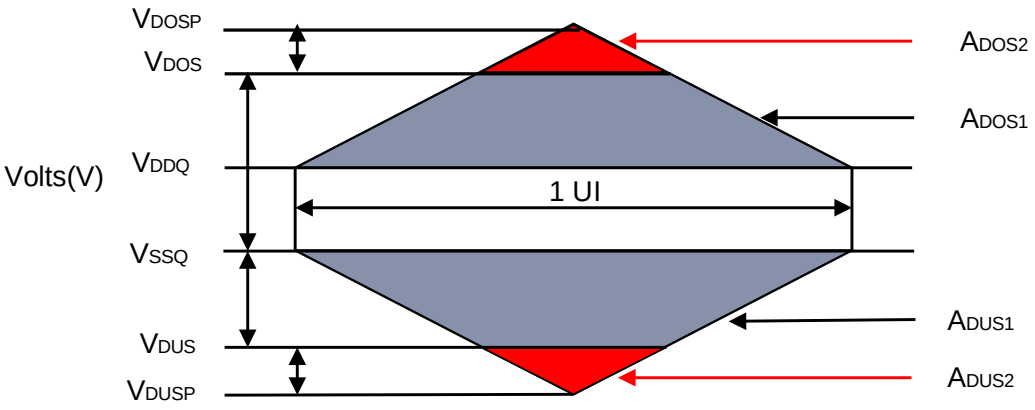
5.3.6 Data, Strobe and Mask Overshoot/Undershoot Specifications

Table 14 - AC Overshoot/Undershoot Specification for Data, Strobe and Mask

Parameter	Symbol	1600	1866	2133	2400	2666	2933	3200	Unit	Note
Maximum peak amplitude above V_{DOS}	V_{DOSP}	0.16							V	-
Upper boundary of overshoot area A_{DOS1}	V_{DOS}	V_{DD} + 0.24							V	1
Lower boundary of undershoot area A_{DUS1}	V_{DUS}	0.3							V	2
Maximum peak amplitude below V_{DUS}	V_{DUSP}	0.1							V	-
Maximum overshoot area per UI Above V_{DOS}	A_{DOS2}	0.0150	0.0129	0.0113	0.0100	0.0100	0.0100	0.0100	V-ns	-
Maximum overshoot area per 1 UI Between V_{DDQ} and V_{DOS}	A_{DOS1}	0.1050	0.0900	0.0788	0.0700	0.0700	0.0700	0.0700	V-ns	-
Maximum undershoot area per 1 UI Between V_{SSQ} and V_{DUS}	A_{DUS1}	0.1050	0.0900	0.0788	0.0700	0.0700	0.0700	0.0700	V-ns	-
Maximum undershoot area per 1 UI below V_{DUS}	A_{DUS2}	0.0150	0.0129	0.0113	0.0100	0.0100	0.0100	0.0100	V-ns	-
(DQ, DQS_t, DQS_c, DM_n, DBI_n, TDQS_t, TDQS_c)										

Note:
1. The value of V_{DOS} matches (V_{IN}, V_{OUT}) max as defined in Table 5 if V_{DDQ} equals V_{DDQ} max as defined Table 6. If V_{DDQ} is above the recommended operating conditions, V_{DOS} remains at (V_{IN}, V_{OUT}) max as defined in Table 5.
2. The value of V_{DUS} matches (V_{IN}, V_{OUT}) min as defined in Table 5.

Figure 10 - Data, Strobe and Mask Overshoot and Undershoot Definition



5.4 Slew Rate Definitions for Differential Input Signals

5.4.1 Slew Rate Definitions for Differential Input Signals

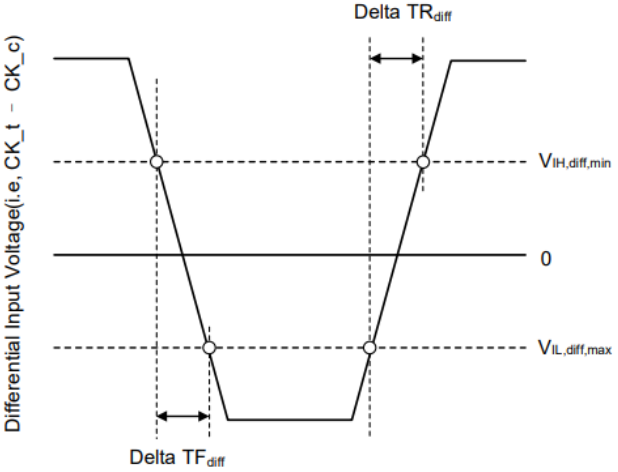
Input slew rate for differential signals (CK_t, CK_c) are defined and measured as shown in Table 156 and Figure 8.

Table 15 - CK Differential Input Slew Rate Definition

Description	From	To	Defined by
Differential input slew rate for rising edge (CK_t - CK_c)	$V_{IL,diff,max}$	$V_{IH,diff,min}$	[$V_{IH,diff,min}$ - $V_{IL,diff,max}$]/Delta TR_{diff}
Differential input slew rate for falling edge (CK_t - CK_c)	$V_{IH,diff,min}$	$V_{IL,diff,max}$	[$V_{IH,diff,min}$ - $V_{IL,diff,max}$]/Delta TF_{diff}

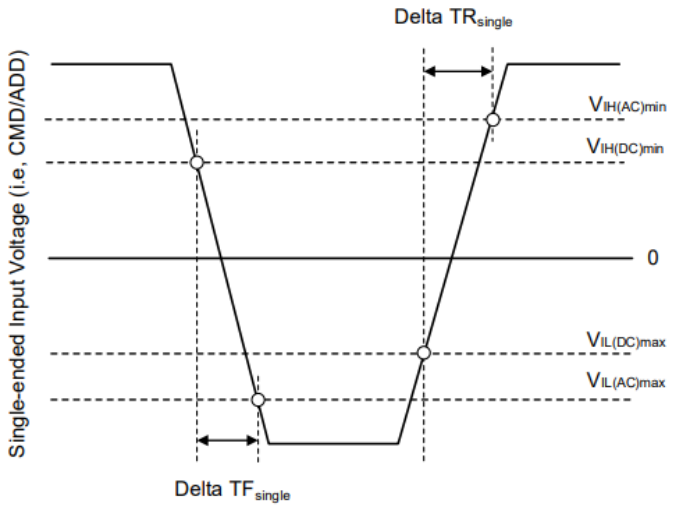
Note:
1. The differential signal (i, e., CK_t - CK_c) must be linear between these thresholds.

Figure 11 - Differential Input Slew Rate Definition for CK_t, CK_c



5.4.2 Slew Rate Definitions for Single-ended Input Signals (CMD/ADD)

Figure 12 - Single-ended Input Slew Rate Definition for CMD and ADD



Note:

1. Single-ended input slew rate for rising edge = {$V_{IH(AC)min}$ - $V_{IL(DC)max}$}/Delta TR_{single}.
2. Single-ended input slew rate for falling edge = {$V_{IH(DC)min}$ - $V_{IL(AC)max}$}/Delta TF_{single}.
3. Single-ended signal rising edge from $V_{IL(DC)max}$ to $V_{IH(DC)min}$ must be monotonic slope.
4. Single-ended signal falling edge from $V_{IH(DC)min}$ to $V_{IL(DC)max}$ must be monotonic slope.

5.5 CK Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock, each cross point voltage of differential input signals (CK_t, CK_c) must meet the requirements shown below. The differential input cross point voltage V_{IX} is measured from the actual cross point of true and complement signals to the midlevel between of V_{DD} and V_{SS}.

Figure 13 - VIX Definition (CK)

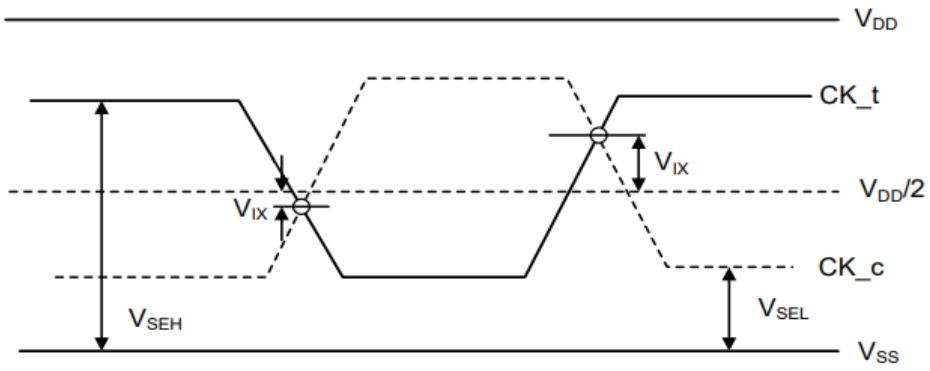


Table 16 - Cross Point Voltage for CK Differential Input Signals at DDR4-1666 through DDR4-2400

Symbol	Parameter	Input Level	DDR4 – 1666/1866/2133/2400	
			Min	Max
$V_{IX(CK)}$	Differential Input Cross Point Voltage relative to V_{DD}/2 for CK_t, CK_c	V_{SEH} > V_{DD}/2 + 145mV	-	120mV
		V_{DD}/2 + 100mV ≤ V_{SEH} ≤ V_{DD}/2 + 145mV	-	(V_{SEH} - V_{DD}/2) - 25mV
		V_{DD}/2 - 145mV ≤ V_{SEL} ≤ V_{DD}/2 – 100mV	- (V_{DD}/2 - V_{SEL}) + 25mV	-
		V_{SEL} < V_{DD}/2 - 145mV	-120mV	-

Table 17 - Cross Point Voltage for CK Differential Input Signals at DDR4-2666/2933/3200

Symbol	Parameter	Input Level	DDR4 – 2666/2933/3200	
			Min	Max
$V_{IX(CK)}$	Differential Input Cross Point Voltage relative to $V_{DD}/2$ for CK_t, CK_c	$V_{SEH} > V_{DD}/2 + 145$ mV	-	110mV
		$V_{DD}/2 + 100mV \le V_{SEH} \le V_{DD}/2 + 145$ mV	-	$(V_{SEH} - V_{DD}/2) - 30mV$
		$V_{DD}/2 - 145mV \le V_{SEL} \le V_{DD}/2 - 90mV$	$-(V_{DD}/2 - V_{SEL}) + 30mV$	-
		$V_{SEL} < V_{DD}/2 - 145mV$	-110mV	-

5.6 CMOS Rail to Rail Input Levels for RESET_n

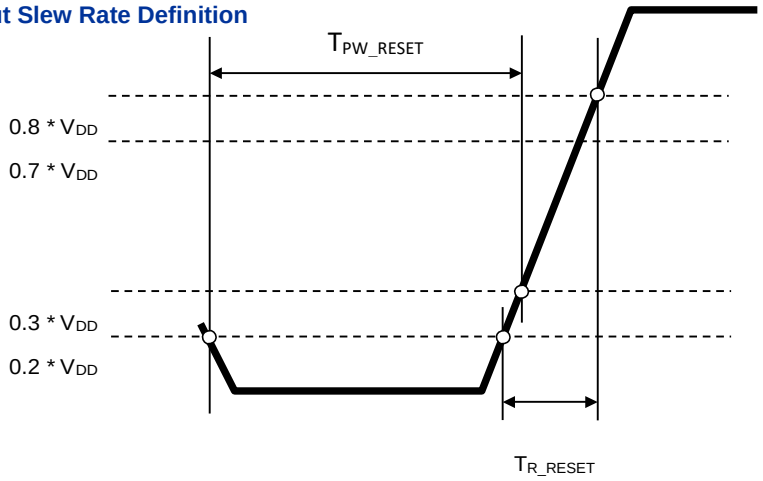
Table 18 - CMOS Rail to Rail Input Levels for RESET_n

Parameter	Symbol	Min	Max	Unit	Note
AC Input High Voltage	$V_{IH(AC)\_RESET}$	0.8 * V_{DD}	V_{DD}	V	6
DC Input High Voltage	$V_{IH(DC)\_RESET}$	0.7 * V_{DD}	V_{DD}	V	2
AC Input Low Voltage	$V_{IL(AC)\_RESET}$	V_{SS}	0.2 * V_{DD}	V	7
DC Input Low Voltage	$V_{IL(DC)\_RESET}$	V_{SS}	0.3 * V_{DD}	V	1
Rising Time	T_{R_RESET}	-	1.0	µs	4
RESET Pulse Width	T_{PW_RESET}	1.0	-	µs	3, 5

Note:

1. After RESET_n is registered LOW, RESET_n level shall be maintained below $V_{IL(DC)\_RESET}$ during T_{PW_RESET}, otherwise, the DRAM may not be reset.
2. Once RESET_n is registered HIGH, RESET_n level must be maintained above $V_{IH(DC)\_RESET}$, otherwise, the DRAM operation will not be guaranteed until it is reset asserting RESET_n signal LOW.
3. RESET is destructive to data contents.
4. No slope reversal (ringback) requirement during its level transition from LOW to HIGH.
5. This definition is applied only “Reset Procedure at Power Stable”.
6. Overshoot might occur. It should be limited by Absolute Maximum DC Ratings.
7. Undershoot might occur. It should be limited by Absolute Maximum DC Ratings.

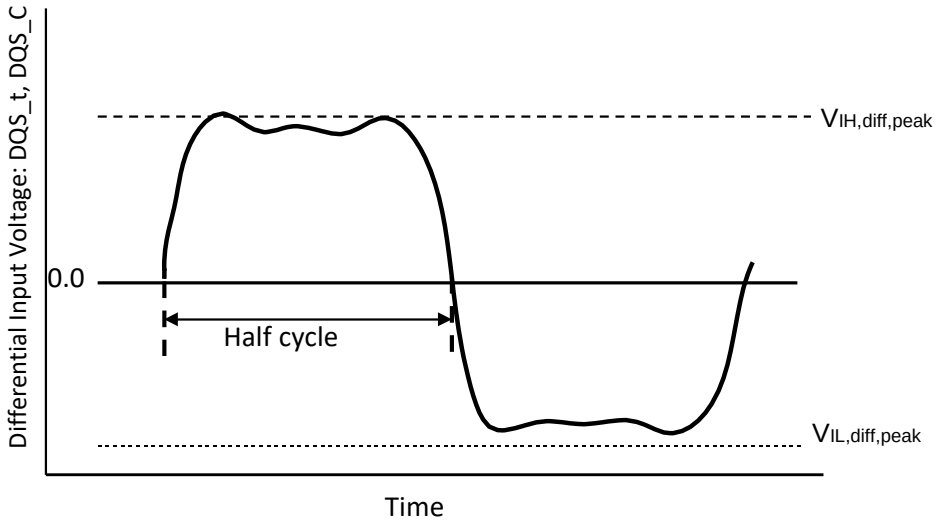
Figure 14 - RESET_n Input Slew Rate Definition



5.7 AC and DC Logic Input Levels for DQS Signals

5.7.1 Differential Signal Definition

Figure 15 - Definition of differential DQS Signal AC-swing Level



5.7.2 Differential Swing Requirements for DQS (DQS_t - DQS_c)

Table 19 - Differential Input Swing Requirements for DQS

Symbol	Parameter	1600/1866/2133		2400		2666		2999		3200		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
$V_{IH,diff,peak}$	$V_{IH,diff,peak}$ Voltage	186	Note 2	160	Note2	150	Note 2	145	Note 2	140	Note 2	mV	1
$V_{IL,diff,peak}$	$V_{IL,diff,peak}$ Voltage	Note 2	-186	Note 2	-160	Note 2	-150	Note 2	-145	Note 2	-140	mV	1

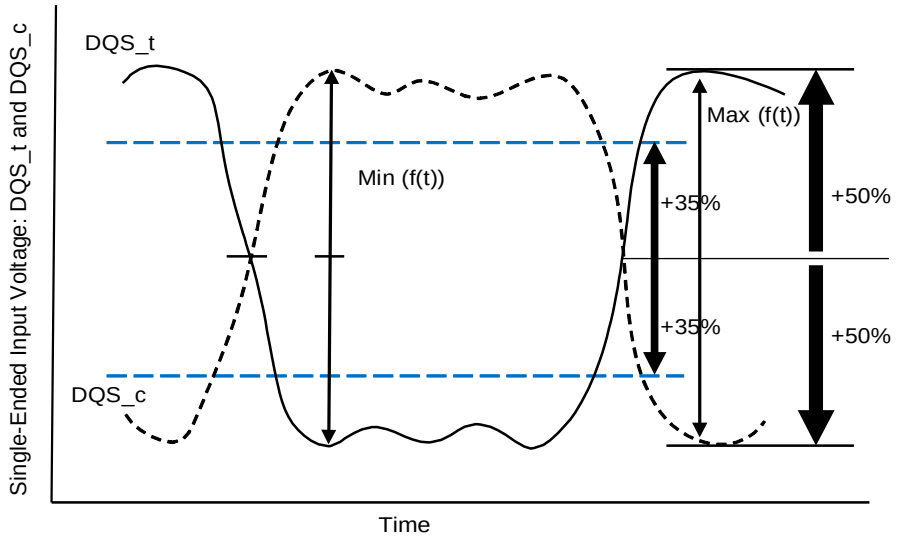
Note:

1. Used to define a differential signal slew-rate.
2. These values are not defined; however, the differential signals DQS_t - DQS_c, need to be within the respective limits of Overshoot, Undershoot Specification for single-ended signals.

5.7.3 Peak Voltage Calculation Method

The peak voltage of Differential DQS signals are calculated using following equations:
$V_{IH,diff,peak}$ Voltage = Max(f(t))
$V_{IL,diff,peak}$ Voltage = Min(f(t))
f(t) = V_{DQS_t} - V_{DQS_c}
The Max(f(t)) or Min(f(t)) used to determine the midpoint from which to reference the ± 35% window of the exempt non-monotonic signaling shall be the smallest peak voltage observed in all UI's.

Figure 16 - Definition of Differential DQS Peak Voltage and Range of Exempt Non-monotonic Signaling



5.7.4 Differential Input Cross Point Voltage

To achieve tight RxMask input requirements as well as output skew parameters with respect to strobe, the cross-point voltage of differential input signals (DQS_t, DQS_c) must meet the requirements in Table 20. The differential input cross point voltage V_{IX_DQS} ($V_{IX\_DQS,FR}$ and $V_{IX\_DQS,RF}$) is measured from the actual cross point of DQS_t, DQS_c relative to the $V_{DQS,mid}$ of the DQS_t and DQS_c signals.
$V_{DQS,mid}$ is the midpoint of the minimum levels achieved by the transitioning DQS_t and DQS_c signals, and noted by V_{DQS_trans}. V_{DQS_trans} is the difference between the lowest horizontal tangent above $V_{DQS,mid}$ of the transitioning DQS signals and the highest horizontal tangent below $V_{DQS,mid}$ of the transitioning DQS signals.
A non-monotonic transitioning signal's ledge is exempt or not used in determination of a horizontal tangent provided the said ledge occurs within ± 35% of the midpoint of either $V_{IH,diff,peak}$ Voltage (DQS_t rising) or $V_{IL,diff,peak}$ Voltage (DQS_c rising), refer to Figure 14.
A secondary horizontal tangent resulting from a ring-back transition is also exempt in determination of a horizontal tangent. That is, a falling transition's horizontal tangent is derived from its negative slope to zero slope transition (point A in Figure 14) and a ring-back's horizontal tangent derived from its positive slope to zero slope transition (point B in Figure 14) is not a valid horizontal tangent; and a rising transition's horizontal tangent is derived from its positive slope to zero slope transition (point C in Figure 14) and a ring-back's horizontal tangent derived from its negative slope to zero slope transition (point D in Figure 14) is not a valid horizontal tangent.

Figure 17 - VIX Definition (DQS)

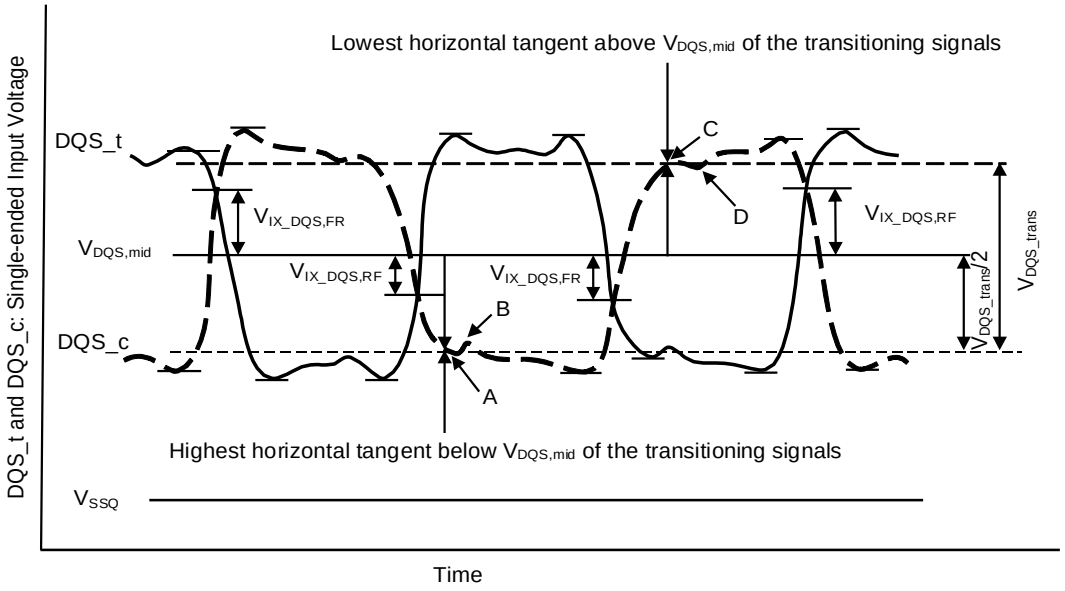


Table 20 - Cross Point Voltage for DQS Differential Input Signals

Symbol	Parameter	1600/1866/2133/2400/2666/2933/3200		Unit	Note
		Min	Max		
$V_{IX\_DQS,ratio}$	DQS_t and DQS_c crossing relative to the midpoint of the DQS_t and DQS_c signal swings	-	25	%	1,2
V_{DQS,mid_to_Vcent}	$V_{DQS,mid}$ offset relative to $V_{cent\_DQ(midpoint)}$	-	Note 3	mV	3,4,5

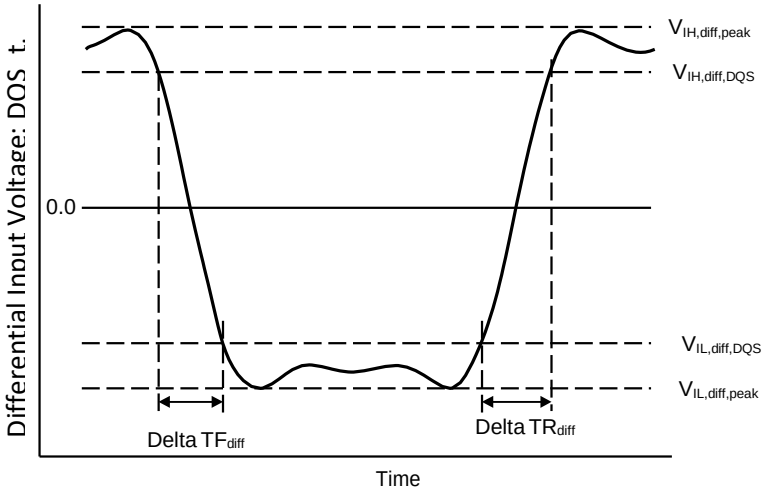
Note:

1. $V_{IX\_DQS,ratio}$ is DQS V_{IX} crossing ($V_{IX\_DQS,FR}$ or $V_{IX\_DQS,RF}$) divided by V_{DQS_trans}. V_{DQS_trans} is the difference between the lowest horizontal tangent above $V_{DQS,mid}$ of the transitioning DQS signals and the highest horizontal tangent below $V_{DQS,mid}$ of the transitioning DQS signals.
2. $V_{DQS,mid}$ will be similar to the V_{REFDQ} internal setting value obtained during V_{REF} Training if the DQS and DQs drivers and paths are matched.
3. The maximum limit shall not exceed the smaller of $V_{IH,diff,DQS}$ minimum limit or 50mV.
4. V_{IX} measurements are only applicable for transitioning DQS_t and DQS_c signals when toggling data, preamble and high-z states are not applicable conditions.
5. The parameter $V_{DQS,mid}$ is defined for simulation and ATE testing purposes, it is not expected to be tested in a system.

5.7.5 Differential Input Slew Rate Definition

Input slew rate for differential signals (DQS_t, DQS_c) are defined and measured as shown in Figure 15 and Table 21.

Figure 18 - Differential Input Slew Rate Definition for DQS_t, DQS



Note:

1. Differential signal rising edge from $V_{IL,diff,DQS}$ to $V_{IH,diff,DQS}$ must be monotonic slope.
2. Differential signal falling edge from $V_{IH,diff,DQS}$ to $V_{IL,diff,DQS}$ must be monotonic slope.

Table 21 - Differential Input Slew Rate Definition for DQS_t, DQS_c

Description	From	To	Defined by
Differential input slew rate for rising edge (DQS_t - DQS_c)	$V_{IL,diff,DQS}$	$V_{IH,diff,DQS}$	$\lvert V_{IL,diff,DQS} - V_{IH,diff,DQS}\rvert$/Delta TR_{diff}
Differential input slew rate for falling edge (DQS_t - DQS_c)	$V_{IH,diff,DQS}$	$V_{IL,diff,DQS}$	$\lvert V_{IL,diff,DQS} - V_{IH,diff,DQS}\rvert$/Delta TF_{diff}

Table 22 - Differential Input Level for DQS_t, DQS_c

Symbol	Parameter	1600/1866/2133		2400/2666		2999		3200		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
$V_{IH,diff,DQS}$	DC input logic high	136	-	130	-	115	-	110	-	mV
$V_{IL,diff,DQS}$	DC input logic low	-	-136	-	-130	-	-115	-	-110	mV

Table 23 - Differential Input Slew Rate for DQS_t, DQS_c

Symbol	Parameter	1600/1866/2133/2400		2666/2933/3200		Unit
		Min	Max	Min	Max	
SR_{Idiff}	Differential input slew rate	3	18	2.5	18	V/ns

6 AC And DC Output Measurement Levels

6.1 Output Driver DC Electronic Characteristics

The DDR4 driver supports two different R_{ON} values. These R_{ON} values are referred as strong (low R_{ON}) and weak mode (high R_{ON}). A functional representation of the output buffer is shown in Figure 16 below. Output driver impedance R_{ON} is defined as the individual pull-up and pull-down resistors (R_{ONPu} and R_{ONPd}).

$R_{ONPu} = \frac{V_{DDQ} - V_{OUT}}{|I_{OUT}|}$ under the condition that R_{ONPd} is off.

$R_{ONPd} = \frac{V_{OUT}}{|I_{OUT}|}$ under the condition that R_{ONPu} is off.

Figure 19 - Output Driver

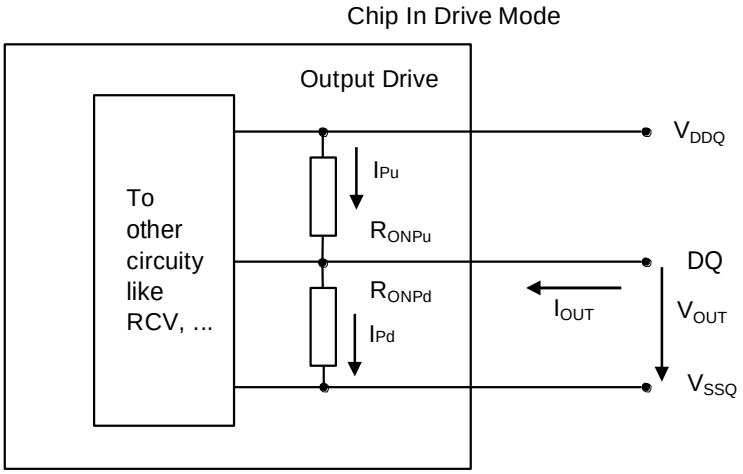


Table 24 - Output Driver DC Electronical Characteristics, Assuming R_{ZQ} = 240Ω; Entire Operating Temperature Range; after Proper ZQ Calibration

R_{ONnom}	Resistor	V_{OUT}	Min	Nom	Max	Unit	Note
34Ω	R_{ON34Pd}	$V_{OL(DC)}$ = 0.5 * V_{DDQ}	0.73	1.00	1.10	R_{ZQ}/7	1,2
		$V_{OM(DC)}$ = 0.8 * V_{DDQ}	0.83	1.00	1.10	R_{ZQ}/7	1,2
		$V_{OH(DC)}$ = 1.1 * V_{DDQ}	0.83	1.00	1.25	R_{ZQ}/7	1,2
	R_{ON34Pu}	$V_{OL(DC)}$ = 0.5 * V_{DDQ}	0.90	1.00	1.25	R_{ZQ}/7	1,2
		$V_{OM(DC)}$ = 0.8 * V_{DDQ}	0.90	1.00	1.10	R_{ZQ}/7	1,2
		$V_{OH(DC)}$ = 1.1 * V_{DDQ}	0.80	1.00	1.10	R_{ZQ}/7	1,2
48Ω	R_{ON48Pd}	$V_{OL(DC)}$ = 0.5 * V_{DDQ}	0.73	1.00	1.10	R_{ZQ}/5	1,2
		$V_{OM(DC)}$ = 0.8 * V_{DDQ}	0.83	1.00	1.10	R_{ZQ}/5	1,2
		$V_{OH(DC)}$ = 1.1 * V_{DDQ}	0.83	1.00	1.25	R_{ZQ}/5	1,2
	R_{ON48Pu}	$V_{OL(DC)}$ = 0.5 * V_{DDQ}	0.90	1.00	1.25	R_{ZQ}/5	1,2
		$V_{OM(DC)}$ = 0.8 * V_{DDQ}	0.90	1.00	1.10	R_{ZQ}/5	1,2
		$V_{OH(DC)}$ = 1.1 * V_{DDQ}	0.80	1.00	1.10	R_{ZQ}/5	1,2
Mismatch between pull-up and pull-down, MM_{PuPd}		$V_{OM(DC)}$ = 0.8 * V_{DDQ}	-10	-	17	%	1,2,3,4
Mismatch DQ-DQ within byte variation pull-up, MM_{Pudd}		$V_{OM(DC)}$ = 0.8 * V_{DDQ}	-	-	10	%	1,2,4
Mismatch DQ-DQ within byte variation pull-down, MM_{Pddd}		$V_{OM(DC)}$ = 0.8 * V_{DDQ}	-	-	10	%	1,2,4

Note:

1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
2. Pull-up and pull-down output driver impedances are recommended to be calibrated at 0.8 * V_{DDQ}. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.5 * V_{DDQ} and 1.1 * V_{DDQ}.
3. Measurement definition for mismatch between pull-up and pull-down, MM_{PuPd}: Measure R_{ONPu} and R_{ONPd} both at 0.8 * V_{DD} separately; R_{ONnom} is the nominal R_{ON} value.
   $MM_{PuPd} = [(R_{ONPu} - R_{ONPd})/R_{ONnom}] * 100$
4. R_{ON} variance range ratio to R_{ON} nominal value in a given component, including DQS_t and DQS_c. $MM_{Pudd} = [(R_{ONPu,max} - R_{ONPu,min})/R_{ONnom}] * 100$
   $MM_{Pddd} = [(R_{ONPd,max} - R_{ONPd,min})/R_{ONnom}] * 100$
5. This parameter of x16 device is specified for upper byte and lower byte.

6.1.1 Alert_n Output Driver Characteristic

A functional representation of the output buffer is shown in Figure 17. Output driver impedance R_{ON} is defined as follows:

$R_{ONPd} = \frac{V_{OUT}}{|I_{OUT}|}$ under the condition that R_{ONPu} is off.

Figure 20 - Functional Representation of the Output Buffer

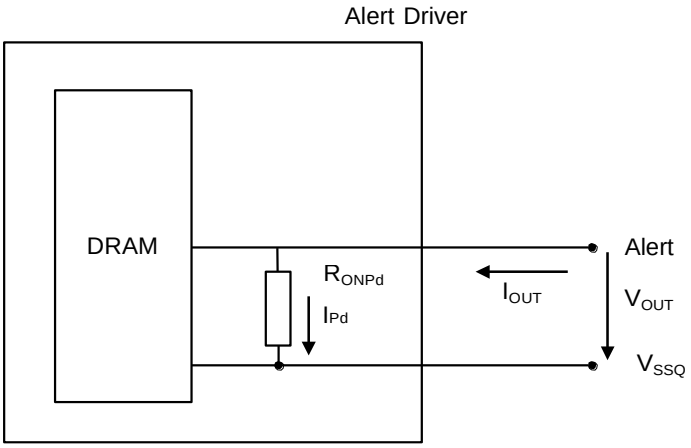


Table 25 - Output Driver Impedance

Resister	V_{OUT}	Min	Max	Unit	Note
R_{ONPd}	$V_{OL(DC)}$ = 0.1 * V_{DDQ}	0.3	1.2	34Ω	1
	$V_{OM(DC)}$ = 0.8 * V_{DDQ}	0.4	1.2	34Ω	1
	$V_{OH(DC)}$ = 1.1 * V_{DDQ}	0.4	1.4	34Ω	1

Note:

V_{DDQ} voltage is at $V_{DDQ(DC)}$. $V_{DDQ(DC)}$ definition is TBD.

6.1.2 Output Driver Characteristic of Connectivity Test (CT) Mode

Following output driver impedance R_{ON} will be applied Test Output Pin during Connectivity Test (CT) Mode. The individual pull-up and pull-down resistors (R_{ONPu_CT} and R_{ONPd_CT}) are defined as follows:

$R_{ONPu\_CT} = \frac{V_{DDQ} - V_{OUT}}{|I_{OUT}|}$ when R_{ONPd_CT} is off.

$R_{ONPd\_CT} = \frac{V_{OUT}}{|I_{OUT}|}$ when R_{ONPu_CT} is off.

Figure 21 - Output Driver

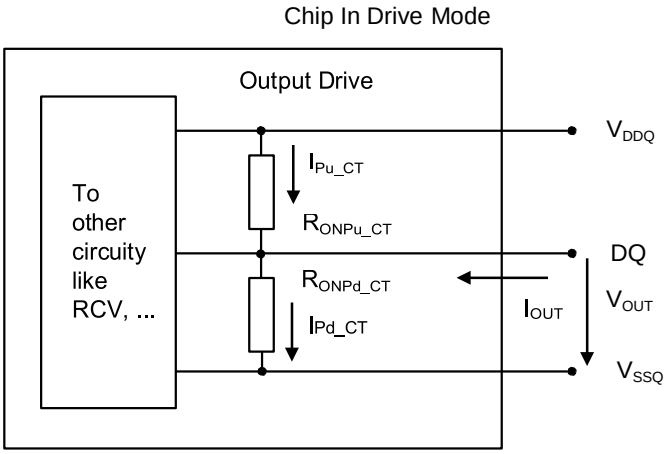


Table 26 - R_{ONPu_CT} and R_{ONPd_CT}

R_{ONnom_CT}	Resister	V_{OUT}	Max	Unit
34Ω	R_{ONPd_CT}	$V_{OB(DC)} = 0.2 * V_{DDQ}$	1.9	34Ω
		$V_{OL(DC)} = 0.5 * V_{DDQ}$	2.0	34Ω
		$V_{OM(DC)} = 0.8 * V_{DDQ}$	2.2	34Ω
		$V_{OH(DC)} = 1.1 * V_{DDQ}$	2.5	34Ω
	R_{ONPu_CT}	$V_{OB(DC)} = 0.2 * V_{DDQ}$	2.5	34Ω
		$V_{OL(DC)} = 0.5 * V_{DDQ}$	2.2	34Ω
		$V_{OM(DC)} = 0.8 * V_{DDQ}$	2.0	34Ω
		$V_{OH(DC)} = 1.1 * V_{DDQ}$	1.9	34Ω

Note:

Connectivity test mode uses un-calibrated drivers, showing the full range over PVT. No mismatch between pull up and pull down is defined.

6.2 Single-ended AC and DC Output Levels

Table 27 - Single-ended AC and DC Output Levels

Symbol	Parameter	DDR4-1600 to DDR4-3200	Unit
$V_{OH(DC)}$	DC output high measurement level (for IV curve linearity)	1.1 * V_{DDQ}	V
$V_{OM(DC)}$	DC output mid measurement level (for IV curve linearity)	0.8 * V_{DDQ}	V
$V_{OL(DC)}$	DC output low measurement level (for IV curve linearity)	0.5 * V_{DDQ}	V
$V_{OH(AC)}$	AC output high measurement level (for output SR)	(0.7 + 0.15) * V_{DDQ}	V
$V_{OL(AC)}$	AC output low measurement level (for output SR)	(0.7 - 0.15) * V_{DDQ}	V

Note:

The swing of ± 0.15 * V_{DDQ} is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of $R_{ZQ}/7$ and an effective test load of 50Ω to $V_{TT} = V_{DDQ}$.

6.3 Differential AC&DC Output Levels

Table 28 - Differential AC&DC Output Levels

Symbol	Parameter	DDR4-1600 to DDR4-3200	Unit
$V_{OH,diff(AC)}$	AC differential output high measurement level (for output SR)	+0.3 * V_{DDQ}	V
$V_{OL,diff(AC)}$	AC differential output low measurement level (for output SR)	-0.3 * V_{DDQ}	V

Note:

The swing of ± 0.3 * V_{DDQ} is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of $R_{ZQ}/7$ and an effective test load of 50Ω to $V_{TT} = V_{DDQ}$ at each of the differential outputs.

6.4 Single-ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$ for single-ended signals as shown in Table 29 and Figure 19.

Table 29 - Single-ended Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Single-ended output slew rate for rising edge	$V_{OL(AC)}$	$V_{OH(AC)}$	$[V_{OH(AC)} - V_{OL(AC)}]$/Delta TR_{se}
Single-ended output slew rate for falling edge	$V_{OH(AC)}$	$V_{OL(AC)}$	$[V_{OH(AC)} - V_{OL(AC)}]$/Delta TF_{se}

Note:

Output slew rate is verified by designed and characterization, and may not be subject to production test.

Figure 22 - Single-ended Output Slew Rate Definition

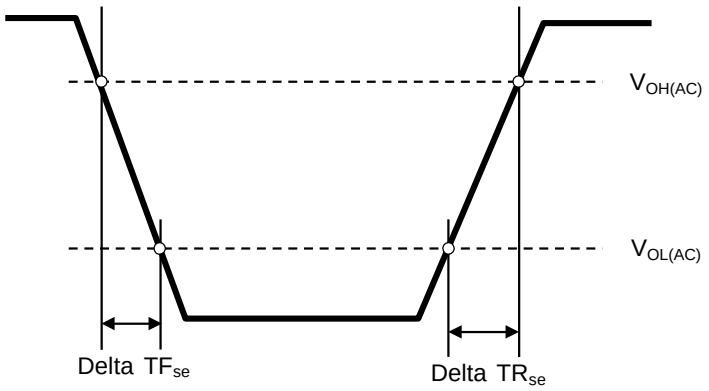


Table 30 - Single-ended Output Slew Rate

Parameter	Symbol	DDR4-1600 to DDR4-3200		Unit
		Min	Max	
Single-ended output slew rate	SRQse	4	9	V/ns

Description:
SR: Slew Rate; Q: Query Output (like in DQ, which stands for Data-in, Query-Output) se: Single-ended Singnals; For $R_{ON} = R_{ZQ}/7$ setting.

Note:

In two cases, a maximum slew rate of 12V/ns applies for a single DQ signal within a byte lane.

- Case 1 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from HIGH to LOW or LOW to HIGH) while all remaining DQ signals in the same byte lane are static (i.e. they stay at either HIGH or LOW).
- Case 2 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from HIGH to LOW or LOW to HIGH) while all remaining DQ signals in the same byte lane are switching into the opposite direction (i.e. from LOW to HIGH or HIGH to LOW respectively). For the remaining DQ signal switching into the opposite direction, the regular maximum limit of 9V/ns applies.

6.5 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OLdiff(AC)}$ and $V_{OHdiff(AC)}$ for differential signals as shown in Table 31 and Figure 20.

Table 31 - Differential Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	$V_{OL,diff(AC)}$	$V_{OH,diff(AC)}$	$[V_{OH,diff(AC)} - V_{OL,diff(AC)}]$/Delta TR_{diff}
Differential output slew rate for falling edge	$V_{OH,diff(AC)}$	$V_{OL,diff(AC)}$	$[V_{OH,diff(AC)} - V_{OL,diff(AC)}]$/Delta TF_{diff}

Note:

1. Output slew rate is verified by design and characterization, and may not be subject to production test.

Figure 23 - Differential Output Slew Rate Definition

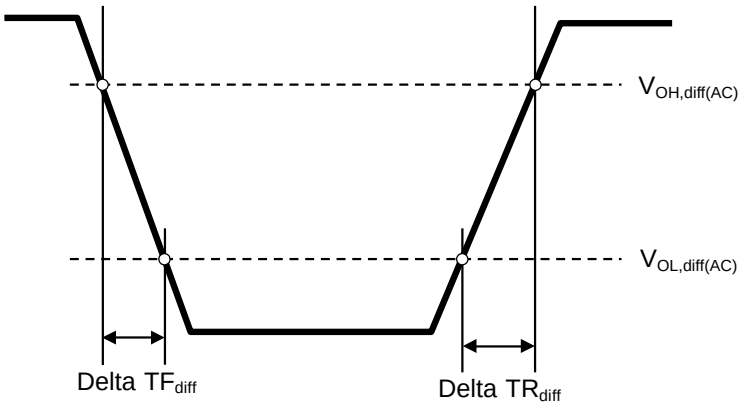


Table 32 - Differential Output Slew Rate

Parameter	Symbol	DDR4-1600 to DDR4-3200		Unit
		Min	Max	
Differential output slew rate	SRQ_{diff}	8	18	V/ns

Description:

SR: Slew Rate; Q: Query Output (like in DQ, which stands for Data-in, Query-Output);

Diff: Differential Singnals; For $R_{ON} = R_{ZQ}/7$ setting.

6.6 Single-ended AC& DC Output Levels of Connectivity Test Mode

Following output parameters will be applied for DDR4 SDRAM Output Signal during Connectivity Test Mode.

Table 33 - Single-ended AC&DC Output Level of Connectivity Test Mode

Symbol	Parameter	DDR4-1600 to DDR4-3200	Unit	Note
$V_{OH(DC)}$	DC output high measurement level (for IV curve linearity)	1.1 * V_{DDQ}	V	-
$V_{OM(DC)}$	DC output mid measurement level (for IV curve linearity)	0.8 * V_{DDQ}	V	-
$V_{OL(DC)}$	DC output low measurement level (for IV curve linearity)	0.5 * V_{DDQ}	V	-
$V_{OB(DC)}$	DC output below measurement level (for IV curve linearity)	0.2 * V_{DDQ}	V	-
$V_{OH(AC)}$	AC output high measurement level (for output SR)	V_{TT} + (0.1 * V_{DDQ})	V	1
$V_{OL(AC)}$	AC output below measurement level (for output SR)	V_{TT} - (0.1 * V_{DDQ})	V	1

Note:

1. The effective test load is 50Ω terminated by V_{TT} = 0.5 * V_{DDQ}.

Figure 24 - Output Slew Rate Definition of Connectivity Test Mode

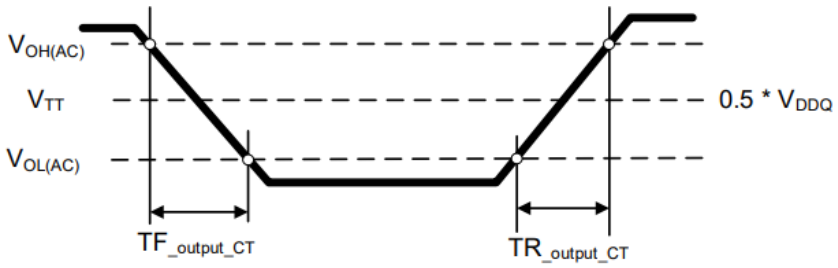


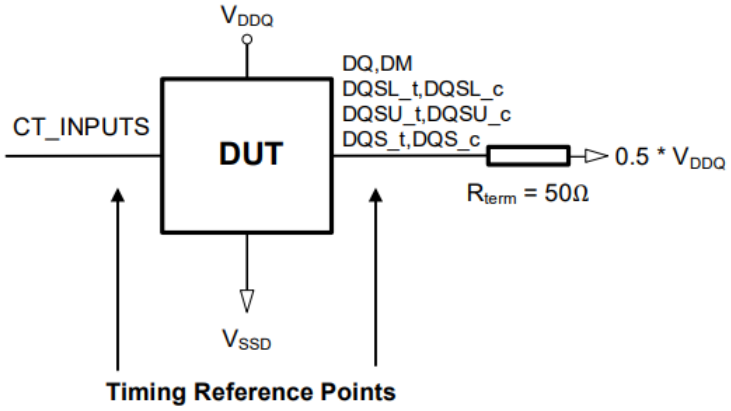
Table 34 - Single-ended Output Slew Rate of Connectivity Test Mode

Parameter	Symbol	DDR4-1600 to DDR4-3200		Unit
		Min	Max	
Output signal Falling time	$TF_{\_output\_CT}$	-	10	ns/V
Output signal Rising time	$TR_{\_output\_CT}$	-	10	ns/V

6.7 Reference Load for Connectivity Test Mode Timing

The reference load for ODT timings is defined in Figure 22.

Figure 25 - Connectivity Test Mode Timing Reference Load



7 Speed Bin

7.1 DDR4-2400 Speed Bins and Operations

Table 35 - DDR4-2400 Speed Bins and Operations

Speed Bin				DDR4-2400		Unit	Note
CL-nRCD-nRP				17-17-17			
Parameter			Symbol	Min	Max		
Internal READ command to first data			t_{AA}	14.16 (13.75)(9)	18.00	ns	9
Internal READ command to first data with Read DBI enabled			t_{AA_DBI}	$t_{AA\ (min)}$ + 3nCK	$t_{AA\ (max)}$ + 3nCK	ns	9
ACT to internal READ or WRITE delay time			t_{RCD}	14.16 (13.75)(9)	-	ns	9
PRE command period			t_{RP}	14.16 (13.75)(9)	-	ns	9
ACT to PRE command period			t_{RAS}	32	9 * t_{REFI}	ns	9
ACT to ACT or REF command period			t_{RC}	46.16 (45.75)(9)	-	ns	9
	Normal	READ DBI					
CWL = 9	CL = 9	CL = 11	$t_{CK\ (avg)}$	Reserved		ns	1,2,3,4,5,8
	CL = 10	CL = 12	$t_{CK\ (avg)}$	1.5	1.6	ns	1,2,3,4,5,8
CWL = 9,11	CL = 10	CL = 12	$t_{CK\ (avg)}$	Reserved		ns	4
	CL = 11	CL = 13	$t_{CK\ (avg)}$	1.25	<1.5	ns	1,2,3,4,5
	CL = 12	CL = 14	$t_{CK\ (avg)}$	1.25	<1.5	ns	1,2,3,5
CWL = 10,12	CL = 12	CL = 14	$t_{CK\ (avg)}$	Reserved		ns	4
	CL = 13	CL = 15	$t_{CK\ (avg)}$	1.071	<1.25	ns	1,2,3,4,5
	CL = 14	CL = 16	$t_{CK\ (avg)}$	1.071	<1.25	ns	1,2,3,5
CWL = 11,14	CL = 14	CL = 17	$t_{CK\ (avg)}$	Reserved		ns	4
	CL = 15	CL = 18	$t_{CK\ (avg)}$	0.937	<1.071	ns	1,2,3,4,5
	CL = 16	CL = 19	$t_{CK\ (avg)}$	0.937	<1.071	ns	1,2,3,5
CWL = 12,16	CL = 15	CL = 18	$t_{CK\ (avg)}$	Reserved		ns	1,2,3,4
	CL = 16	CL = 19	$t_{CK\ (avg)}$	Reserved		ns	1,2,3,4
	CL = 17	CL = 20	$t_{CK\ (avg)}$	0.833	<0.937	ns	1,2,3,4
	CL = 18	CL = 21	$t_{CK\ (avg)}$	0.833	<0.937	ns	1,2,3
Supported CL Settings				10,(11),12,(13),14,(15),16,17,18		nCK	10
Supported CL Settings with READ DBI				12,(13),14,(15),16,(18),19,20,21		nCK	10
Supported CWL Settings				9, 10, 11, 12, 14, 16		nCK	-

7.2 DDR4-2666 Speed Bins and Operations

Table 36 - DDR4-2666 Speed Bins and Operations

Speed Bin				DDR4-2666		Unit	Note
CL-nRCD-nRP				19-19-19			
Parameter			Symbol	Min	Max		
Internal READ command to first data			t_{AA}	14.25 (13.75)(9)	18.00	ns	9
Internal READ command to first data with Read DBI enabled			t_{AA_DBI}	$t_{AA\ (min)}$ + 3nCK	$t_{AA\ (max)}$ + 3nCK	ns	9
ACT to internal READ or WRITE delay time			t_{RCD}	14.25 (13.75)(9)	-	ns	9
PRE command period			t_{RP}	14.25 (13.75)(9)	-	ns	9
ACT to PRE command period			t_{RAS}	32	9 * t_{REFI}	ns	9
ACT to ACT or REF command period			t_{RC}	46.25 (13.75)(9)	-	ns	9
	Normal	READ DBI					
CWL = 9	CL = 9	CL = 11	$t_{CK\ (avg)}$	Reserved		ns	1,2,3,4,6,8
	CL = 10	CL = 12	$t_{CK\ (avg)}$	1.5	1.6	ns	1,2,3,6,8
CWL = 9,11	CL = 10	CL = 12	$t_{CK\ (avg)}$	Reserved		ns	4
	CL = 11	CL = 13	$t_{CK\ (avg)}$	1.25	<1.5	ns	1,2,3,4,6
	CL = 12	CL = 14	$t_{CK\ (avg)}$	1.25	<1.5	ns	1,2,3,6
CWL=10,12	CL = 12	CL = 14	$t_{CK\ (avg)}$	Reserved		ns	4
	CL = 13	CL = 15	$t_{CK\ (avg)}$	1.071	<1.25	ns	1,2,3,4,6
	CL = 14	CL = 16	$t_{CK\ (avg)}$	1.071	<1.25	ns	1,2,3,6
CWL= 11,14	CL = 14	CL = 17	$t_{CK\ (avg)}$	Reserved		ns	4
	CL = 15	CL = 18	$t_{CK\ (avg)}$	0.937	<1.071	ns	1,2,3,4,6
	CL = 16	CL = 19	$t_{CK\ (avg)}$	0.937	<1.071	ns	1,2,3,6
CWL=12,16	CL = 15	CL = 18	$t_{CK\ (avg)}$	Reserved		ns	4
	CL = 16	CL = 19	$t_{CK\ (avg)}$	Reserved		ns	1,2,3,4,6
	CL = 17	CL = 20	$t_{CK\ (avg)}$	0.833	<0.937	ns	1,2,3,4,6
	CL = 18	CL = 21	$t_{CK\ (avg)}$	0.833	<0.937	ns	1,2,3,6
CWL=14,18	CL = 17	CL = 20	$t_{CK\ (avg)}$	Reserved		ns	1,2,3,4
	CL = 18	CL = 21	$t_{CK\ (avg)}$	Reserved		ns	1,2,3,4
	CL = 19	CL = 22	$t_{CK\ (avg)}$	0.75	<0.833	ns	1,2,3,4
	CL = 20	CL = 23	$t_{CK\ (avg)}$	0.75	<0.833	ns	1,2,3
Supported CL Settings				10,(11),12,(13),14,(15),16,(17),18,19,20		nCK	10
Supported CL Settings with READ DBI				12,(13),14,(15),16,(18),19,(20),21,22,23		nCK	10
Supported CWL Settings				9,10,11,12,14,16,18		nCK	-

7.3 DDR4-3200 Speed Bins and Operations

Table 37 - DDR4-3200 Speed Bins and Operations

Speed Bin			DDR4-3200		Unit	Note
CL-nRCD-nRP			22-22-22			
Parameter		Symbol	Min	Max		
Internal READ command to first data		t_{AA}	13.75	18.00	ns	9
Internal READ command to first data with READ DBI enabled		t_{AA_DBI}	$t_{AA\ (min)}$ + 4nCK	$t_{AA\ (max)}$ + 4nCK	ns	9
ACT to internal Read or Write delay time		t_{RCD}	13.75	-	ns	9
PRE command period		t_{RP}	13.75	-	ns	9
ACT to PRE command period		t_{RAS}	32	9 * tREFI	ns	9
ACT to ACT or REF command period		t_{RC}	45.75	-	ns	9
	Normal	Read DBI				
CWL = 9	CL = 9	CL = 11	$t_{CK\ (avg)}$	Reserved	ns	1,2,3,4,7,8
	CL = 10	CL = 12	$t_{CK\ (avg)}$	1.5 1.6	ns	1,2,3,7,8
CWL = 9,11	CL = 10	CL = 12	$t_{CK\ (avg)}$	Reserved	ns	4
	CL = 11	CL = 13	$t_{CK\ (avg)}$	1.25 <1.5	ns	1,2,3,4,7
	CL = 12	CL = 14	$t_{CK\ (avg)}$	1.25 <1.5	ns	1,2,3,7
CWL=10,12	CL = 12	CL = 14	$t_{CK\ (avg)}$	Reserved	ns	4
	CL = 13	CL = 15	$t_{CK\ (avg)}$	1.071 <1.25	ns	1,2,3,4,7
	CL = 14	CL = 16	$t_{CK\ (avg)}$	1.071 <1.25	ns	1,2,3,7
CWL=11,14	CL = 14	CL = 17	$t_{CK\ (avg)}$	Reserved	ns	4
	CL = 15	CL = 18	$t_{CK\ (avg)}$	0.937 <1.071	ns	1,2,3,4,7
	CL = 16	CL = 19	$t_{CK\ (avg)}$	0.937 <1.071	ns	1,2,3,7
CWL=12,16	CL = 15	CL = 18	$t_{CK\ (avg)}$	Reserved	ns	4
	CL = 16	CL = 19	$t_{CK\ (avg)}$	Reserved	ns	1,2,3,4,7
	CL = 17	CL = 20	$t_{CK\ (avg)}$	0.833 <0.937	ns	1,2,3,4,7
	CL = 18	CL = 21	$t_{CK\ (avg)}$	0.833 <0.937	ns	1,2,3,7
CWL=14,18	CL = 17	CL = 20	$t_{CK\ (avg)}$	Reserved	ns	1,2,3,4
	CL = 18	CL = 21	$t_{CK\ (avg)}$	Reserved	ns	1,2,3,4
	CL = 19	CL = 22	$t_{CK\ (avg)}$	0.75 <0.833	ns	1,2,3,4
	CL = 20	CL = 23	$t_{CK\ (avg)}$	0.75 <0.833	ns	1,2,3
CWL=16,20	CL = 20	CL = 24	$t_{CK\ (avg)}$	Reserved	ns	1,2,3,4,7
	CL = 21	CL = 25	$t_{CK\ (avg)}$	0.682 <0.75	ns	1,2,3,4,7
	CL = 22	CL = 26	$t_{CK\ (avg)}$	0.682 <0.75	ns	1,2,3,7
	CL = 24	CL = 28	$t_{CK\ (avg)}$	0.682 <0.75	ns	1,2,3,7
CWL=16,20	CL = 20	CL = 24	$t_{CK\ (avg)}$	Reserved	ns	1,2,3,4
	CL = 22	CL = 26	$t_{CK\ (avg)}$	0.625 <0.682	ns	1,2,3,4
	CL = 24	CL = 28	$t_{CK\ (avg)}$	0.625 <0.682	ns	1,2,3
Supported CL Settings			10,11,12,13,14,15,16,17,18,19,20,22, 24		nCK	-
Supported CL Settings with READ DBI			12,13,14,15,16,18,19,20,21,22,23,24, 26,28		nCK	-
Supported CWL Settings			9,10,11,12,14,16,18,20		nCK	-

7.4 Speed Bin Table Note

Absolute Specifications

- V_{DDQ} = V_{DD} = 1.20V ± 0.06V
- V_{PP} = 2.5V (2.375V min, 2.75V max)
- The values defined with above-mentioned table are DLL ON case.
- DDR4-2400, 2666, 2933 and 3200 Speed Bin Tables are valid only when gear down mode is disabled.

1. The CL setting and CWL setting result in $t_{CK\ (avg)min}$ and $t_{CK\ (avg)max}$ requirements. When selecting $t_{CK\ (avg)}$, both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. $t_{CK\ (avg)min}$ limits: Since CAS latency is not purely analog - data and strobe output are synchronized by the DLL-all possible intermediate frequencies may not be guaranteed. CL in clock cycle is calculated from t_{AA} following rounding algorithm defined in JEDEC-79D Section 13.5.
3. $t_{CK\ (avg)max}$ limits: Calculate $t_{CK\ (avg)}$ = $t_{AA\ (max)}$/CL SELECTED and round the resulting $t_{CK\ (avg)}$ down to the next valid speed bin (i.e. 1.5ns or 1.25ns or 1.071ns or 0.937ns or 0.833ns). This result is $t_{CK\ (avg)max}$ corresponding to CL SELECTED.
4. 'Reserved' settings are not allowed. User must program a different value.
5. Any DDR4-2400 speed bin also supports functional operation at lower frequencies as shown in the corresponding table which are not subject to production tests but verified by design/characterization.
6. Any DDR4-2666 speed bin also supports functional operation at lower frequencies as shown in the corresponding table which are not subject to production tests but verified by design/characterization.
7. Any DDR4-3200 speed bin also supports functional operation at lower frequencies as shown in the corresponding table which are not subject to production tests but verified by design/characterization.
8. DDR4-1600 AC timing apply if DRAM operates at lower than 1600MT/s data rate.
9. Parameters apply from $t_{CK\ (avg)min}$ to $t_{CK\ (avg)max}$ at all standard JEDEC clock period values as stated in the Speed Bin Tables.
10. CL number in parentheses, it means that these numbers are optional.
11. DDR4 SDRAM supports CL = 9 as long as a system meets $t_{AA\ (min)}$, $t_{RCD\ (min)}$, $t_{RP\ (min)}$, and $t_{RC\ (min)}$.
12. Each speed bin lists the timing requirements that need to be supported in order for a given DRAM to be JEDEC compliant. JEDEC compliance does not require support for all speed bins within a given speed. JEDEC compliance requires meeting the parameters for a least one of the listed speed bins.

7.5 t_{REFI} and t_{RFC} Parameters

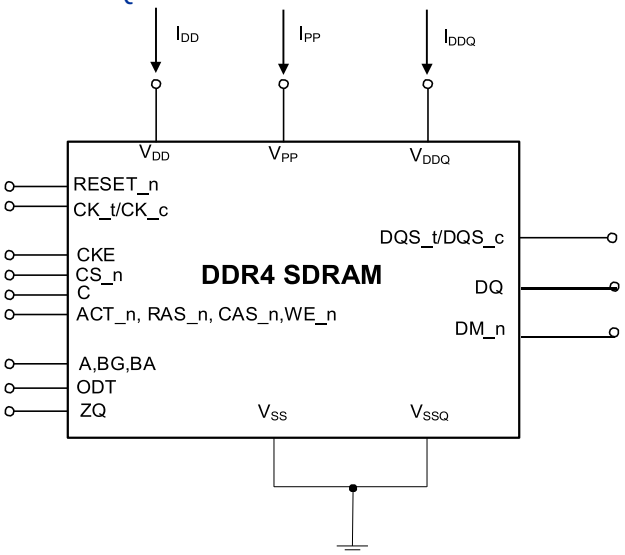
In the Fixed 1x Refresh rate mode, only REF1x commands are permitted. In the Fixed 2x Refresh rate mode, only REF2x commands are permitted. In the Fixed 4x Refresh rate mode, only REF4x commands are permitted. When the on-the-fly 1x/2x Refresh rate mode is enabled, both REF1x and REF2x commands are permitted. When the on-the-fly 1x/4x Refresh rate mode is enabled, both REF1x and REF4x commands are permitted.

Table 38 - t_{REFI} and t_{RFC} Parameters

Refresh Mode	Parameter		8Gb	Unit
	$t_{REFI(base)}$		7.8	µs
1x mode	t_{REFI1}	-40°C ≤ T_{CASE} ≤ 85°C	$t_{REFI(base)}$	µs
		85°C < T_{CASE} ≤ 95°C	$t_{REFI(base)}$/2	µs
	$t_{RFC1\ (min)}$		350	ns
2x mode	t_{REFI2}	-40°C ≤ T_{CASE} ≤ 85°C	$t_{REFI(base)}$/2	µs
		85°C < T_{CASE} ≤ 95°C	$t_{REFI(base)}$/4	µs
	$t_{RFC2\ (min)}$		260	ns
4x mode	t_{REFI4}	-40°C ≤ T_{CASE} ≤ 85°C	$t_{REFI(base)}$/4	µs
		85°C < T_{CASE} ≤ 95°C	$t_{REFI(base)}$/8	µs
	$t_{RFC4\ (min)}$		160	ns

8 IDD And IDDQ Specification Parameters And TestConditions

8.1 I_{DD}, I_{PP} and I_{DDQ} Measurement Conditions



Note:

DIMM level Output test load condition may be different from above

Figure 26 - Correlation from Simulated Channel I/O Power to Actual Channel I/O Power Supported by IDDQ Measurement

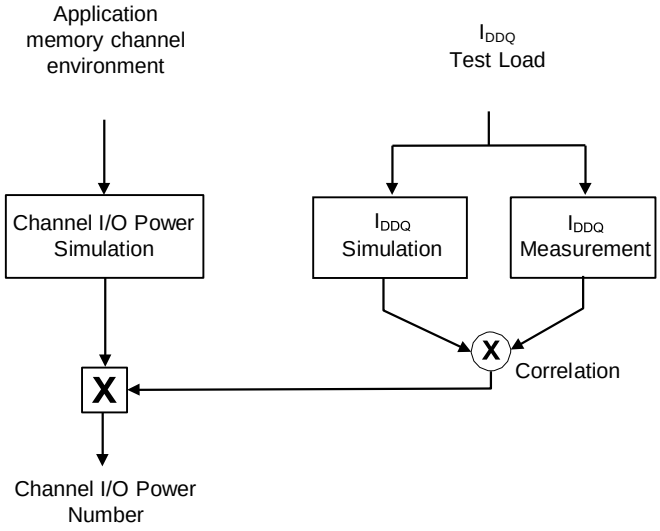


Table 39 - Timings used for I_{DD}, I_{PP} and I_{DDQ} Measurement-Loop Patterns

Symbol		DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit
		11-11-11	13-13-13	15-15-15	17-17-17	19-19-19	21-21-21	22-22-22	
t_{CK}		1.25	1.071	0.937	0.833	0.75	0.682	0.625	ns
CL		11	13	15	17	19	21	22	nCK
CWL		11	12	14	16	18	20	20	nCK
nRCD		11	13	15	17	19	21	22	nCK
nRC		39	45	51	56	62	68	74	nCK
nRAS		28	32	36	39	43	47	52	nCK
nRP		11	13	15	17	19	21	22	nCK
nFAW	x8	20	22	23	26	28	31	34	nCK
	x16	28	28	32	36	40	44	48	nCK
nRRDS	x8	4	4	4	4	4	4	4	nCK
	x16	5	5	6	7	8	8	9	nCK
nRRDL	x8	5	5	6	6	7	8	8	nCK
	x16	6	6	7	8	9	10	11	nCK
t_{CCD_S}		4	4	4	4	4	4	4	nCK
t_{CCD_L}		5	5	6	6	7	8	8	nCK
t_{WTR_S}		2	3	3	3	4	4	4	nCK
t_{WTR_L}		6	7	8	9	10	11	12	nCK
nRFC 2Gb		128	150	171	193	214	235	256	nCK
nRFC 4Gb		208	243	278	313	347	382	416	nCK
nRFC 8Gb		280	327	374	421	467	514	560	nCK

Table 40 - Basic I_{DD}, I_{PP} and I_{DDQ} Measurement Conditions

Symbol	Description
I_{DD0}	**Operating One Bank Active-Precharge Current (AL = 0) CKE:** HIGH; **External clock:** On; **t_{CK}, nRC, nRAS, nRCD, CL:** See Table 38; **BL:** 8(1); **AL:** 0; **CS_n:** HIGH between ACT and PRE; **Command, Address, Bank Group Address, Bank Address Inputs:** Partially toggling according to Table 41. **Data I/O:** V_{DDQ}; **DM_n:** Stable at 1; **Bank Activity:** Cycling with one bank active at a time: 0, 0, 1, 1, 2, 2, ... (see Table 41); **Output Buffer and R_{TT}:** Enabled in Mode Registers[2]; **ODT Signal:** Stable at 0; **Pattern Details:** See Table 41.
I_{DD0A}	**Operating One Bank Active-Precharge Current (AL = CL - 1)** **AL = CL - 1, Other conditions:** See I_{DD0}.
I_{PP0}	**Operating One Bank Active-Precharge I_{PP} Current (AL = 0)** Same condition with I_{DD0}.
I_{DD1}	**Operating One Bank Active-Read-Precharge Current (AL = 0) CKE:** HIGH; **External clock:** On; **t_{CK}, nRC, nRAS, nRCD, CL:** See Table 39; **BL:** 8(1); **AL:** 0; **CS_n**: HIGH between ACT, RD and PRE; **Command, Address, Bank Group Address, Bank Address Inputs, Data IO:** Partially toggling according to Table 42. **DM_n:** stable at 1; **Bank Activity:** Cycling with one bank active at a time: 0, 0, 1, 1, 2, 2, ... (see Table 42); **Output Buffer and R_{TT}:** Enabled in Mode Registers[2]; **ODT Signal:** Stable at 0; **Pattern Details:** See Table 42
I_{DD1A}	**Operating One Bank Active-Read-Precharge Current (AL = CL - 1) AL = CL - 1, Other conditions**: See I_{DD1}.
I_{PP1}	**Operating One Bank Active-Read-Precharge I_{PP} Current** Same condition with I_{DD1}.
I_{DD2N}	**Precharge Standby Current (AL = 0) CKE:** HIGH; **External clock:** On; **t_{CK}, CL:** See Table 39; **BL:** 8(1); **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** Partially toggling according to Table 43. **Data I/O:** V_{DDQ}; **DM_n:** Stable at 1; **Bank Activity:** All banks closed; **Output Buffer and R_{TT}:** Enabled in Mode Registers[2]; **ODT Signal:** Stable at 0; **Pattern Details:** See Table 43.
I_{DD2NA}	**Precharge Standby Current (AL = CL - 1) AL = CL - 1, Other conditions:** See I_{DD2N}.
I_{PP2N}	**Precharge Standby I_{PP} Current** Same condition with I_{DD2N}.

Symbol	Description
I_{DD2NT}	**Precharge Standby ODT Current CKE:** HIGH; **External clock:** On; **t_{CK}, CL:** See Table 39; **BL:** 8(1); **AL:** 0; **CS_n**: Stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** Partially toggling according to Table 44. **Data I/O:** V_{SSQ}; **DM_n:** Stable at 1; **Bank Activity:** All banks closed; **Output Buffer and R_{TT}:** Enabled in Mode Registers(2); **ODT Signal:** Toggling according to Table 44; **Pattern Details:** See Table 44.
I_{DDQ2NT}	**Precharge Standby ODT I_{DDQ} Current** Same definition like for I_{DD2NT}, however measuring I_{DDQ} current instead of I_{DD} current.
I_{DD2NL}	**Precharge Standby Current with CAL enabled** Same definition like for I_{DD2N}, CAL enabled(3), (5).
I_{DD2NG}	**Precharge Standby Current with Gear Down mode enabled** Same definition like for I_{DD2N}, Gear Down mode enabled(3),(5).
I_{DD2ND}	**Precharge Standby Current with DLL disabled** Same definition like for I_{DD2N}, DLL disabled(3) .
I_{DD2N_par}	**Precharge Standby Current with CA parity enabled** Same definition like for I_{DD2N}, CA parity enabled(3) .
I_{DD2P}	**Precharge Power-Down Current CKE:** LOW; **External clock:** On; **t_{CK}, CL:** See Table 39; **BL:** 8(1); **AL:** 0; **CS_n**: Stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** Stable at 0; **Data I/O:** V_{DDQ}; **DM_n:** Stable at 1; **Bank Activity:** All banks closed; **Output Buffer and R_{TT}:** Enabled in Mode Registers(2); **ODT Signal:** Stable at 0.
I_{PP2P}	**Precharge Power-Down I_{PP} Current** Same condition with I_{DD2P}.
I_{DD2Q}	**Precharge Quiet Standby Current CKE**: HIGH; **External clock:** On; **tCK, CL:** See Table 39; **BL:** 8(1); **AL:** 0; **CS_n**: Stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** Stable at 0; **Data I/O:** V_{DDQ}; **DM_n:** Stable at 1; **Bank Activity:** All banks closed; **Output Buffer and R_{TT}:** Enabled in Mode Registers(2); **ODT Signal:** Stable at 0.
I_{DD3N}	**Active Standby Current (AL = 0) CKE:** HIGH; **External clock:** On; **tCK, CL:** see Table 39; **BL:** 8(1); **AL:** 0; **CS_n:** Stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** Partially toggling according to Table 43. **Data IO**: V_{DDQ}; **DM_n:** Stable at 1; **Bank Activity:** All banks open; **Output Buffer and R_{TT}:** Enabled in Mode Registers2; **ODT Signal:** Stable at 0; **Pattern Details:** See Table 43.
I_{DD3NA}	**Active Standby Current (AL = CL - 1) AL = CL - 1, Other conditions:** See I_{DD3N}

Symbol	Description
I_{PP3N}	**Active Standby I_{PP} Current** Same condition with I_{DD3N}.
I_{DD3P}	**Active Power-Down Current CKE:** LOW; **External clock:** On; **tCK, CL:** See Table 39; **BL:** 8(1); **AL:** 0; **CS_n:** Stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** Stable at 0; **Data I/O:** V_{DDQ}; **DM_n:** Stable at 1; **Bank Activity:** All banks open; **Output Buffer and R_{TT}**: Enabled in Mode Registers2; **ODT Signal:** Stable at 0.
I_{PP3P}	**Active Power-Down I_{PP} Current** Same condition with I_{DD3P}.
I_{DD4R}	**Operating Burst Read Current CKE:** HIGH; **External clock:** On; **tCK, CL:** See Table 39; **BL:** 8(2); **AL:** 0; **CS_n**: HIGH between RD; **Command, Address, Bank Group Address, Bank Address Inputs:** Partially toggling according to Table 45. **Data I/O**: Seamless read data burst with different data between one burst and the next one according to Table 45. **DM_n:** Stable at 1; **Bank Activity:** All banks open, RD commands cycling through banks: 0, 0, 1, 1, 2, 2, ... (see Table 45). **Output Buffer and R_{TT}**: Enabled in Mode Registers(2); **ODT Signal:** Stable at 0; **Pattern Details:** See Table 45.
I_{DD4RA}	**Operating Burst Read Current (AL = CL - 1) AL = CL - 1, Other conditions:** See I_{DD4R}.
I_{DD4RB}	**Operating Burst Read Current with Read DBI Read DBI enabled(3), Other conditions:** See I_{DD4R}.
I_{PP4R}	**Operating Burst Read I_{PP} Current** Same condition with I_{DD4R}.
I_{DDQ4R}	**Operating Burst Read I_{DDQ} Current** Same definition like for I_{DD4R}, however measuring I_{DDQ} current instead of I_{DD} current.
I_{DDQ4RB}	**Operating Burst Read I_{DDQ} Current with READ DBI** Same definition like for I_{DD4RB}, however measuring I_{DDQ} current instead of I_{DD} current.
I_{DD4W}	**Operating Burst Write Current CKE:** HIGH; **External clock:** On; **t_{CK}, CL:** See Table 39; **BL:** 81; **AL:** 0; **CS_n:** HIGH between WR; **Command, Address, Bank Group Address, Bank Address Inputs:** Partially toggling according to Table 46; **Data I/O**: Seamless write data burst with different data between one burst and the next one according to Table 46 **DM_n:** Stable at 1; **Bank Activity:** All banks open, WR commands cycling through banks: 0, 0, 1, 1, 2, 2, ...(Table 46); **Output Buffer and R_{TT}:** Enabled in Mode Registers2; **ODT Signal:** Stable at HIGH; **Pattern Details:** See Table 46.
I_{DD4WA}	**Operating Burst Write Current (AL = CL - 1) AL = CL - 1, Other conditions:** See I_{DD4W}.
I_{DD4WB}	**Operating Burst Write Current with Write DBI Write DBI enabled3, Other conditions:** See I_{DD4W}.

Symbol	Description
I_{DD4WC}	**Operating Burst Write Current with Write CRC Write CRC enabled3, Other conditions:** See I_{DD4W}.
I_{DD4W_par}	**Operating Burst Write Current with CA Parity CA Parity enabled3, Other conditions:** See I_{DD4W}.
I_{PP4W}	**Operating Burst Write I_{PP} Current** Same condition with I_{DD4W}.
I_{DD5B}	**Burst Refresh Current (1X REF) CKE:** HIGH; **External clock:** On; **t_{CK}, CL nRFC:** See Table 39; **BL:** 8(1); **AL:** 0; **CS_n:** HIGH between REF; **Command, Address, Bank Group Address, Bank Address Inputs:** Partially toggling according to Table 48. **Data I/O:** V_{DDQ}; **DM_n:** Stable at 1; **Bank Activity:** REF command every nRFC (see Table 48); **Output Buffer and R_{TT}:** Enabled in Mode Registers(2); **ODT Signal:** Stable at 0; **Pattern Details**: See Table 48.
I_{PP5B}	**Burst Refresh Write I_{PP} Current (1X REF)** Same condition with I_{DD5B}.
I_{DD5F2}	**Burst Refresh Current (2X REF)** **t_{RFC} = $t_{RFC\_}$ * 2, Other conditions:** See I_{DD5B}.
I_{PP5F2}	**Burst Refresh Write I_{PP} Current (2X REF)** Same condition with I_{DD5F2}.
I_{DD5F4}	**Burst Refresh Current (4X REF)** **t_{RFC} = $t_{RFC\_}$ * 4, Other conditions:** See I_{DD5B}.
I_{PP5F4}	**Burst Refresh Write I_{PP} Current (4X REF)** Same condition with I_{DD5F4}.
I_{DD6N}	**Self Refresh Current: Normal Temperature Range T_{CASE}:** 0 - 85°C; **Low Power Array Self Refresh (LP ASR)**: Normal(4); **CKE:** LOW; **External clock:** Off; CK_t and CK_c: LOW; **CL:** See Table 39; **BL:** 8(1); **AL:** 0; **CS_n, Command, Address, Bank Group Address, Bank Address, Data I/O:** HIGH; **DM_n:** Stable at 1; **Bank Activity:** SELF REFRESH operation; **Output Buffer and R_{TT}:** Enabled in Mode Registers(2); **ODT Signal:** MID-LEVEL.
I_{PP6N}	**Self Refresh I_{PP} Current: Normal Temperature Range** Same condition with I_{DD6N}.
I_{DD6E}	**Self Refresh Current: Extended Temperature Range) T_{CASE}:** 0 - 95°C; **Low Power Array Self Refresh (LP ASR)**: Extended(4); **CKE:** LOW; **External clock:** Off; CK_t and CK_c: LOW; **CL:** See Table 39; **BL:** 8(1) **AL:** 0; **CS_n, Command, Address, Bank Group Address, Bank Address, Data I/O:** HIGH; **DM_n**: Stable at 1; **Bank Activity:** Extended Temperature SELF REFRESH operation; **Output Buffer and R_{TT}:** Enabled in Mode Registers(2); **ODT Signal:** MID-LEVEL.
I_{PP6E}	**Self Refresh I_{PP} Current: Extended Temperature Range** Same condition with I_{DD6E}.

Symbol	Description
I_{DD6R}	**Self Refresh Current: Reduced Temperature Range T_{CASE}:** 0 - 45°C; **Low Power Array Self Refresh (LP ASR)**: Reduced(4); **CKE:** LOW; **External clock:** Off; CK_t and CK_c: LOW; **CL:** See Table 39; **BL:** 8(1) **AL:** 0; **CS_n, Command, Address, Bank Group Address, Bank Address, Data I/O:** HIGH; **DM_n**: Stable at 1; **Bank Activity:** Extended Temperature SELF REFRESH operation; **Output Buffer and R_{TT}:** Enabled in Mode Registers(2); **ODT Signal:** MID-LEVEL.
I_{PP6R}	**Self Refresh I_{PP} Current: Reduced Temperature Range** Same condition with I_{DD6R}.
I_{DD6A}	**Auto Self Refresh Current T_{CASE}:** 0 - 95°C; **Low Power Array Self Refresh (LP ASR)**: Auto(4); **CKE:** LOW; **External clock:** Off; CK_t and CK_c: LOW; **CL:** See Table 39; **BL:** 8(1) **AL:** 0; **CS_n, Command, Address, Bank Group Address, Bank Address, Data I/O:** HIGH; **DM_n**: Stable at 1; **Bank Activity:** Auto SELF REFRESH operation; **Output Buffer and R_{TT}:** Enabled in Mode Registers(2); **ODT Signal:** MID-LEVEL.
I_{PP6A}	**Auto Self Refresh I_{PP} Current** Same condition with I_{DD6A}.
I_{DD7}	**Operating Bank Interleave Read Current CKE:** HIGH; **External clock:** On; **tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL:** See Table 39; **BL:** 8(1); **AL:** CL-1; **CS_n**: HIGH between ACT and RDA; **Command, Address, Bank Group Address, Bank Address Inputs:** Partially toggling according to Table 49; **Data I/O:** Read data bursts with different data between one burst and the next one according to Table 49; **DM_n:** Stable at 1; **Bank Activity:** Two times interleaved cycling through banks (0, 1, ...7) with different addressing, see Table 49; **Output Buffer and R_{TT}:** Enabled in Mode Registers(2); **ODT Signal:** Stable at 0; **Pattern Details:** See Table 49.
I_{PP7}	**Operating Bank Interleave Read I_{PP} Current** Same condition with I_{DD7}.
I_{DD8}	**Maximum Power Down Current** **Place DRAM in MPSM then CKE:** HIGH; **External Clock:** On; **tCK, CL:** See Table 39; **BL:** 8(1); **AL:** 0; **CS_n:** stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** Stable at 0; **Data I/O:** V_{DDQ}; **DM_n:** Stable at 1; **Bank Activity:** All banks closed; **Output Buffer and R_{TT}:** Enabled in Mode Registers(2); **ODT Signal:** Stable at 0.
I_{PP8}	**Maximum Power Down I_{PP} Current** Same condition with I_{DD8}.

Note:

1. Burst length: BL8 fixed by MRS: set MR0[A1:0 = 00].
2. Output buffer enable:
   Set MR1 [A12 = 0]: Qoff = Output buffer enabled
   Set MR1 [A2:1 = 00]: Output Driver Impedance Control = $R_{ZQ}/7$
   R_{TT_NOM} enable:
   Set MR1 [A10:8 = 011]: $R_{TT\_NOM} = R_{ZQ}/6$
   R_{TT_WR} enable:
   Set MR2 [A10:9 = 01]: $R_{TT\_WR} = R_{ZQ}/6$
3. CAL enabled: Set MR4 [A8:6 = 001]: 1600MT/s
   010]: 1866MT/s, 2133MT/s
   011]: 2400MT/s
   Gear Down mode enabled: Set MR3 [A3 = 1]: 1/4 Rate
   DLL disabled: Set: MR1 [A0 = 0]
   CA parity enabled: Set MR5 [A2:0 = 001]: 1600MT/s,1866MT/s, 2133MT/s
   010]: 2400MT/s
   Read DBI enabled: Set MR5 [A12 = 1]
   Write DBI enabled: Set: MR5 [A11 = 1]
4. Low Power Array Self Refresh (LP ASR): Set MR2 [A7:6 = 00]: Normal
   01]: Reduced Temperature range
   10]: Extended Temperature range
   11]: Auto Self Refresh
5. I_{DD2NG} should be measured after sync pulse (NOP) input.

8.1.1 I_{DD0}, I_{DD0A} and I_{PP0} Measurement-Loop Pattern

Table 41 - I_{DD0}, I_{DD0A} and I_{PP0} Measurement-Loop Pattern(1)

CK_t/CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0](3)	BG[1:0](2)	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data(4)
Toggling	Static High	0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			1,2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			3,4	D#, D#	1	1	1	1	1	0	0	3(2)	3	0	0	0	7	F	0	-
			...	Repeat pattern 1…4 until nRAS - 1, truncate if necessary																
			nRAS	PRE	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	-
			…	Repeat pattern 1…4 until nRC -1, truncate if necessary																
		1	1 * nRC	Repeat Sub-Loop 0, use BG[1:0](2) = 1, BA[1:0] = 1 instead																
		2	2 * nRC	Repeat Sub-Loop 0, use BG[1:0] (2) = 0, BA[1:0] = 2 instead																
		3	3 * nRC	Repeat Sub-Loop 0, use BG[1:0] (2)= 1, BA[1:0] = 3 instead																
		4	4 * nRC	Repeat Sub-Loop 0, use BG[1:0] (2) = 0, BA[1:0] = 1 instead																
		5	5 * nRC	Repeat Sub-Loop 0, use BG[1:0] (2) = 1, BA[1:0] = 2 instead																
		6	6 * nRC	Repeat Sub-Loop 0, use BG[1:0] (2)= 0, BA[1:0] = 3 instead																
		7	7 * nRC	Repeat Sub-Loop 0, use BG[1:0] (2)= 1, BA[1:0] = 0 instead																
		8	8 * nRC	Repeat Sub-Loop 0, use BG[1:0] (2) = 2, BA[1:0] = 0 instead																For x4 and x8 only
		9	9 * nRC	Repeat Sub-Loop 0, use BG[1:0] (2) = 3, BA[1:0] = 1 instead																
		10	10 * nRC	Repeat Sub-Loop 0, use BG[1:0] (2) = 2, BA[1:0] = 2 instead																
		11	11 * nRC	Repeat Sub-Loop 0, use BG[1:0] (2)= 3, BA[1:0] = 3 instead																
		12	12 * nRC	Repeat Sub-Loop 0, use BG[1:0] (2)= 2, BA[1:0] = 1 instead																
		13	13 * nRC	Repeat Sub-Loop 0, use BG[1:0] (2) = 3, BA[1:0] = 2 instead																
		14	14 * nRC	Repeat Sub-Loop 0, use BG[1:0] (2) = 2, BA[1:0] = 3 instead																
		15	15 * nRC	Repeat Sub-Loop 0, use BG[1:0] (2)= 3, BA[1:0] = 0 instead																

Note:

1. DQS_t, DQS_c are V_{DDQ}.
2. BG1 is a “Don’t Care” for x16 device.
3. C[2:0] are used only for 3DS device.
4. DQ signals are V_{DDQ}.

8.1.2 I_{DD1}, I_{DD1A} and I_{PP1} Measurement-Loop Pattern

Table 42 - I_{DD1}, I_{DD1A} and I_{PP1} Measurement-Loop Pattern(1)

CK_t/CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C2,n(3)	BG[1:0](2)	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data(4)
Toggling	Static High	0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			1,2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			3,4	D#, D#	1	1	1	1	1	0	0	3(2)	3	0	0	0	7	F	0	-
			...	Repeat pattern 1…4 until nRCD – AL - 1, truncate if necessary																
			nRCD – AL	RD	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	D0 = 00, D1 = FF D2 = FF, D3 = 00 D4 = FF, D5 = 00 D6 = 00, D7 = FF
			…	Repeat pattern 1…4 until nRAS - 1, truncate if necessary																
			nRAS	PRE	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	-
			…	Repeat pattern nRC + 1…4 until 1 * nRC + nRAS - 1, truncate if necessary																
		1	1 * nRC + 0	ACT	0	0	0	1	1	0	0	1	1	0	0	0	0	0	0	-
			1 * nRC + 1,2	D,D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			1 * nRC + 3,4	D_#, D_#	1	1	1	1	1	0	0	3b	3	0	0	0	7	F	0	-
			…	Repeat pattern nRC + 1…4 until 1 * nRC + nRAS - 1, truncate if necessary																
			1 * nRC + nRCD – AL	RD	0	1	1	0	1	0	0	1	1	0	0	0	0	0	0	D0 = FF, D1 = 00 D2 = 00, D3 = FF D4 = 00, D5 = FF D6 = FF, D7 = 00
			…	Repeat pattern 1…4 until nRAS - 1, truncate if necessary																
			1 * nRC + nRAS	PRE	0	1	0	1	0	0	0	1	1	0	0	0	0	0	0	-
			…	Repeat nRC + 1…4 unit 2 * nRC -1, truncate if necessary																
		2	2 * nRC	Repeat Sub-Loop 0, use BG[1:0](2) = 0, BA[1:0] = 2 instead																
		3	3 * nRC	Repeat Sub-Loop 1, use BG[1:0](2) = 1, BA[1:0] = 3 instead																
		4	4 * nRC	Repeat Sub-Loop 0, use BG[1:0](2) = 0, BA[1:0] = 1 instead																
		5	5 * nRC	Repeat Sub-Loop 1, use BG[1:0](2) = 1, BA[1:0] = 2 instead																
		6	6 * nRC	Repeat Sub-Loop 0, use BG[1:0](2) = 0, BA[1:0] = 3 instead																
		8	7 * nRC	Repeat Sub-Loop 1, use BG[1:0](2) = 1, BA[1:0] = 0 instead																
		9	9 * nRC	Repeat Sub-Loop 1, use BG[1:0](2) = 2, BA[1:0] = 0 instead																For x4 and x8 only
		10	10 * nRC	Repeat Sub-Loop 0, use BG[1:0](2) = 3, BA[1:0] = 1 instead																
		11	11 * nRC	Repeat Sub-Loop 1, use BG[1:0](2) = 2, BA[1:0] = 2 instead																
		12	12 * nRC	Repeat Sub-Loop 0, use BG[1:0](2) = 3, BA[1:0] = 3 instead																
		13	13 * nRC	Repeat Sub-Loop 1, use BG[1:0](2) = 2, BA[1:0] = 1 instead																
		14	14 * nRC	Repeat Sub-Loop 0, use BG[1:0](2) = 3, BA[1:0] = 2 instead																
		15	15 * nRC	Repeat Sub-Loop 1, use BG[1:0](2) = 2, BA[1:0] = 3 instead																
		16	16 * nRC	Repeat Sub-Loop 0, use BG[1:0](2) = 3, BA[1:0] = 0 instead																

Note:

1. DQS_t, DQS_c are used according to RD Commands, otherwise V_{DDQ}.
2. BG1 is a “Don’t Care” for x16 device.
3. C[2:0] are used only for 3DS device.
4. Burst Sequence driven on each DQ signal by READ Command. Outside burst operation, DQ signals are V_{DDQ}.

8.1.3 I_{DD2N}, I_{DD2NA}, I_{DD2NL}, I_{DD2NG}, I_{DD2ND}, I_{DD2N_par}, I_{PP2}, I_{DD3N}, I_{DD3NA} and I_{DD3P} Measurement-Loop Pattern

Table 43 - I_{DD2N}, I_{DD2NA}, I_{DD2NL}, I_{DD2NG}, I_{DD2ND}, I_{DD2N_par}, I_{PP2}, I_{DD3N}, I_{DD3NA} and I_{DD3P} Measurement-Loop Pattern(1)

CK_t/CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0](3)	BG[1:0](2)	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data(4)
Toggling	Static High	0	0	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
			1	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
			2	D#, D#	1	1	1	1	1	0	0	3(2)	3	0	0	0	7	F	0	0
			3	D#, D#	1	1	1	1	1	0	0	3(2)	3	0	0	0	7	F	0	0
		1	4-7	Repeat Sub-Loop 0, use BG[1:0](2) = 1, BA[1:0] = 1 instead															
		2	8-11	Repeat Sub-Loop 0, use BG[1:0](2) = 0, BA[1:0] = 2 nstead															
		3	12-15	Repeat Sub-Loop 0, use BG[1:0](2) = 1, BA[1:0] = 3 instead															
		4	16-19	Repeat Sub-Loop 0, use BG[1:0](2) = 0, BA[1:0] = 1 instead															
		5	20-23	Repeat Sub-Loop 0, use BG[1:0](2) = 1, BA[1:0] = 2 instead															
		6	24-27	Repeat Sub-Loop 0, use BG[1:0](2) = 0, BA[1:0] = 3 instead															
		7	28-31	Repeat Sub-Loop 0, use BG[1:0](2) = 1, BA[1:0] = 0 instead															
		8	32-35	Repeat Sub-Loop 0, use BG[1:0](2) = 2, BA[1:0] = 0 instead															
		9	36-39	Repeat Sub-Loop 0, use BG[1:0](2) = 3, BA[1:0] = 1 instead															
		10	40-43	Repeat Sub-Loop 0, use BG[1:0](2) = 2, BA[1:0] = 2 instead															
		11	44-47	Repeat Sub-Loop 0, use BG[1:0](2) = 3, BA[1:0] = 3 instead															
		12	48-51	Repeat Sub-Loop 0, use BG[1:0](2) = 2, BA[1:0] = 1 instead															
		13	52-55	Repeat Sub-Loop 0, use BG[1:0](2) = 3, BA[1:0] = 2 instead															
		14	56-59	Repeat Sub-Loop 0, use BG[1:0](2) = 2, BA[1:0] = 3 instead															
		15	60-63	Repeat Sub-Loop 0, use BG[1:0](2) = 3, BA[1:0] = 0 instead															

Note:

1. DQS_t, DQS_c are V_{DDQ}.
2. BG1 is a “Don’t Care” for x16 device.
3. C[2:0] are used only for 3DS device.
4. DQ signals are V_{DDQ}.

8.1.4 I_{DD2NT} and I_{DDQ2NT} Measurement-Loop Pattern

Table 44 - I_{DD2NT} and I_{DDQ2NT} Measurement-Loop Pattern(1)

CK_t/CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0](3)	BG[1:0](2)	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data(4)
Toggling	Static High	0	0	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			1	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			2	D#, D#	1	1	1	1	1	0	0	3(2)	3	0	0	0	7	F	0	-
			3	D#, D#	1	1	1	1	1	0	0	3(2)	3	0	0	0	7	F	0	-
		1	4-7	Repeat Sub-Loop 0, but ODT = 1 and BG[1:0](2) = 1, BA[1:0] = 1 instead																
		2	8-11	Repeat Sub-Loop 0, but ODT = 0 and BG[1:0](2) = 0, BA[1:0] = 2 instead																
		3	12-15	Repeat Sub-Loop 0, but ODT = 1 and BG[1:0](2) = 1, BA[1:0] = 3 instead																
		4	16-19	Repeat Sub-Loop 0, but ODT = 0 and BG[1:0](2) = 0, BA[1:0] = 1 instead																
		5	20-23	Repeat Sub-Loop 0, but ODT = 1 and BG[1:0](2) = 1, BA[1:0] = 2 instead																
		6	24-27	Repeat Sub-Loop 0, but ODT = 0 and BG[1:0](2) = 0, BA[1:0] = 3 instead																
		7	28-31	Repeat Sub-Loop 0, but ODT = 1 and BG[1:0](2) = 1, BA[1:0] = 0 instead																
		8	32-35	Repeat Sub-Loop 0, but ODT = 0 and BG[1:0](2) = 2, BA[1:0] = 0 instead																For x4 and x8 only
		9	36-39	Repeat Sub-Loop 0, but ODT = 1 and BG[1:0](2) = 3, BA[1:0] = 1 instead																
		10	40-43	Repeat Sub-Loop 0, but ODT = 0 and BG[1:0](2) = 2, BA[1:0] = 2 instead																
		11	44-47	Repeat Sub-Loop 0, but ODT = 1 and BG[1:0](2) = 3, BA[1:0] = 3 instead																
		12	48-51	Repeat Sub-Loop 0, but ODT = 0 and BG[1:0](2) = 2, BA[1:0] = 1 instead																
		13	52-55	Repeat Sub-Loop 0, but ODT = 1 and BG[1:0](2) = 3, BA[1:0] = 2 instead																
		14	56-59	Repeat Sub-Loop 0, but ODT = 0 and BG[1:0](2) = 2, BA[1:0] = 3 instead																
		15	60-63	Repeat Sub-Loop 0, but ODT = 1 and BG[1:0](2) = 3, BA[1:0] = 0 instead																

Note:

1. DQS_t, DQS_c are V_{DDQ}.
2. BG1 is a “Don’t Care” for x16 device.
3. C[2:0] are used only for 3DS device.
4. DQ signals are V_{DDQ}.

8.1.5 I_{DD4R}, I_{DDR4RA}, I_{DD4RB} and I_{DDQ4R} Measurement-Loop Pattern1

Table 45 - I_{DD4R}, I_{DDR4RA}, I_{DDR4RB} and I_{DDQ4R} Measurement-Loop Pattern(1)

CK_t/CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0](3)	BG[1:0](2)	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data(4)
Toggling	Static High	0	0	RD	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	D0 = 00, D1 = FF D2 = FF, D3 = 00 D4 = FF, D5 = 00 D6 = 00, D7 = FF
			1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			2,3	D#, D#	1	1	1	1	1	0	0	3(2)	3	0	0	0	7	F	0	-
		1	4	RD	0	1	1	0	1	0	0	1	1	0	0	0	7	F	0	D0 = FF, D1 = 00 D2 = 00, D3 = FF D4 = 00, D5 = FF D6 = FF, D7 = 00
			5	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			6,7	D#, D#	1	1	1	1	1	0	0	3(2)	3	0	0	0	7	F	0	-
		2	8-11	Repeat Sub-Loop 0, use BG[1:0](2) = 0, BA[1:0] = 2 instead															
		3	12-15	Repeat Sub-Loop 1, use BG[1:0](2) = 1, BA[1:0] = 3 instead															
		4	16-19	Repeat Sub-Loop 0, use BG[1:0](2) = 0, BA[1:0] = 1 instead															
		5	20-23	Repeat Sub-Loop 1, use BG[1:0](2) = 1, BA[1:0] = 2 instead															
		6	24-27	Repeat Sub-Loop 0, use BG[1:0](2) = 0, BA[1:0] = 3 instead															
		7	28-31	Repeat Sub-Loop 1, use BG[1:0](2) = 1, BA[1:0] = 0 instead															
		8	32-35	Repeat Sub-Loop 0, use BG[1:0](2) = 2, BA[1:0] = 0 instead															For x4 and x8 only
		9	36-39	Repeat Sub-Loop 1, use BG[1:0](2) = 3, BA[1:0] = 1 instead															
		10	40-43	Repeat Sub-Loop 0, use BG[1:0](2) = 2, BA[1:0] = 2 instead															
		11	44-47	Repeat Sub-Loop 1, use BG[1:0](2) = 3, BA[1:0] = 3 instead															
		12	48-51	Repeat Sub-Loop 0, use BG[1:0](2) = 2, BA[1:0] = 1 instead															
		13	52-55	Repeat Sub-Loop 1, use BG[1:0](2) = 3, BA[1:0] = 2 instead															
		14	56-59	Repeat Sub-Loop 0, use BG[1:0](2) = 2, BA[1:0] = 3 instead															
		15	60-63	Repeat Sub-Loop 1, use BG[1:0](2) = 3, BA[1:0] = 0 instead															

Note:

1. DQS_t, DQS_c are used according to RD Commands, otherwise V_{DDQ}.
2. BG1 is a “Don’t Care” for x16 device.
3. C[2:0] are used only for 3DS device.
4. Burst Sequence driven on each DQ signal by READ Command.

8.1.6 I_{DD4W}, I_{DDR4WA}, I_{DD4WB} and I_{DD4W_par} Measurement-Loop Pattern

Table 46 - I_{DD4W}, I_{DDR4WA}, I_{DD4WB} and I_{DD4W_par} Measurement-Loop Pattern

CK_t/CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0](3)	BG[1:0](2)	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data(4)
Toggling	Static High	0	0	WR	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	D0 = 00, D1 = FF D2 = FF, D3 = 00 D4 = FF, D5 = 00 D6 = 00, D7 = FF
			1	D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	-
			2,3	D#, D#	1	1	1	1	1	1	0	3(2)	3	0	0	0	7	F	0	-
		1	4	WR	0	1	1	0	0	1	0	1	1	0	0	0	7	F	0	D0 = FF, D1 = 00 D2 = 00, D3 = FF D4 = 00, D5 = FF D6 = FF, D7 = 00
			5	D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	-
			6,7	D#, D#	1	1	1	1	1	1	0	3(2)	3	0	0	0	7	F	0	-
		2	8-11	Repeat Sub-Loop 0, use BG[1:0](2) = 0, BA[1:0] = 2 instead															
		3	12-15	Repeat Sub-Loop 1, use BG[1:0](2) = 1, BA[1:0] = 3 instead																
		4	16-19	Repeat Sub-Loop 0, use BG[1:0](2) = 0, BA[1:0] = 1 instead																
		5	20-23	Repeat Sub-Loop 1, use BG[1:0](2) = 1, BA[1:0] = 2 instead																
		6	24-27	Repeat Sub-Loop 0, use BG[1:0](2) = 0, BA[1:0] = 3 instead																
		7	28-31	Repeat Sub-Loop 1, use BG[1:0](2) = 1, BA[1:0] = 0 instead																
		8	32-35	Repeat Sub-Loop 0, use BG[1:0](2) = 2, BA[1:0] = 0 instead																For x4 and x8 only
		9	36-39	Repeat Sub-Loop 1, use BG[1:0](2) = 3, BA[1:0] = 1 instead																
		10	40-43	Repeat Sub-Loop 0, use BG[1:0](2) = 2, BA[1:0] = 2 instead																
		11	44-47	Repeat Sub-Loop 1, use BG[1:0](2) = 3, BA[1:0] = 3 instead																
		12	48-51	Repeat Sub-Loop 0, use BG[1:0](2) = 2, BA[1:0] = 1 instead																
		13	52-55	Repeat Sub-Loop 1, use BG[1:0](2) = 3, BA[1:0] = 2 instead																
		14	56-59	Repeat Sub-Loop 0, use BG[1:0](2) = 2, BA[1:0] = 3 instead																
		15	60-63	Repeat Sub-Loop 1, use BG[1:0](2) = 3, BA[1:0] = 0 instead																

Note:

1. DQS_t, DQS_c are used according to WR Commands, otherwise V_{DDQ}.
2. BG1 is a “Don’t Care” for x16 device.
3. C[2:0] are used only for 3DS device.
4. Burst Sequence driven on each DQ signal by WRITE Command.

8.1.7 I_{DD4WC} Measurement-Loop Pattern

Table 47 - I_{DD4WC} Measurement-Loop Pattern(1)

CK_t/CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0](3)	BG[1:0](2)	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data(4)
Toggling	Static High	0	0	WR	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	D0 = 00, D1 = FF D2 = FF, D3 = 00 D4 = FF, D5 = 00 D6 = 00, D7 = FF D8 = CRC
			1,2	D, D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	-
			3,4	D#, D#	1	1	1	1	1	1	0	3(2)	3	0	0	0	7	F	0	-
			5	WR	0	1	1	0	0	1	0	1	1	0	0	0	7	F	0	D0 = FF, D1 = 00 D2 = 00, D3 = FF D4 = 00, D5 = FF D6 = FF, D7 = 00 D8 = CRC
			6,7	D, D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	-
			8,9	D#, D#	1	1	1	1	1	1	0	3(2)	3	0	0	0	7	F	0	-
		2	10-14	Repeat Sub-Loop 0, use BG[1:0](2) = 0, BA[1:0] = 2 instead															
		3	15-19	Repeat Sub-Loop 1, use BG[1:0](2) = 1, BA[1:0] = 3 instead															
		4	20-24	Repeat Sub-Loop 0, use BG[1:0](2) = 0, BA[1:0] = 1 instead															
		5	25-29	Repeat Sub-Loop 1, use BG[1:0](2) = 1, BA[1:0] = 2 instead															
		6	30-34	Repeat Sub-Loop 0, use BG[1:0](2) = 0, BA[1:0] = 3 instead															
		7	35-39	Repeat Sub-Loop 1, use BG[1:0](2) = 1, BA[1:0] = 0 instead															
		8	40-44	Repeat Sub-Loop 0, use BG[1:0](2) = 2, BA[1:0] = 0 instead															For x4 and x8 only
		9	45-49	Repeat Sub-Loop 1, use BG[1:0](2) = 3, BA[1:0] = 1 instead															
		10	50-54	Repeat Sub-Loop 0, use BG[1:0](2) = 2, BA[1:0] = 2 instead															
		11	55-59	Repeat Sub-Loop 1, use BG[1:0](2) = 3, BA[1:0] = 3 instead															
		12	60-64	Repeat Sub-Loop 0, use BG[1:0](2) = 2, BA[1:0] = 1 instead															
		13	65-69	Repeat Sub-Loop 1, use BG[1:0](2) = 3, BA[1:0] = 2 instead															
		14	70-74	Repeat Sub-Loop 0, use BG[1:0](2) = 2, BA[1:0] = 3 instead															
		15	75-79	Repeat Sub-Loop 1, use BG[1:0](2) = 3, BA[1:0] = 0 instead															

Note:

1. DQS_t, DQS_c are V_{DDQ}.
2. BG1 is a “Don’t Care” for x16 device.
3. C[2:0] are used only for 3DS device.
4. Burst Sequence driven on each DQ signal by WRITE Command.

8.1.8 I_{DD5B} Measurement-Loop Pattern

Table 48 - I_{DD5B} Measurement-Loop Pattern(1)

CK_t/CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0](3)	BG[1:0](2)	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	[6:3]	A[2:0]	Data(4)
Toggling	Static High	0	0	REF	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
		1	1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			2	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			3	D#, D#	1	1	1	1	1	0	0	3(2)	3	0	0	0	7	F	0	-
			4	D#, D#	1	1	1	1	1	0	0	3(2)	3	0	0	0	7	F	0	-
			4-7	Repeat pattern 1…4, use BG[1:0](2) = 1, BA[1:0] = 1 instead.																
			8-11	Repeat pattern 1…4, use BG[1:0](2) = 0, BA[1:0] = 2 instead.																
			12-15	Repeat pattern 1…4, use BG[1:0](2) = 1, BA[1:0] = 3 instead.																
			16-19	Repeat pattern 1…4, use BG[1:0](2) = 0, BA[1:0] = 1 instead.																
			20-23	Repeat pattern 1…4, use BG[1:0](2) = 1, BA[1:0] = 2 instead.																
			24-27	Repeat pattern 1…4, use BG[1:0](2) = 0, BA[1:0] = 3 instead.																
			28-31	Repeat pattern 1…4, use BG[1:0](2) = 1, BA[1:0] = 0 instead.																
			32-35	Repeat pattern 1…4, use BG[1:0](2) = 2, BA[1:0] = 0 instead.																For x4 and x8 only
			36-39	Repeat pattern 1…4, use BG[1:0](2) = 3, BA[1:0] = 1 instead.																
			40-43	Repeat pattern 1…4, use BG[1:0](2) = 2, BA[1:0] = 2 instead.																
			44-47	Repeat pattern 1…4, use BG[1:0](2) = 3, BA[1:0] = 3 instead.																
			48-51	Repeat pattern 1…4, use BG[1:0](2) = 2, BA[1:0] = 1 instead.																
			52-55	Repeat pattern 1…4, use BG[1:0](2) = 3, BA[1:0] = 2 instead.																
			56-59	Repeat pattern 1…4, use BG[1:0](2) = 2, BA[1:0] = 3 instead.																
			60-63	Repeat pattern 1…4, use BG[1:0](2) = 3, BA[1:0] = 0 instead.																
		2	64…nRFC-1	Repeat Sub-Loop 1, Truncate, if necessary																

Note:

1. DQS_t, DQS_c are V_{DDQ}.
2. BG1 is a “Don’t Care” for x16 device.
3. C[2:0] are used only for 3DS device.
4. DQ signals are V_{DDQ}.

8.1.9 I_{DD7} Measurement-Loop Pattern

Table 49 - I_{DD7} Measurement-Loop Pattern(1)

CK_t/CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0](3)	BG[1:0](2)	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data(4)
Toggling	Static High	0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			1	RDA	0	1	1	0	1	0		0	0	0	0	1	0	0	0	D0 = 00, D1 = FF D2 = FF, D3 = 00 D4 = FF, D5 = 00 D6 = 00, D7 = FF
			2	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-

CK_t/CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0](3)	BG[1:0](2)	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data(4)
			3	D #	1	1	1	1	1	0	0	3(2)	3	0	0	0	7	F	0	-
			…	Repeat pattern 2…3, until nRRD – 1, if nRRD > 4. Truncate if necessary.																
		1	nRRD	ACT	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	-
			nRRD + 1	RDA	0	1	1	0	1	0		1	1	0	0	1	0	0	0	D0 = FF, D1 = 00 D2 = 00, D3 = FF D4 = 00, D5 = FF D6 = FF, D7 = 00
			…	Repeat pattern 2…3, until 2 * nRRD – 1, if nRRD > 4. Truncate if necessary.																
		2	2 * nRRD	Repeat Sub-Loop 0, use BG[1:0](2) = 0, BA[1:0] = 2 instead.																
		3	3 * nRRD	Repeat Sub-Loop 1, use BG[1:0](2) = 1, BA[1:0] = 3 instead.																
		4	4 * nRRD	Repeat pattern 2…3, until nFAW – 1, if nFAW > 4 * nRRD. Truncate if necessary.																
		5	nFAW	Repeat Sub-Loop 0, use BG[1:0](2) = 0, BA[1:0] = 1 instead.																
		6	nFAW + nRRD	Repeat Sub-Loop 1, use BG[1:0](2) = 1, BA[1:0] = 2 instead.																
		7	nFAW + 2 * nRRD	Repeat Sub-Loop 0, use BG[1:0](2) = 0, BA[1:0] = 3 instead.																
		8	nFAW + 3 * nRRD	Repeat Sub-Loop 1, use BG[1:0](2) = 1, BA[1:0] = 0 instead.																
		9	nFAW + 4 * nRRD	Repeat Sub-Loop 4																
		10	2 * nFAW	repeat Sub-Loop 0, use BG[1:0](2) = 2, BA[1:0] = 0 instead.																For x4 and x8 only
		11	2*nFAW + nRRD	repeat Sub-Loop 1, use BG[1:0](2) = 3, BA[1:0] = 1 instead.																
		12	* nFAW + 2 * nRRD	repeat Sub-Loop 0, use BG[1:0](2) = 2, BA[1:0] = 2 instead.																
		13	* nFAW + 3 * nRRD	repeat Sub-Loop 1, use BG[1:0](2) = 3, BA[1:0] = 3 instead.																
		14	* nFAW + 4 * nRRD	repeat Sub-Loop 4.																
		15	3 * nFAW	repeat Sub-Loop 0, use BG[1:0](2) = 2, BA[1:0] = 1 instead.																
		16	3 * nFAW + nRRD	repeat Sub-Loop 1, use BG[1:0](2) = 3, BA[1:0] = 2 instead.																
		17	* nFAW + 2 * nRRD	repeat Sub-Loop 0, use BG[1:0](2) = 2, BA[1:0] = 3 instead.																
		18	* nFAW + 3 * nRRD	repeat Sub-Loop 1, use BG[1:0](2) = 3, BA[1:0] = 0 instead.																
		19	* nFAW + 4 * nRRD	repeat Sub-Loop 4																
		20	4 * nFAW	repeat pattern 2…3, until nRC – 1, if nRC > 4 * nFAW. Truncate if necessary.																

Note:

1. DQS_t, DQS_c are V_{DDQ}.
2. BG1 is a “Don’t Care” for x16 device.
3. C[2:0] are used only for 3DS device.
4. Burst Sequence driven on each DQ signal by READ Command. Outside burst operation, DQ signals are V_{DDQ}.

8.1 I_{DD} Specifications

I_{DD} and I_{PP} values are for full operation range of voltage and temperature unless otherwise noted.

Table 50 - I_{DD} and I_{DDQ} Specifications

Symbol	DDR4-2400		DDR4-2666		DDR4-3200		Unit
	X8	X16	X8	X16	X8	X16	
I_{DD0}	72	91	75	93	82	101	mA
I_{DD1}	87	116	90	119	96	126	mA
I_{DD2N}	71	71	73	73	79	79	mA
I_{DD2NT}	80	80	83	83	90	90	mA
I_{DD2P}	52	52	53	53	55	55	mA
I_{DD2Q}	68	68	70	70	74	74	mA
I_{DD3N}	90	96	93	98	99	103	mA
I_{DD3P}	66	69	67	69	68	71	mA
I_{DD4R}	169	244	182	263	203	294	mA
I_{DD4W}	166	228	177	247	198	278	mA
I_{DD5R}	86	86	89	89	94	94	mA
I_{DD6N}	82	82	82	82	82	82	mA
I_{DD6E}	100	100	100	100	100	100	mA
I_{DD6R}	79	79	79	79	79	79	mA
I_{DD6A}	100	100	100	100	100	100	mA
I_{DD7}	222	297	230	302	237	311	mA

Table 51 - I_{PP} Specifications

Symbol	DDR4-2400		DDR4-2666		DDR4-3200		Unit
	x8	x16	x8	x16	x8	x16	
I_{PP0}	4	6	4	6	4	6	mA
I_{PP3N}	4	5	4	5	4	5	mA
I_{PP5R}	4	5	4	5	4	5	mA
I_{PP6N}	82	82	82	82	82	82	mA
I_{PP6E}	100	100	100	100	100	100	mA
I_{PP6R}	79	79	79	79	79	79	mA
I_{PP6A}	100	100	100	100	100	100	mA
I_{PP7}	19	25	19	25	19	25	mA

Table 52- I_{DD6} Specifications

Symbol	Temperature Range	DDR4-2400		DDR4-2666		DDR4-3200		Unit	Note
		x8	x16	x8	x16	x8	x16		
I_{DD6N}	0~85°	82	82	82	82	82	82	mA	3,4
I_{DD6E}	0~95°	100	100	100	100	100	100	mA	4,5,6
I_{DD6R}	0~45°	79	79	79	79	79	79	mA	4,6,9
I_{DD6A}	0~95°	100	100	100	100	100	100	mA	4,6,7,8

Note:

1. Some I_{DD} currents are higher for x16 organization due to larger page size architecture.
2. Max values for I_{DD} currents considering worst case conditions of process, temperature and voltage.
3. Applicable for MR2 settings A6 =0 and A7=0.
4. Datasheet include a max value for I_{DD6}.
5. Applicable for MR2 settings A6 = 0 and A7 = 1. I_{DD6E} is only specified for devices which support the Extended Temperature Range feature.
6. Refer to datasheet for the value specification method (e.g. max, typical) for I_{DD6E} and I_{DD6A}.
7. Applicable for MR2 settings A6 = 1 and A7 = 0. I_{DD6A} is only specified for devices which support the Auto Self Refresh feature.
8. The number of discrete temperature ranges supported and the associated Ta-Tz values are supplier/design specific. Temperature ranges are specified for all supported values of TOPER. Refer to supplier datasheet for more information.
9. Applicable for MR2 settings MR2 [A7:A6 = 01]: Reduced Temperature range. I_{DD6R} is verified by design and characterization, and may not be subject to production test.

9 Input/Output Capacitance

Table 53 - Silicon Pad I/O Capacitance

Symbol	Parameter	1600/1866/2133		2400/2666		3200		Unit	Note
		Min	Max	Min	Max	Min	Max		
C_{IO}	Input/output capacitance	0.55	1.4	0.55	1.15	0.55	1.00	pF	1,2,3
C_{DIO}	Input/output capacitance delta	-0.1	0.1	-0.1	0.1	-0.1	0.1	pF	1,2,3,11
C_{DDQS}	Input/output capacitance delta DQS_t and DQS_c	-	0.05	-	0.05	-	0.05	pF	1,2,3,5
C_{CK}	Input capacitance, CK_t and CK_c	0.2	0.8	0.2	0.7	0.2	0.7	pF	1,3
C_{DCK}	Input capacitance delta CK_t and CK_c	-	0.05	-	0.05	-	0.05	pF	1,3,4
C_{I}	Input capacitance (CTRL, ADD, CMD pins only)	0.2	0.8	0.2	0.7	0.2	0.55	pF	1,3,6
C_{DI_CTRL}	Input capacitance delta (All CTRL pins only)	-0.1	0.1	-0.1	0.1	-0.1	0.1	pF	1,3,7,8
$C_{DI\_ADD\_CMD}$	Input capacitance delta (All ADD/ CMD pins only)	-0.1	0.1	-0.1	0.1	-0.1	0.1	pF	1,2,9,10
C_{ALERT}	Input/output capacitance of ALERT	0.5	1.5	0.5	1.5	0.5	1.5	pF	1,3
C_{ZQ}	Input/output capacitance of ZQ	-	2.3	-	2.3	-	2.3	pF	1,3,12
C_{TEN}	Input capacitance of TEN	0.2	2.3	0.2	2.3	0.2	2.3	pF	1,3,13

Note:

1. This parameter is not subject to production test. It is verified by design and characterization. The silicon only capacitance is validated by deembedding the package L & C parasitic. The capacitance is measured with VDD, VDDQ, VSS, VSSQ applied with all other signal pins floating.
2. DQ, DM_n, DQS_t, DQS_c, TDQS_t, TDQS_c. Although the DM, TDQS_t and TDQS_c pins have different functions, the loading matches DQ and DQS.
3. This parameter applies to monolithic devices only; stacked/dual die devices are not covered here.
4. Absolute value of CK_t - CK_c.
5. Absolute value of CIO(DQS_t) - CIO(DQS_c).
6. CI applies to ODT, CS_n, CKE, A0 - A17, BA0 - BA1, BG0 - BG1, RAS_n/A16, CAS_n/A15, WE_n/A14, ACT_n and PAR.
7. CDI_CTRL applies to ODT, CS_n and CKE.
8. CDI_CTRL = CI(CTRL) - 0.5 * (CI(CLK_T) + CI(CLK_C)).
9. CDI_ADD_CMD applies to, A0 - A17, BA0 - BA1, BG0 - BG1, RAS_n/A16, CAS_n/A15, WE_n/A14, ACT_n and PAR.
10. CDI_ADD_CMD = CI(ADD_CMD) - 0.5 * (CI(CLK_T) + CI(CLK_C)).
11. CDIO = CIO(DQ, DM) - 0.5 * (CIO(DQS_t) + CIO(DQS_c)).
12. Maximum external load capacitance on ZQ pin: 5pF.
13. TEN pin may be DRAM internally pulled low through a weak pull-down resistor to VSS. In this case CTEN might not be valid and system shall verify TEN signal with Vendor specific information.

Table 54 - DRAM Package Electrical Specifications (x16)

Symbol	Parameter	1600/1866/2133		2400/2666/3200		Unit	Note
		Min	Max	Min	Max		
Z_{IO}	Input/output Zpkg	45	85	45	85	Ω	1
Td_{IO}	Input/output Pkg Delay	14	45	14	45	ps	1
L_{IO}	Input/output Lpkg	-	3.4	-	3.4	nH	1,2
C_{IO}	Input/output Cpkg	-	0.82	-	0.82	pF	1,3
$Z_{IO\ DQS}$	DQS_t and DQS_c Zpkg	45	85	45	85	Ω	1
$Td_{IO\ DQS}$	DQS_t and DQS_c Pkg Delay	14	45	14	45	ps	1
$L_{IO\ DQS}$	DQS Lpkg	-	3.4	-	3.4	nH	1,2
$C_{IO\ DQS}$	DQS Cpkg	-	0.82	-	0.82	pF	1,3
$DZ_{IO\ DQS}$	Delta Zpkg DQSU_t, DQSU_c	-	10	-	10	Ω	-
	Delta Zpkg DQSL_t, DQSL_c	-	10	-	10	Ω	-
$DTd_{IO\ DQS}$	Delta Delay DQSU_t, DQSU_c	-	5	-	5	ps	-
	Delta Delay DQSL_t, DQSL_c	-	5	-	5	ps	-
$Z_{I\ CTRL}$	Input-CTRL pins Zpkg	50	90	50	90	Ω	1
$Td_{I\ ADD\ CMD}$	Input-CTRL pins Pkg Delay	14	42	14	42	ps	1
$L_{I\ CTRL}$	Input CTRL Lpkg	-	3.4	-	3.4	nH	1,2
$C_{I\ CTRL}$	Input CTRL Cpkg	-	0.7	-	0.7	pF	1,3
$Z_{I\ ADD\ CMD}$	Input-CMD ADD pins Zpkg	50	90	50	90	Ω	1
$Td_{I\ ADD\ CMD}$	Input-CMD ADD pins Pkg Delay	14	52	14	52	ps	1
$L_{I\ ADD\ CMD}$	Input-CMD ADD Lpkg	-	3.9	-	3.9	nH	1,2
$C_{I\ ADD\ CMD}$	Input-CMD ADD Cpkg	-	0.86	-	0.86	pF	1,3
Z_{CK}	CK_c Zpkg	50	90	50	90	Ω	1
Td_{CK}	CK_c Pkg Delay	14	42	14	42	ps	1
$L_{I\ CLK}$	Input CK Lpkg	-	3.4	-	3.4	nH	1,2
$C_{I\ CLK}$	Input CK Cpkg	-	0.7	-	0.7	pF	1,3
DZ_{DCK}	Delta Zpkg CK_t and CK_c	-	10	-	10	Ω	-
DTd_{DCK}	Delta Delay CK_t and CK_c	-	5	-	5	ps	-
$Z_{O\ ZQ}$	ZQ Zpkg	-	100	-	100	Ω	-
$Td_{O\ ZQ}$	ZQ Delay	20	90	20	90	ps	-
$Z_{O\ ALERT}$	ALERT Zpkg	40	100	40	100	Ω	-
$Td_{O\ ALERT}$	ALERT Delay	20	55	20	55	ps	-

Note:

1. Package implementations shall meet spec if the Zpkg and Pkg Delay fall within the ranges shown, and the maximum Lpkg and Cpkg do not exceed the maximum value shown.
2. It is assumed that Lpkg can be approximated as Lpkg = Zo * Td.
3. It is assumed that Cpkg can be approximated as Cpkg = Td/Zo.

10 Electrical Characteristics And Ac Timing

10.1 Reference Load for AC Timing and Output Slew Rate

Figure 25 represents the effective reference load of 50Ω used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.

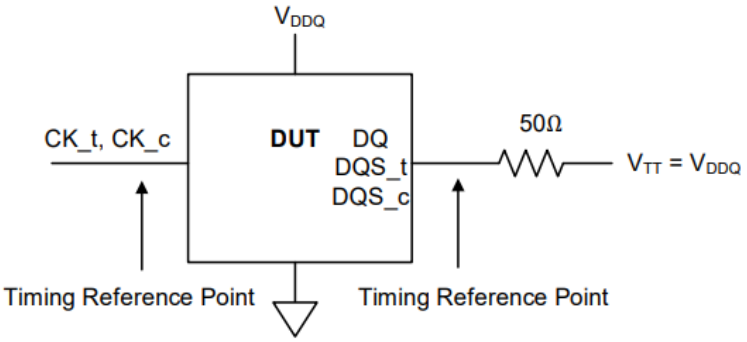
R_{ON} nominal of DQ, DQS_t and DQS_c drivers uses 34Ω to specify the relevant AC timing parameter values of the device.

- The maximum DC high level of output signal = 1.0 * V_{DDQ}
- The minimum DC low level of output signal = {34/(34 + 50)} * V_{DDQ} = 0.4 * V_{DDQ}
- The nominal reference level of an output signal can be approximated by the following:
- The center of maximum DC high and minimum DC low = {(1 + 0.4)/2} * V_{DDQ} = 0.7 * V_{DDQ}

The actual reference level of output signal might vary with driver R_{ON} and reference load tolerances. Thus, the actual reference level or midpoint of an output signal is at the widest part of the output signal's eye. Prior to measuring AC parameters, the reference level of the verification tool should be set to an appropriate level.

It is not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

Figure 27 - Reference Load for AC Timing and Output Slew Rate



10.2 tREFI

Average periodic Refresh interval (t_{REFI}) of DDR4 SDRAM is defined as shown in Table 55 below.

Table 55 - t_{REFI} by Device Density

Parameter	Symbol		8Gb	Unit
Average periodic refresh interval	t_{REFI}	0°C ≤ T_{CASE} ≤ 85°C	7.8	µs
		85°C ≤ T_{CASE} ≤ 95°C	3.9	µs

10.3 Clock Specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input clocks violating the min/max values may result in malfunction of the DDR4 SDRAM device.

10.4 Definition for $t_{CK\ (ABS)}$

$t_{CK(ABS)}$ is defined as the absolute clock period, as measured from one rising edge to the next consecutive rising edge. $t_{CK(ABS)}$ is not subject to production test.

10.4.1 Definition for $t_{CK\ (avg)}$

$t_{CK\ (avg)}$ is calculated as the average clock period across any consecutive 200 cycle windows, where each clock period is calculated from rising edge to rising edge.

$$t_{CK\ (avg)} = (\sum_{j=1}^{N} t_{CK\ (avg)j})/N \quad N = 200$$

10.4.2 Definition for $t_{CH\ (avg)}$ and $t_{CL\ (avg)}$

$t_{CH\ (avg)}$ is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

$$t_{CH\ (avg)} = (\sum_{j=1}^{N} t_{CHj})/(N * t_{CK\ (avg)}) \quad N = 200$$

$t_{CL\ (avg)}$ is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$t_{CL\ (avg)} = (\sum_{j=1}^{N} t_{CLj})/(N * t_{CK\ (avg)}) \quad N = 200$$

10.4.3 Definition for tERR (nper)

t_{ERR} is defined as the cumulative error across n consecutive cycles of n * tCK (avg). tERR is not subject to production test.

10.5 Timing Parameters by Speed Grade

10.5.1 Timing Parameters by Speed Bin for DDR4-1600 to 2400

Table 56 - Timing Parameters by Speed Bin for DDR4-1600 to 2400

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Clock Timing											
Minimum Clock Cycle Time (DLL off mode)	$t_{CK(DLL\_OFF)}$	8	20	8	20	8	20	8	20	ns	-
Average Clock Period	$t_{CK\ (avg)}$	1.25	<1.5	1.071	<1.25	0.937	<1.071	0.833	<0.937	ns	35,36
Average high pulse width	$t_{CH\ (avg)}$	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	$t_{CK\ (avg)}$	-
Average low pulse width	$t_{CL\ (avg)}$	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	$t_{CK\ (avg)}$	-
Absolute Clock Period	$t_{CK\ (abs)}$	Min: $t_{CK\ (avg)min} + t_{JIT\ (per)min\_tot}$								$t_{CK\ (avg)}$	-
		Max: $t_{CK\ (avg)max} + t_{JIT\ (per)max\_tot}$									
Absolute clock HIGH pulse width	$t_{CH\ (abs)}$	0.45	-	0.45	-	0.45	-	0.45	-	$t_{CK\ (avg)}$	23
Absolute clock LOW pulse width	$t_{CL\ (abs)}$	0.45	-	0.45	-	0.45	-	0.45	-	$t_{CK\ (avg)}$	24
Clock Period Jitter- total	$t_{JIT\ (per)\_tot}$	-63	63	-54	54	-47	47	-42	42	ps	25
Clock Period Jitter- deterministic	$t_{JIT\ (per)\_dj}$	-31	31	-27	27	-23	23	-21	21	ps	26
Clock Period Jitter during DLL locking period	$t_{JIT\ (per,\ lck)}$	-50	50	-43	43	-38	38	-33	33	ps	-
Cycle to Cycle Period Jitter	$t_{JIT\ (cc)}$	-	125	-	107	-	94	-	83	ps	-
Cycle to Cycle Period Jitter during DLL locking period	$t_{JIT\ (cc,\ lck)}$	-	100	-	86	-	75	-	67	ps	-
Cumulative error across 2 cycles	$t_{ERR\ (2per)}$	-92	92	-79	79	-69	69	-61	61	ps	-
Cumulative error across 3 cycles	$t_{ERR\ (3per)}$	-109	109	-94	94	-82	82	-73	73	ps	-
Cumulative error across 4 cycles	$t_{ERR\ (4per)}$	-121	121	-104	104	-91	91	-81	81	ps	-
Cumulative error across 5 cycles	$t_{ERR\ (5per)}$	-131	131	-112	112	-98	98	-87	87	ps	-
Cumulative error across 6 cycles	$t_{ERR\ (6per)}$	-139	139	-119	119	-104	104	-92	92	ps	-
Cumulative error across 7 cycles	$t_{ERR\ (7per)}$	-145	145	-124	124	-109	109	-97	97	ps	-

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Cumulative error across 8 cycles	$t_{ERR\ (8per)}$	-151	151	-129	129	-113	113	-101	101	ps	-
Cumulative error across 9 cycles	$t_{ERR\ (9per)}$	-156	156	-134	134	-117	117	-104	104	ps	-
Cumulative error across 10 cycles	$t_{ERR\ (10per)}$	-160	160	-137	137	-120	120	-107	107	ps	-
Cumulative error across 11 cycles	$t_{ERR\ (11per)}$	-164	164	-141	141	-123	123	-110	110	ps	-
Cumulative error across 12 cycles	$t_{ERR\ (12per)}$	-168	168	-144	144	-126	126	-112	112	ps	-
Cumulative error across 13 cycles	$t_{ERR\ (13per)}$	-172	172	-147	147	-129	129	-114	114	ps	-
Cumulative error across 14 cycles	$t_{ERR\ (14per)}$	-175	175	-150	150	-131	131	-116	116	ps	-
Cumulative error across 15 cycles	$t_{ERR\ (15per)}$	-178	178	-152	152	-133	133	-118	118	ps	-
Cumulative error across 16 cycles	$t_{ERR\ (16per)}$	-180	189	-155	155	-135	135	-120	120	ps	-
Cumulative error across 17 cycles	$t_{ERR\ (17per)}$	-183	183	-157	157	-137	137	-122	122	ps	-
Cumulative error across 18 cycles	$t_{ERR\ (18per)}$	-185	185	-159	159	-139	139	-124	124	ps	-
Cumulative error across n = 13, 14 . . . 49, 50 cycles	$t_{ERR\ (nper)}$	$t_{ERR\ (nper)min} = ((1 + 0.68ln(n)) * t_{JIT\ (per)\_total\ min})$								ps	-
		$t_{ERR\ (nper)max} = ((1 + 0.68ln(n)) * t_{JIT\ (per)\_total\ max})$									
Command and Address setup time to CK_t, CK_c referenced to $V_{IH(AC)}/V_{IL(AC)}$ levels	$t_{IS\ (base)}$	115	-	100	-	80	-	62	-	ps	-
Command and Address setup time to CK_t, CK_c referenced to V_{REF} levels	$t_{IS\ (VREF)}$	215	-	200	-	180	-	162	-	ps	-
Command and Address hold time to CK_t, CK_c referenced to $V_{IH(DC)}/V_{IL(DC)}$ levels	$t_{IH\ (base)}$	140	-	125	-	105	-	87	-	ps	-
Command and Address hold time to CK_t, CK_c referenced to V_{REF} levels	$t_{IH\ (VREF)}$	215	-	200	-	180	-	162	-	ps	-
Control and Address Input pulse width for each input	t_{IPW}	600	-	525	-	460	-	410	-	ps	-
Command and Address Timing											

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
CAS_n to CAS_n command delay for same bank group	t_{CCD_L}	Max (5nCK,6.250ns)	-	Max (5nCK,5.355ns)	-	Max (5nCK,5.355ns)	-	Max (5nCK, 5ns)	-	nCK	34
CAS_n to CAS_n command delay for different bank group	t_{CCD_S}	4	-	4	-	4	-	4	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	$t_{RRD\_S\ (2K)}$	Max (4nCK, 6ns)	-	Max (4nCK, 5.3ns)	-	Max (4nCK, 5.3ns)	-	Max (4nCK, 5.3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 1KB page size	$t_{RRD\_S\ (1K)}$	Max (4nCK, 5ns)	-	Max (4nCK, 4.2ns)	-	Max (4nCK, 3.7ns)	-	Max (4nCK, 3.3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 1/2KB page size	$t_{RRD\_S\ (1/2K)}$	Max (4nCK, 5.0ns)	-	Max (4nCK, 4.2ns)	-	Max (4nCK, 3.7ns)	-	Max (4nCK, 3.3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	$t_{RRD\_L\ (2K)}$	Max (4nCK, 7.5ns)	-	Max (4nCK, 6.4ns)	-	Max (4nCK, 6.4ns)	-	Max (4nCK, 6.4ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	$t_{RRD\_L\ (1K)}$	Max (4nCK, 6.0ns)	-	Max (4nCK, 5.3ns)	-	Max (4nCK, 5.3ns)	-	Max (4nCK, 4.9ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	$t_{RRD\_L\ (1/2K)}$	Max (4nCK, 6.0ns)	-	Max (4nCK, 5.3ns)	-	Max (4nCK, 5.3ns)	-	Max (4nCK, 4.9ns)	-	nCK	34
Four activate window for 2KB page size	$t_{FAW\ (2K)}$	Max (28nCK, 35ns)	-	Max (28nCK, 30ns)	-	Max (28nCK, 30ns)	-	Max (28nCK, 30ns)	-	ns	34
Four activate window for 1KB page size	$t_{FAW\ (1K)}$	Max (20nCK, 25ns)	-	Max (20nCK, 23ns)	-	Max (20nCK, 21ns)	-	Max (20nCK, 21ns)	-	ns	34
Four activate window for 1/2KB page size	$t_{FAW\ (1/2K)}$	Max (16nCK, 20ns)	-	Max (16nCK, 17ns)	-	Max (16nCK, 15ns)	-	Max (16nCK, 13ns)	-	ns	34
Delay from start of internal WRITE transaction to internal READ command for different bank group	t_{WTR_S}	Max (2nCK,2.5ns)	-	Max (2nCK, 2.5ns)	-	Max (2nCK, 2.5ns)	-	Max (2nCK, 2.5ns)	-	ns	1, 2, 34

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Delay from start of internal WRITE transaction to internal READ command for same bank group	t_{WTR_L}	Max (4nCK, 7.5ns)	-	Max (4nCK, 7.5ns)	-	Max (4nCK, 7.5ns)	-	Max (4nCK, 7.5ns)	-	ns	1, 34
Internal READ command to PRECHARGE command delay	t_{RTP}	Max (4nCK, 7.5ns)	-	Max (4nCK, 7.5ns)	-	Max (4nCK, 7.5ns)	-	Max (4nCK, 7.5ns)	-	ns	-
WRITE recovery time	t_{WR}	15	-	15	-	15	-	15	-	ns	1
Write recovery time when CRC and DM are enabled	$t_{WR\_CRC\_DM}$	t_{WR} + Max (4nCK, 3.75ns)	-	t_{WR} + Max (5nCK, 3.75ns)	-	t_{WR} + Max (5nCK, 3.75ns)	-	t_{WR} + Max (5nCK, 3.75ns)	-	ns	1, 28
Delay from start of internal WRITE transaction to internal READ command for different bank group with both CRC and DM enabled	$t_{WTR\_S\_CRC\_DM}$	t_{WTR_S} + Max (4nCK, 3.75ns)	-	t_{WTR_S} + Max (5nCK, 3.75ns)	-	t_{WTR_S} + Max (5nCK, 3.75ns)	-	t_{WTR_S} + Max (5nCK, 3.75ns)	-	ns	2,,29, 34
Delay from start of internal WRITE transaction to internal READ command for same bank group with both CRC and DM enabled	$t_{WTR\_L\_CRC\_DM}$	t_{WTR_L} + Max (4nCK, 3.75ns)	-	t_{WTR_L} + Max (5nCK, 3.75ns)	-	t_{WTR_L} + Max (5nCK, 3.75ns)	-	t_{WTR_L} + Max (5nCK, 3.75ns)	-	ns	3, 30, 34
DDL locking time	t_{DLLK}	597	-	597	-	768	-	768	-	nCK	-
MODE REGISTER SET command cycle time	t_{MRD}	8	-	8	-	8	-	8	-	nCK	-
MODE REGISTER SET command update delay	t_{MOD}	Max (24nCK, 15ns)	-	Max (24nCK, 15ns)	-	Max (24nCK, 15ns)	-	Max (24nCK, 15ns)	-	nCK	50
Mult-Purpose Register Recovery Time	t_{MPRR}	1	-	1	-	1	-	1	-	nCK	33
Mult-Purpose Register Write Recovery Time	t_{WR_MPR}	$t_{MOD\ (min)}$ +AL + PL	-	$t_{MOD\ (min)}$ +AL + PL	-	$t_{MOD\ (min)}$ +AL + PL	-	$t_{MOD\ (min)}$ +AL + PL	-	ns	-
Auto precharge write recovery + precharge time	$t_{DAL\ (min)}$	Programmed WR + roundup ($t_{RP}/t_{CK\ (avg)}$)								nCK	-
DQ0 or DQL0 driven to set-up time to first DQS rising edge	t_{PDA_S}	0.5	-	0.5	-	0.5	-	0.5	-	UI	45, 47
DQ0 or DQL0 driven to hold time from last DQS falling edge	t_{PDA_H}	0.5	-	0.5	-	0.5	-	0.5	-	UI	46, 47

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
CS_n to Command Address Latency											
CS_n to Command Address Latency	t_{CAL}	Max (3nCK, 3.748ns)	-	Max (3nCK, 3.748ns)	-	Max (3nCK, 3.748ns)	-	Max (3nCK, 3.748ns)	-	nCK	-
MODE REGISTER SET command cycle time in CAL mode	t_{MRD_CAL}	$t_{MOD} + t_{CAL}$	-	$t_{MOD} + t_{CAL}$	-	$t_{MOD} + t_{CAL}$	-	$t_{MOD} + t_{CAL}$	-	nCK	-
MODE REGISTER SET update delay in CAL mode	t_{MOD_CAL}	$t_{MOD} + t_{CAL}$	-	$t_{MOD} + t_{CAL}$	-	$t_{MOD} + t_{CAL}$	-	$t_{MOD} + t_{CAL}$	-	nCK	-
DRAM Data Timing											
DQS_t, DQS_c to DQ skew, per group, per acces	t_{DQSQ}	-	0.16	-	0.16	-	0.16	-	0.17	$t_{CK\ (avg)}/2$	13,18,39, 49
DQ output hold time from DQS_t, DQS_c	t_{QH}	0.76	-	0.76	-	0.76	-	0.74	-	$t_{CK\ (avg)}/2$	13,17,18, 39,49
Data Valid Window per device per UI: (t_{QH} - t_{DQSQ}) of each UI on a given DRAM	t_{DVWd}	0.63	-	0.63	-	0.64	-	0.64	-	UI	17,18,39, 49
Data Valid Window per pin per UI: (t_{QH} - t_{DQSQ}) each UI on a pin of a given DRAM	t_{DVWp}	0.66	-	0.66	-	0.69	-	0.72	-	UI	17,18,39, 49
DQ low impedance time from CK_t, CK_c	$t_{LZ\ (DQ)}$	-450	225	-390	195	-360	180	-330	175	ps	39
DQ high impedance time from CK_t, CK_c	$t_{HZ\ (DQ)}$	-	225	-	195	-	180	-	175	ps	39
Data Strobe Timing											
DQS_t, DQS_c differential READ Preamble (1 clock preamble)	t_{RPRE}	0.9	Note 44	0.9	Note 44	0.9	Note 44	0.9	Note 44	nCK	39,40
DQS_t, DQS_c differential READ Preamble (2 clock preamble)	t_{RPRE2}	N/A	N/A	NA	N/A	N/A	N/A	1.8	Note 44	t_{CK}	39,41
DQS_t, DQS_c differential READ Postamble	t_{RPST}	0.33	Note	0.33	Note	0.33	Note	0.33	Note	t_{CK}	39

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
DQS_t, DQS_c differential output high time	t_{QSH}	0.4	-	0.4	-	0.4	-	0.4	-	t_{CK}	21,39
DQS_t, DQS_c differential output low time	t_{QSL}	0.4	-	0.4	-	0.4	-	0.4	-	t_{CK}	20,39
DQS_t, DQS_c differential WRITE Preamble (1 clock preamble)	t_{WPRE}	0.9	-	0.9	-	0.9	-	0.9	-	t_{CK}	42
DQS_t, DQS_c differential WRITE Preamble (2 clock preamble)	t_{WPRE2}	NA	NA	NA	NA	NA	NA	1.8	-	t_{CK}	43
DQS_t, DQS_c differential WRITE Postamble	t_{WPST}	0.33	-	0.33	-	0.33	-	0.33	-	t_{CK}	-
DQS_t and DQS_c low-impedance time (Referenced from RL - 1)	$t_{LZ\ (DQS)}$	-450	225	-390	195	-360	180	-330	175	ps	39
DQS_t and DQS_c high-impedance time (Referenced from RL + BL/2)	$t_{HZ\ (DQS)}$	-	225	-	195	-	180	-	175	ps	39
DQS_t, DQS_c differential input low pulse width	t_{DQSL}	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	t_{CK}	-
DQS_t, DQS_c differential input high pulse width	t_{DQSH}	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	t_{CK}	-
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (1 clock preamble)	t_{DQSS}	-0.27	0.27	-0.27	0.27	-0.27	0.27	-0.27	0.27	t_{CK}	42
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (2 clock preamble)	t_{DQSS2}	N/A	N/A	N/A	N/A	N/A	N/A	-0.5	0.5	-	43
DQS_t, DQS_c falling edge setup time to CK_t, CK_c rising edge	t_{DSS}	0.18	-	0.18	-	0.18	-	0.18	-	t_{CK}	-
DQS_t, DQS_c falling edge hold time from CK_t, CK_c rising edge	t_{DSH}	0.18	-	0.18	-	0.18	-	0.18	-	t_{CK}	-
DQS_t, DQS_c rising edge output variance window per DRAM	$t_{DQSCKI\ (DLL\ On)}$	-	370	-	330	-	310	-	290	ps	37,38,39

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
DQS_t, DQS_c rising edge output timing location from rising CK_t, CK_c with DDL on mode	$t_{DQSCK\ (DLL\ On)}$	-225	225	-195	195	-180	180	-175	175	ps	37,38,39
MPSM Timing											
Command path disable delay upon MPSM entry	t_{MPED}	$t_{MOD\ (min)} + t_{CPDED\ (min)}$								tCK	-
Valid clock requirement after MPSM entry	t_{CKMPE}	$t_{MOD\ (min)} + t_{CPDED\ (min)}$								tCK	-
Valid clock requirement before MPSM exit	t_{CKMPX}	$t_{CKSRX\ (min)}$								tCK	-
Exit MPSM to commands not requiring a locked DLL	t_{XMP}	$t_{XS\ (min)}$								tCK	-
Exit MPSM to commands requiring a locked DLL	t_{XMPDLL}	$t_{XMP\ (min)} + t_{XSDLL\ (min)}$								tCK	-
CS setup time to CKE	t_{MPX_S}	$t_{IS\ (min)} + t_{IH\ (min)}$								ns	-
Calibration Timing											
Power-up and RESET calibration time	t_{ZQinit}	1024	-	1024	-	1024	-	1024	-	nCK	-
Normal operation Full calibration time	t_{ZQoper}	512	-	512	-	512	-	512	-	nCK	-
Normal operation short calibration Short calibration time	t_{ZQCS}	128	-	128	-	128	-	128	-	nCK	-
Reset/Self Refresh Timing											
Exit reset from CKE HIGH to a valid command	t_{XPR}	Max (5nCK, $t_{RFC\ (min)}$ + 10ns)	-	Max (5nCK, $t_{RFC\ (min)}$ + 10ns)	-	Max (5nCK, $t_{RFC\ (min)}$ + 10ns)	-	Max (5nCK, $t_{RFC\ (min)}$ + 10ns)	-	nCK	-
Exit self refresh to commands not requiring a locked DLL	t_{XS}	$t_{RFC4\ (min)}$ + 10ns	-	$t_{RFC4\ (min)}$ + 10ns	-	$t_{RFC4\ (min)}$ + 10ns	-	$t_{RFC4\ (min)}$ + 10ns	-	nCK	-

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
SRX to Commands not requiring a locked DLL in self refresh abort	$t_{XS\_ABORT\ (min)}$	$t_{RFC4\ (min)}$ + 10ns	-	$t_{RFC4\ (min)}$ + 10ns	-	$t_{RFC4\ (min)}$ + 10ns	-	$t_{RFC4\ (min)}$ + 10ns	-	nCK	-
Exit self refresh to ZQCL, ZQCS and MRS (CL, CWL, WR, RTP and Gear Down)	$t_{XS\_FAST\ (min)}$	$t_{RFC4\ (min)}$ + 10ns	-	$t_{RFC4\ (min)}$ + 10ns	-	$t_{RFC4\ (min)}$ + 10ns	-	$t_{RFC4\ (min)}$ + 10ns	-	nCK	-
Exit self refresh to commands requiring a locked DLL	t_{XSDLL}	$t_{DLLK\ (min)}$	-	$t_{DLLK\ (min)}$	-	$t_{DLLK\ (min)}$	-	$t_{DLLK\ (min)}$	-	nCK	-
Minimum CKE low width for self refresh entry to exit timing	t_{CKESR}	$t_{CKE\ (min)}$ + 1nCK	-	$t_{CKE\ (min)}$ + 1nCK	-	$t_{CKE\ (min)}$ + 1nCK	-	$t_{CKE\ (min)}$ + 1nCK	-	nCK	-
Minimum CKE low width for self refresh entry to exit timing with CA Parity enabled	t_{CKESR_PAR}	$t_{CKE\ (min)}$ +1nCK + PL	-	$t_{CKE\ (min)}$ +1nCK + PL	-	$t_{CKE\ (min)}$ +1nCK + PL	-	$t_{CKE\ (min)}$ +1nCK + PL	-	nCK	-
Valid Clock Requirement after self refresh Entry (SRE) or Power-Down Entry (PDE)	t_{CKSRE}	Max (5nCK, 10ns)	-	Max (5nCK, 10ns)	-	Max (5nCK, 10ns)	-	Max (5nCK, 10ns)	-	nCK	-
Valid Clock Requirement after self refresh Entry (SRE) or Power-Down when CA Parity is enabled	t_{cksre_PAR}	Max (5nCK, 10ns) + PL	-	Max (5nCK, 10ns) +PL	-	Max (5nCK, 10ns) +PL	-	Max (5nCK, 10ns) +PL	-	nCK	-
Valid Clock Requirement before self refresh Exit (SRX) or Power Down Exit (PDX) or Reset Exit	t_{CKSRX}	Max (5nCK, 10ns)	-	Max (5nCK, 10ns)	-	Max (5nCK, 10ns)	-	Max (5nCK, 10ns)	-	nCK	-
Power Down Timing											
Exit power-down with DLL on to any valid command, Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	t_{XP}	Max (4nCK, 6ns)	-	Max (4nCK, 6ns)	-	Max (4nCK, 6ns)	-	Max (4nCK, 6ns)	-	nCK	-
CKE minimum pulse width	t_{CKE}	Max (3nCK, 5ns)	-	Max (3nCK, 5ns)	-	Max (3nCK, 5ns)	-	Max (3nCK, 5ns)	-	nCK	31,32
Command pass disable delay	t_{CPDED}	4	-	4	-	4	-	4	-	nCK	-
Power Down Entry to Exit Timing	t_{PD}	$t_{CKE\ (min)}$	9 * t_{REFI}	$t_{CKE\ (min)}$	9 * t_{REFI}	$t_{CKE\ (min)}$	9 * t_{REFI}	$t_{CKE\ (min)}$	9 * t_{REFI}	nCK	6

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Timing of ACT command to Power Down entry	$t_{ACTPDEN}$	1	-	1	-	2	-	2	-	nCK	7
Timing of PRE or PREA command to Power Down entry	t_{PRPDEN}	1	-	1	-	2	-	2	-	nCK	7
Timing of RD/RDA command to Power Down entry	t_{RDPDEN}	RL + 4 + 1	-	RL + 4 + 1	-	RL + 4 + 1	-	RL + 4 + 1	-	nCK	-
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	t_{WRPDEN}	WL + 4 + ($t_{WR}/t_{CK\ (avg)}$)	-	WL + 4 + ($t_{WR}/t_{CK\ (avg)}$)	-	WL + 4 + ($t_{WR}/t_{CK\ (avg)}$)	-	WL + 4 + ($t_{WR}/t_{CK\ (avg)}$)	-	nCK	4
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	$t_{WRAPDEN}$	WL + 4 + WR + 1	-	WL + 4 + WR + 1	-	WL + 4 + WR + 1	-	WL + 4 + WR + 1	-	nCK	5
Timing of WR command to Power Down entry (BC4MRS)	$t_{WRP-BC4DEN}$	WL + 2 + ($t_{WR}/t_{CK\ (avg)}$)	-	WL + 2 + ($t_{WR}/t_{CK\ (avg)}$)	-	WL + 2 + ($t_{WR}/t_{CK\ (avg)}$)	-	WL + 2 + ($t_{WR}/t_{CK\ (avg)}$)	-	nCK	4
Timing of WRA command to Power Down entry (BC4MRS)	$t_{WRAP-BC4DEN}$	WL + 2 + WR + 1	-	WL + 2 + WR + 1	-	WL + 2 + WR + 1	-	WL + 2 + WR + 1	-	nCK	5
Timing of REF command to Power Down entry	$t_{REFPDEN}$	1	-	1	-	2	-	2	-	nCK	7
Timing of MRS command to Power Down entry	$t_{MRSPDEN}$	$t_{MOD\ (min)}$	-	$t_{MOD\ (min)}$	-	$t_{MOD\ (min)}$	-	$t_{MOD\ (min)}$	-	nCK	-
PDA Timing											
MODE REGISTER SET command cycle time in PDA mode	t_{MRD_PDA}	Max (16nCK, 10ns)	-	Max (16nCK, 10ns)	-	Max (16nCK, 10ns)	-	Max (16nCK, 10ns)	-	nCK	-
MODE REGISTER SET command update delay in PDA mode	t_{MOD_PDA}	t_{MOD}		t_{MOD}		t_{MOD}		t_{MOD}		nCK	-
ODT Timing											
Asynchronous R_{TT} turn-on delay (Power-Down with DLL frozen)	t_{AONAS}	1	9	1	9	1	9	1	9	ns	-

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Asynchronous R_{TT} turn-off delay (Power-Down with DLL frozen)	t_{AOFAS}	1	9	1	9	1	9	1	9	ns	-
R_{TT} dynamic change skew	t_{ADC}	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	$t_{CK\ (avg)}$	-
Write Leveling Timing											
First DQS_t/DQS_c rising edge after write leveling mode is programmed	t_{WLMRD}	40	-	40	-	40	-	40	-	nCK	12
DQS_t/DQS_c delay after write leveling mode is programmed	$t_{WLDQSEN}$	25	-	25	-	25	-	25	-	nCK	12
Write leveling setup time from rising CK_t, CK_c crossing to rising DQS_t/DQS_c crossing	t_{WLS}	0.13	-	0.13	-	0.13	-	0.13	-	$t_{CK\ (avg)}$	-
Write leveling hold time from rising DQS_t/DQS_c crossing to rising CK_t, CK_crossing	t_{WLH}	0.13	-	0.13	-	0.13	-	0.13	-	$t_{CK\ (avg)}$	-
Write leveling output delay	t_{WLO}	0	9.5	0	9.5	0	9.5	0	9.5	ns	-
Write leveling output error	t_{WLOE}	0	2	0	2	0	2	0	2	ns	-
CA Parity Timing											
Commands not guaranteed to be executed during this time	$t_{PAR\_UNKNOWN}$	-	PL	-	PL	-	PL	-	PL	nCK	-
Delay from errant command to ALERT_n assertion	$t_{PAR\_ALERT\_ON}$	-	PL + 6ns	-	PL + 6ns	-	PL + 6ns	-	PL + 6ns	nCK	-
Pulse width of ALERT_n signal when asserted	$t_{PAR\_ALERT\_PW}$	48	96	56	112	64	128	72	144	nCK	-
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	$t_{PAR\_ALERT\_RSP}$	-	43	-	50	-	57	-	64	nCK	-

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Parity Latency	PL	4		4		4		5		nCK	-
CRC Error Reporting											
CRC error to ALERT_n latency	t_{CRC_ALERT}	3	13	3	13	3	13	3	13	ns	-
CRC ALERT_n pulse width	$t_{CRC\_ALERT\_PW}$	6	10	6	10	6	10	6	10	nCK	-
t_{REFI}											
$t_{RFC1\ (min)}$	8Gb	260	-	260	-	260	-	260	-	ns	tRFC1 (min)
$t_{RFC2\ (min)}$	8Gb	160	-	160	-	160	-	160	-	ns	tRFC2 (min)
$t_{RFC4\ (min)}$	8Gb	110	-	110	-	110	-	110	-	ns	tRFC4 (min)

10.5.2 Timing Parameters by Speed Bin for DDR4-2666 to 3200

Table 57 - Timing Parameters by Speed Bin for DDR4-2666 to 3200

Speed		DDR4-2666		DDR4-2933		DDR4-3200		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
Clock Timing									
Minimum Clock Cycle Time (DLL off mode)	$t_{CK\ (DLL\_OFF)}$	8	20	8	20	8	20	ns	-
Average Clock Period	$t_{CK\ (avg)}$	0.75	<0.833	0.682	<0.750	0.625	<0.682	ns	35,36
Average high pulse width	$t_{CH\ (avg)}$	0.48	0.52	0.48	0.52	0.48	0.52	$t_{CK\ (avg)}$	-
Average low pulse width	$t_{CL\ (avg)}$	0.48	0.52	0.48	0.52	0.48	0.52	$t_{CK\ (avg)}$	-
Absolute Clock Period	$t_{CK\ (abs)}$	Min = $t_{CK\ (avg)min}$ + $t_{JIT(per)min\_tot}$						$t_{CK\ (avg)}$	-
		Max = $t_{CK\ (avg)max}$ + $t_{JIT(per)max\_tot}$							
Absolute clock HIGH pulse width	$t_{CH\ (abs)}$	0.45	-	0.45	-	0.45	-	$t_{CK\ (avg)}$	23
Absolute clock LOW pulse width	$t_{CL\ (abs)}$	0.45	-	0.45	-	0.45	-	$t_{CK\ (avg)}$	24
Clock Period Jitter-total	$t_{JIT\ (per)\_tot}$	-38	38	-34	34	-32	32	ps	25
Clock Period Jitter-deterministic	$t_{JIT\ (per)\_dj}$	-19	19	-17	17	-16	16	ps	26

Speed		DDR4-2666		DDR4-2933		DDR4-3200		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
Clock Period Jitter during DLL locking period	$t_{JIT\ (per,\ lck)}$	-30	30	-27	27	-25	25	ps	-
Cycle to Cycle Period Jitter	$t_{JIT\ (cc)}$	-	75	-	68	-	62	ps	25
Cycle to Cycle Period Jitter during DLL locking period	$t_{JIT\ (cc,\ lck)}$	-	60	-	55	-	50	ps	-
Cumulative error across 2 cycles	$t_{ERR\ (2per)}$	-55	55	-50	50	-46	46	ps	-
Cumulative error across 3 cycles	$t_{ERR\ (3per)}$	-66	66	-60	60	-55	55	ps	-
Cumulative error across 4 cycles	$t_{ERR\ (4per)}$	-73	73	-66	66	-61	61	ps	-
Cumulative error across 5 cycles	$t_{ERR\ (5per)}$	-78	78	-71	71	-65	65	ps	-
Cumulative error across 6 cycles	$t_{ERR\ (6per)}$	-83	83	-75	75	-69	69	ps	-
Cumulative error across 7 cycles	$t_{ERR\ (7per)}$	-87	87	-79	79	-73	73	ps	-
Cumulative error across 8 cycles	$t_{ERR\ (8per)}$	-91	91	-83	83	-76	76	ps	-
Cumulative error across 9 cycles	$t_{ERR\ (9per)}$	-94	94	-85	85	-78	78	ps	-
Cumulative error across 10 cycles	$t_{ERR\ (10per)}$	-96	96	-88	88	-80	80	ps	-
Cumulative error across 11 cycles	$t_{ERR\ (11per)}$	-99	99	-90	90	-83	83	ps	-
Cumulative error across 12 cycles	$t_{ERR\ (12per)}$	-101	101	-92	92	-84	84	ps	-
Cumulative error across 13 cycles	$t_{ERR\ (13per)}$	-103	103	-93	93	-86	86	ps	-
Cumulative error across 14 cycles	$t_{ERR\ (14per)}$	-104	104	-95	95	-87	87	ps	-
Cumulative error across 15 cycles	$t_{ERR\ (15per)}$	-106	106	-97	97	-89	89	ps	-
Cumulative error across 16 cycles	$t_{ERR\ (16per)}$	-108	108	-98	98	-90	90	ps	-
Cumulative error across 17 cycles	$t_{ERR\ (17per)}$	-110	110	-100	100	-92	92	ps	-
Cumulative error across 18 cycles	$t_{ERR\ (18per)}$	-112	112	-101	101	-93	93	ps	-
Cumulative error across n = 13, 14 . . . 49, 50 cycles	$t_{ERR\ (nper)}$	$t_{ERR\ (nper)min} = ((1 + 0.68ln(n)) * t_{JIT\ (per)\_total\ min})$						ps	-
		$t_{ERR\ (nper)max} = ((1 + 0.68ln(n)) * t_{JIT\ (per)\_total\ max})$							
Command and Address setup time to CK_t, CK_c referenced to $V_{IH(AC)}/V_{IL(AC)}$ levels	$t_{IS\ (base)}$	55	-	48	-	40	-	ps	-

Speed		DDR4-2666		DDR4-2933		DDR4-3200		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
Command and Address setup time to CK_t, CK_c referenced to V_{REF} levels	$t_{IS\ (V_{REF})}$	145	-	138	-	130	-	ps	-
Command and Address hold time to CK_t, CK_c referenced to $V_{IH(DC)}/V_{IL(DC)}$ levels	$t_{IH\ (base)}$	80	-	73	-	65	-	ps	-
Command and Address hold time to CK_t, CK_c referenced to V_{REF} levels	$t_{IH\ (V_{REF})}$	145	-	138	-	130	-	ps	-
Control and Address Input pulse width for each input	t_{IPW}	385	-	365	-	340	-	ps	-
Command and Address Timing-									
CAS_n to CAS_n command delay for same bank group	t_{CCD_L}	Max (5nCK, 5ns)	-	Max (5nCK, 5ns)	-	Max (5nCK, 5ns)	-	nCK	34
CAS_n to CAS_n command delay for different bank group	t_{CCD_S}	4	-	4	-	4	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	$t_{RRD\_S\ (2K)}$	Max (4nCK, 5.3ns)	-	Max (4nCK, 5.3ns)	-	Max (4nCK, 5.3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 1KB page size	$t_{RRD\_S\ (1K)}$	Max (4nCK, 3ns)	-	Max (4nCK, 2.7ns)	-	Max (4nCK, 2.5ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 1/2KB page size	$t_{RRD\_S\ (1/2K)}$	Max (4nCK, 3ns)	-	Max (4nCK, 2.7ns)	-	Max (4nCK, 2.5ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	$t_{RRD\_L\ (2K)}$	Max (4nCK, 6.4ns)	-	Max (4nCK, 6.4ns)	-	Max (4nCK, 6.4ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	$t_{RRD\_L\ (1K)}$	Max (4nCK, 4.9ns)	-	Max (4nCK, 4.9ns)	-	Max (4nCK, 4.9ns)	-	nCK	34

Speed		DDR4-2666		DDR4-2933		DDR4-3200		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	$t_{RRD\_L\ (1/2K)}$	Max (4nCK, 4.9ns)	-	Max (4nCK, 4.9ns)	-	Max (4nCK, 4.9ns)	-	nCK	34
Four activate window for 2KB page size	$t_{FAW\ (2K)}$	Max (28nCK,30ns)	-	Max (28nCK,30ns)	-	Max (28nCK,30ns)	-	ns	34
Four activate window for 1KB page size	$t_{FAW\ (1K)}$	Max (20nCK,21ns)	-	Max (20nCK,21ns)	-	Max (20nCK,21ns)	-	ns	34
Four activate window for 1/2KB page size	$t_{FAW\ (1/2K)}$	Max (16nCK,13ns)	-	Max (16nCK,12ns)	-	Max (16nCK,10ns)	-	ns	34
Delay from start of internal WRITE transaction to internal READ command for different bank group	t_{WTR_S}	Max (2nCK, 2.5ns)	-	Max (2nCK, 2.5ns)	-	Max (2nCK, 2.5ns)	-	ns	1, 2, 34
Delay from start of internal WRITE transaction to internal READ command for same bank group	t_{WTR_L}	Max (4nCK, 7.5ns)	-	Max (4nCK, 7.5ns)	-	Max (4nCK, 7.5ns)	-	ns	1, 34
Internal READ Command to PRCHARGE command delay	t_{RTP}	Max (4nCK, 7.5ns)	-	Max (4nCK, 7.5ns)	-	Max (4nCK, 7.5ns)	-	ns	-
WRITE recovery time	t_{WR}	15	-	15	-	15	-	ns	1
Write recovery time when CRC and DM are enabled	$t_{WR\_CRC\_DM}$	t_{WR} + Max (5nCK, 3.75ns)	-	t_{WR} + Max (5nCK, 3.75ns)	-	t_{WR} + Max (5nCK, 3.75ns)	-	ns	1, 28
Delay from start of internal WRITE transaction to internal READ command for different bank group with both CRC and DM enabled	$t_{WTR\_S\_CRC\_DM}$	t_{WTR_S} + Max (5nCK, 3.75ns)	-	t_{WTR_S} + Max (5nCK, 3.75ns)	-	t_{WTR_S} + Max (5nCK, 3.75ns)	-	ns	2, 29, 34
Delay from start of internal WRITE transaction to internal READ command for same bank group with both CRC and DM enabled	$t_{WTR\_L\_CRC\_DM}$	t_{WTR_L} + Max (5nCK, 3.75ns)	-	t_{WTR_L} + Max (5nCK, 3.75ns)	-	t_{WTR_L} + Max (5nCK, 3.75ns)	-	ns	3, 30, 34
DDL locking time	t_{DLLK}	1024	-	1024	-	1024	-	nCK	-
MODE REGISTER SET command cycle time	t_{MRD}	8	-	8	-	8	-	nCK	-

Speed		DDR4-2666		DDR4-2933		DDR4-3200		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
MODE REGISTER SET command update delay	t_{MOD}	Max (24nCK,15ns)	-	Max (24nCK,15ns)	-	Max (24nCK,15ns)	-	nCK	-
Mult-Purpose Register Recovery Time	t_{MPRR}	1	-	1	-	1	-	nCK	33
Mult-Purpose Register Write Recovery Time	t_{WR_MPR}	$t_{MOD\ (min)}$ + AL + PL	-	$t_{MOD\ (min)}$ + AL + PL	-	$t_{MOD\ (min)}$ + AL + PL	-	nCK	-
Auto precharge write recovery + precharge time	$t_{DAL\ (min)}$	Programmed WR + roundup ($t_{RP}/t_{CK\ (avg)}$)						nCK	-
DQ0 or DQL0 driven to set-up time to first DQS rising edge	t_{PDA_S}	0.5	-	0.5	-	0.5	-	UI	45, 47
DQ0 or DQL0 driven to hold time from last DQS falling edge	t_{PDA_H}	0.5	-	0.5	-	0.5	-	UI	46, 47
CS_n to Command Address Latency									
CS_n to Command Address Latency	t_{CAL}	Max (3nCK, 3.748ns)	-	Max (3nCK, 3.748ns)	-	Max (3nCK, 3.748ns)	-	nCK	-
MODE REGISTER SET command cycle time in CAL mode	t_{MRD_tCAL}	t_{MOD} + t_{CAL}	-	t_{MOD} + t_{CAL}	-	t_{MOD} + t_{CAL}	-	nCK	-
MODE REGISTER SET update delay in CAL mode	t_{MOD_tCAL}	t_{MOD} + t_{CAL}	-	t_{MOD} + t_{CAL}	-	t_{MOD} + t_{CAL}	-	nCK	-
DRAM Data Timing									
DQS_t, DQS_c to DQ skew, per group, per acces	t_{DQSQ}	-	0.18	-	0.19	-	0.20	$t_{CK\ (avg)}/2$	13,18,39,49
DQ output hold time from DQS_t, DQS_c	t_{QH}	0.74	-	0.72	-	0.70	-	$t_{CK\ (avg)}/2$	17,18,39,49
Data Valid Window per device per UI: (t_{QH} - t_{DQSQ}) of each UI on a given DRAM	t_{DVWd}	0.64	-	0.64	-	0.64	-	$t_{CK\ (avg)}/2$	-
Data Valid Window per pin per UI: (t_{QH} - t_{DQSQ}) each UI on a pin of a given DRAM	t_{DVWp}	0.72	-	0.72	-	0.72	-	$t_{CK\ (avg)}/2$	-

Speed		DDR4-2666		DDR4-2933		DDR4-3200		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
DQ low impedance time from CK_t, CK_c	$t_{LZ\ (DQ)}$	-310	170	-280	165	-250	160	$t_{CK(avg)}$ /2	-
DQ high impedance time from CK_t, CK_c	$t_{HZ\ (DQ)}$	-	170	-	165	-	160	$t_{CK(avg)}$ /2	-
Data Strobe Timing									
DQS_t, DQS_c differential READ Preamble (1 clock preamble)	t_{RPRE}	0.9	Note 44	0.9	Note 44	0.9	Note 44	t_{CK}	-
DQS_t, DQS_c differential READ Preamble (2 clock preamble)	t_{RPRE2}	1.8	Note 44	1.8	Note 44	1.8	Note 44	t_{CK}	-
DQS_t, DQS_c differential READ Postamble	t_{RPST}	0.33	Note 45	0.33	Note 45	0.33	Note 45	t_{CK}	-
DQS_t, DQS_c differential output high time	t_{QSH}	0.4	-	0.4	-	0.4	-	t_{CK}	21,39
DQS_t, DQS_c differential output low time	t_{QSL}	0.4	-	0.4	-	0.4	-	t_{CK}	20,39
DQS_t, DQS_c differential WRITE Preamble (1 clock preamble)	t_{WPRE}	0.9	-	0.9	-	0.9	-	t_{CK}	42
DQS_t, DQS_c differential WRITE Preamble (2 clock preamble)	t_{WPRE2}	1.8	-	1.8	-	1.8	-	t_{CK}	43
DQS_t, DQS_c differential WRITE Postamble	t_{WPST}	0.33	-	0.33	-	0.33	-	t_{CK}	-
DQS_t and DQS_c low-impedance time (Referenced from RL-1)	$t_{LZ\ (DQS)}$	-310	170	-280	165	-250	160	ps	39
DQS_t and DQS_c high-impedance time (Referenced from RL+BL/2)	$t_{HZ\ (DQS)}$	-	170	-	165	-	160	ps	39
DQS_t, DQS_c differential input low pulse width	t_{DQSL}	0.46	0.54	0.46	0.54	0.46	0.54	t_{CK}	-
DQS_t, DQS_c differential input high pulse width	t_{DQSH}	0.46	0.54	0.46	0.54	0.46	0.54	t_{CK}	-
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (1 clock preamble)	t_{DQSS}	-0.27	0.27	-0.27	0.27	-0.27	0.27	t_{CK}	42
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (2 clock preamble)	t_{DQSS2}	-0.50	0.50	-0.50	0.50	-0.50	0.50	t_{CK}	43

Speed		DDR4-2666		DDR4-2933		DDR4-3200		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
DQS_t, DQS_c falling edge setup time to CK_t, CK_c rising edge	t_{DSS}	0.18	-	0.18	-	0.18	-	t_{CK}	-
DQS_t, DQS_c falling edge hold time from CK_t, CK_c rising edge	t_{DSH}	0.18	-	0.18	-	0.18	-	t_{CK}	-
DQS_t, DQS_c rising edge output variance window per DRAM	$t_{DQSCKI\ (DLL\ On)}$	-	270	-	265	-	260	ps	37,38,39
DQS_t, DQS_c rising edge output timing location from rising CK_t, CK_c with DDL on mode	t_{DQSCK}	-170	170	-165	165	-160	160	ps	37,38,39
MPSM Timing									
Command path disable delay upon MPSM entry	t_{MPED}	$t_{MOD\ (min)}$ + $t_{CPDED\ (min)}$	-	$t_{MOD\ (min)}$ + $t_{CPDED\ (min)}$	-	$t_{MOD\ (min)}$ + $t_{CPDED\ (min)}$	-	t_{CK}	-
Valid clock requirement after MPSM entry	t_{CKMPE}	$t_{MOD\ (min)}$ + $t_{CPDED\ (min)}$	-	$t_{MOD\ (min)}$ + $t_{CPDED\ (min)}$	-	$t_{MOD\ (min)}$ + $t_{CPDED\ (min)}$	-	t_{CK}	-
Valid clock requirement before MPSM exit	t_{CKMPX}	$t_{CKSRX\ (min)}$	-	$t_{CKSRX\ (min)}$	-	$t_{CKSRX\ (min)}$	-	t_{CK}	-
Exit MPSM to commands not requiring a locked DLL	t_{XMP}	$t_{XS\ (min)}$	-	$t_{XS\ (min)}$	-	$t_{XS\ (min)}$	-	t_{CK}	-
Exit MPSM to commands requiring a locked DLL	t_{XMPDLL}	$t_{XMP\ (min)}$ + $t_{XSDLL\ (min)}$	-	$t_{XMP\ (min)}$ + $t_{XSDLL\ (min)}$	-	$t_{XMP\ (min)}$ + $t_{XSDLL\ (min)}$	-	t_{CK}	-
CS setup time to CKE	t_{MPX_S}	$t_{IS\ (min)}$ + $t_{IH\ (min)}$	-	$t_{IS\ (min)}$ + $t_{IH\ (min)}$	-	$t_{IS\ (min)}$ + $t_{IH\ (min)}$	-	ns	-
Calibration Timing									
Power-up and RESET calibration time	t_{ZQinit}	1024	-	1024	-	1024	-	nCK	-
Normal operation Full calibration time	t_{ZQoper}	512	-	512	-	512	-	nCK	-
Normal operation Short calibration time	t_{ZQCS}	128	-	128	-	128	-	nCK	-
Reset/Self Refresh Timing									

Speed		DDR4-2666		DDR4-2933		DDR4-3200		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
Exit reset from CKE HIGH to a valid command	t_{XPR}	Max (5nCK, $t_{RFC\ (min)}$ + 10ns)	-	Max (5nCK, $t_{RFC\ (min)}$ + 10ns)	-	Max (5nCK, $t_{RFC\ (min)}$ + 10ns)	-	nCK	-
Exit self refresh to commands not requiring a locked DLL	t_{XS}	$t_{RFC\ (min)}$ + 10ns	-	$t_{RFC\ (min)}$ + 10ns	-	$t_{RFC\ (min)}$ + 10ns	-	nCK	-
SRX to commands not requiring a locked DLL in self refresh abort	$t_{XS\_ABORT\ (min)}$	$t_{RFC4\ (min)}$ + 10ns	-	$t_{RFC4\ (min)}$ + 10ns	-	$t_{RFC4\ (min)}$ + 10ns	-	nCK	-
Exit self refresh to ZQCL, ZQCS and MRS (CL, CWL, WR, RTP and Gear Down)	$t_{XS\_FAST\ (min)}$	$t_{RFC4\ (min)}$ + 10ns	-	$t_{RFC4\ (min)}$ + 10ns	-	$t_{RFC4\ (min)}$ + 10ns	-	nCK	-
Exit self refresh to commands requiring a locked DLL	t_{XSDLL}	$t_{DLLK\ (min)}$	-	$t_{DLLK\ (min)}$	-	$t_{DLLK\ (min)}$	-	nCK	-
Minimum CKE low width for self refresh entry to exit timing	t_{CKESR}	$t_{CKE\ (min)}$ + 1nCK	-	$t_{CKE\ (min)}$ + 1nCK	-	$t_{CKE\ (min)}$ + 1nCK	-	nCK	-
Minimum CKE low width for self refresh entry to exit timing with CA Parity enabled	t_{CKESR_PAR}	$t_{CKE\ (min)}$ + 1nCK + PL	-	$t_{CKE\ (min)}$ + 1nCK + PL	-	$t_{CKE\ (min)}$ + 1nCK + PL	-	nCK	-
Valid Clock Requirement after self refresh Entry (SRE) or Power-Down Entry (PDE)	t_{CKSRE}	Max (5nCK, 10ns)	-	Max (5nCK, 10ns)	-	Max (5nCK, 10ns)	-	nCK	-
Valid Clock Requirement after self refresh Entry (SRE) or Power-Down when CA Parity is enabled	t_{cksre_PAR}	Max (5nCK, 10ns) + PL	-	Max (5nCK, 10ns) + PL	-	Max (5nCK, 10ns) + PL	-	nCK	-
Valid Clock Requirement before self refresh Exit (SRX) or Power Down Exit (PDX) or Reset Exit	t_{CKSRX}	Max (5nCK, 10ns)	-	Max (5nCK, 10ns)	-	Max (5nCK, 10ns)	-	nCK	-
Power Down Timing									
Exit Power Down with DLL on to any valid command,Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	t_{XP}	Max (4nCK, 6ns)	-	Max (4nCK, 6ns)	-	Max (4nCK, 6ns)	-	nCK	-
CKE minimum pulse width	t_{CKE}	Max (3nCK, 5ns)	-	Max (3nCK, 5ns)	-	Max (3nCK, 5ns)	-	nCK	31,32
Command pass disable delay	t_{CPDED}	4	-	4	-	4	-	nCK	-

Speed		DDR4-2666		DDR4-2933		DDR4-3200		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
Power Down Entry to Exit Timing	t_{PD}	$t_{CKE\ (min)}$	9 * t_{REFI}	$t_{CKE\ (min)}$	9 * t_{REFI}	$t_{CKE\ (min)}$	9 * t_{REFI}	nCK	6
Timing of ACT command to Power Down entry	$t_{ACTPDEN}$	2	-	2	-	2	-	nCK	7
Timing of PRE or PREA command to Power Down entry	t_{PRPDEN}	2	-	2	-	2	-	nCK	7
Timing of RD/RDA command to Power Down entry	t_{RDPDEN}	RL + 4 + 1	-	RL + 4 + 1	-	RL + 4 + 1	-	nCK	-
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	t_{WRPDEN}	WL + 4 + (t_{WR}/$t_{CK\ (avg)}$)	-	WL + 4 + (t_{WR}/$t_{CK\ (avg)}$)	-	WL + 4 + (t_{WR}/$t_{CK\ (avg)}$)	-	nCK	4
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	$t_{WRAPDEN}$	WL + 4 + WR + 1	-	WL + 4 + WR + 1	-	WL + 4 + WR + 1	-	nCK	5
Timing of WR command to Power Down entry (BC4MRS)	$t_{WRP-BC4DEN}$	WL + 2 + (t_{WR}/$t_{CK\ (avg)}$)	-	WL + 2 + (t_{WR}/$t_{CK\ (avg)}$)	-	WL + 2 + (t_{WR}/$t_{CK\ (avg)}$)	-	nCK	4
Timing of WRA command to Power Down entry (BC4MRS)	$t_{WRAP-BC4DEN}$	WL + 2 + WR + 1	-	WL + 2 + WR + 1	-	WL + 2 + WR + 1	-	nCK	5
Timing of REF command to Power Down entry	$t_{REFPDEN}$	2	-	2	-	2	-	nCK	7
Timing of MRS command to Power Down entry	$t_{MRSPDEN}$	$t_{MOD\ (min)}$	-	$t_{MOD\ (min)}$	-	$t_{MOD\ (min)}$	-	nCK	-
PDA Timing									
MODE REGISTER SET command cycle time in PDA mode	t_{MRD_PDA}	Max (16nCK, 10ns)	-	Max (16nCK, 10ns)	-	Max (16nCK, 10ns)	-	nCK	-
MODE REGISTER SET command update delay in PDA mode	t_{MOD_PDA}	t_{MOD}		t_{MOD}		t_{MOD}		nCK	-
ODT Timing									
Asynchronous R_{TT} turn-on delay (Power-Down with DLL frozen)	t_{AONAS}	1	9	1	9	1	9	ns	-

Speed		DDR4-2666		DDR4-2933		DDR4-3200		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
Asynchronous R_{TT} turn-off delay (Power-Down with DLL frozen)	t_{AOFAS}	1	9	1	9	1	9	ns	-
R_{TT} dynamic change skew	t_{ADC}	0.28	0.72	0.26	0.74	0.26	0.74	t_{CK} (avg)	-
Write Leveling Timing									
First DQS_t/DQS_c rising edge after write leveling mode is programmed	t_{WLMRD}	40	-	40	-	40	-	nCK	12
DQS_t/DQS_c delay after write leveling mode is programmed	$t_{WLDQSEN}$	25	-	25	-	25	-	nCK	12
Write leveling setup time from rising CK_t, CK_c crossing to rising DQS_t/DQS_c crossing	t_{WLS}	0.13	-	0.13	-	0.13	-	t_{CK}	-
Write leveling hold time from rising DQS_t/DQS_c crossing to rising CK_t, CK_crossing	t_{WLH}	0.13	-	0.13	-	0.13	-	t_{CK} (avg)	-
Write leveling output delay	t_{WLO}	0	9.5	0	9.5	0	9.5	ns	-
Write leveling output error	t_{WLOE}	-	2	-	2	-	2	ns	-
CA Parity Timing									
Commands not guaranteed to be executed during this time	$t_{PAR\_UNKNOWN}$	-	PL	-	PL	-	PL	nCK	-
Delay from errant command to ALERT_n assertion	$t_{PAR\_ALERT\_ON}$	-	PL + 6ns	-	PL + 6ns	-	PL + 6ns	nCK	-
Pulse width of ALERT_n signal when asserted	$t_{PAR\_ALERT\_PW}$	80	160	88	176	96	192	nCK	-
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	$t_{PAR\_ALERT\_RSP}$	-	71	-	78	-	85	nCK	-
Parity Latency	PL	5		6		6		nCK	-
CRC error to ALERT_n latency	t_{CRC_ALERT}	3	13	3	13	3	13	ns	-
CRC ALERT_n pulse width	$t_{CRC\_ALERT\_PW}$	6	10	6	10	6	10	nCK	-

Speed		DDR4-2666		DDR4-2933		DDR4-3200		Unit	Note
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
Gear Down Timing									
Exit RESET from CKE HIGH to a valid MRS geardown (T2/Reset)	t_{XPR_GEAR}	t_{XPR}	-	t_{XPR}	-	t_{XPR}	-	-	-
CKE High Assert to Gear Down Enable time (T2/CKE)	t_{XS_GEAR}	t_{XS}	-	t_{XS}	-	t_{XS}	-	-	-
MRS command to Sync pulse time(T3)	t_{SYNC_GEAR}	t_{MOD} + 4nCK	-	t_{MOD} + 4nCK	-	t_{MOD} + 4nCK	-	-	27
Sync pulse to First valid command(T4)	t_{CMD_GEAR}	t_{MOD}	-	t_{MOD}	-	t_{MOD}	-	-	27
Geardown setup time	$t_{GEAR\ setup}$	2	-	2	-	2	-	nCK	-
Geardown hold time	$t_{GEAR\ hold}$	-	-	2	-	2	-	nCK	-
t_{REFI}									
$t_{RFC1\ (min)}$	8Gb	350	-	350	-	350	-	ns	34
$t_{RFC2\ (min)}$	8Gb	260	-	260	-	260	-	ns	34
$t_{RFC4\ (min)}$	8Gb	160	-	160	-	160	-	ns	34

Note:

1. Start of internal WRITE transaction is defined as follows:
   - For BL8 (Fixed by MRS and on-the-fly): Rising clock edge 4 clock cycles after WL.
   - For BC4 (on-the-fly): Rising clock edge 4 clock cycles after WL.
   - For BC4 (Fixed by MRS): Rising clock edge 2 clock cycles after WL.
2. A separate timing parameter will cover the delay from write to read when CRC and DM are simultaneously enabled.
3. Commands requiring a locked DLL are READ (and Read Auto Precharge) and synchronous ODT commands.
4. t_{WR} is defined in ns, for calculation of t_{WRPDEN} it is necessary to round up t_{WR}/t_{CK} following rouding algorithm defined in Section 11.5.
5. WR in clock cycles as programmed in MR0.
6. t_{REFI} depends on T_{OPER}.
7. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down I_{DD} spec will not be applied until

finishing those operations.

8. For these parameters, the DDR4 SDRAM device supports $t_{nPARAM\ [nCK]}$ = ROUND UP{$t_{PARAM[ns]}/t_{CK(avg)[ns]}$}, which is in clock cycles assuming all input clock jitter specifications are satisfied.
9. When CRC and DM are both enabled, $t_{WR\_CRC\_DM}$ is used in place of t_{WR}.
10. When CRC and DM are both enabled, $t_{WTR\_S\_CRC\_DM}$ is used in place of t_{WTR_S}.
11. When CRC and DM are both enabled, $t_{WTR\_L\_CRC\_DM}$ is used in place of t_{WTR_L}.
12. The max value is system dependent.
13. DQ to DQS total timing per group where the total includes the sum of deterministic and random timing terms for a specified BER. BER spec and measurement method are TBD.
14. The deterministic component of the total timing.
15. DQ to DQ static offset relative to strobe per group.
16. This parameter will be characterized and guaranteed by design.
17. When the device is operated with the input clock jitter, this parameter needs to be derated by the actual $t_{jit(per)\_total}$ of the input clock. (output deratings are relative to the SDRAM input clock).
18. DRAM DBI mode is off.
19. DRAM DBI mode is enabled. Applicable to x8 and x16 DRAM only.
20. t_{QSL} describes the instantaneous differential output low pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge.
21. t_{QSH} describes the instantaneous differential output high pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge.
22. There is no maximum cycle time limit besides the need to satisfy the refresh interval t_{REFI}.
23. $t_{CH(abs)}$ is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.
24. $t_{CL(abs)}$ is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.
25. Total jitter includes the sum of deterministic and random jitter terms for a specified BER. BER target and measurement method are TBD.
26. The deterministic jitter component out of the total jitter. This parameter is characterized and guaranteed by design.
27. This parameter has to be even number of clocks.
28. When CRC and DM are both enabled, $t_{WR\_CRC\_DM}$ is used in place of t_{WR}.
29. When CRC and DM are both enabled, $t_{WTR\_S\_CRC\_DM}$ is used in place of t_{WTR_S}.
30. When CRC and DM are both enabled, $t_{WTR\_L\_CRC\_DM}$ is used in place of t_{WTR_L}.
31. After CKE is registered LOW, CKE signal level shall be maintained below $V_{IL(DC)}$ for t_{CKE} specification (low pulse width).
32. After CKE is registered HIGH, CKE signal level shall be maintained above $V_{IH(DC)}$ for t_{CKE} specification (high pulse width).
33. Defined between end of MPR Read burst and MRS which reloads MPR or disables MPR function.

34. Parameters apply from $t_{CK\ (avg)min}$ to $t_{CK\ (avg)max}$ at all standard JEDEC clock period values as stated in the Section 9 SPEED BIN .
35. This parameter must keep consistency with Section 9 SPEED BIN.
36. DDR4-1600 AC timing apply if DRAM operates at lower than 1600MT/s data rate. UI = $t_{CK\ (avg)min}/2$.
37. Applied when DRAM is in DLL ON mode.
38. Assume no jitter on input clock signals to the DRAM.
39. Value is only valid for $R_{ONnom} = 34\Omega$.
40. $1t_{CK}$ toggle mode with setting MR4: A11 to 0.
41. $2t_{CK}$ toggle mode with setting MR4: A11 to 1, which is valid for DDR4-2400/2666/3200 speed grade.
42. $1t_{CK}$ mode with setting MR4: A12 to 0.
43. $2t_{CK}$ mode with setting MR4: A12 to 1, which is valid for DDR4-2400/2666/3200 speed grade.
44. The maximum read preamble is bounded by $t_{LZ(DQS)min}$ on the left side and $t_{DQSCK(max)}$ on the right side.
45. DQ falling signal middle-point of transferring from HIGH to LOW to first rising edge of DQS diff-signalcross-point.
46. Last falling edge of DQS diff-signal cross-point to DQ rising signal middle-point of transferring from LOW to HIGH.
47. V_{REFDQ} value must be set to either its midpoint or $V_{cent\_DQ(midpoint)}$ in order to capture DQ0 or DQL0 low level for entering PDA mode.
48. The maximum read postamble is bound by $t_{DQSCK\ (min)}$ plus $t_{QSH\ (min)}$ on the left side and $t_{HZ(DQS)max}$ on the right side.
49. Reference level of DQ output signal is specified with a midpoint as a widest part of Output signal eye which should be approximately 0.7 * V_{DDQ} as a center level of the static single-ended output peak-to-peak swing with a driver impedance of 34 Ω and an effective test load of 50Ω to $V_{TT} = V_{DDQ}$.
50. For MR7 commands, the minimum delay to a subsequent non-MRS command is 5nCK.

10.6 Rounding Algorithms

Software algorithms for calculation of timing parameters are subject to rounding errors from many sources. For example, a system may use a memory clock with a nominal frequency of 933.33MHz which yields a clock period of 1.0714ns. Similarly, a system with a memory clock frequency of 1066.66MHz yields mathematically a clock period of 0.9375ns. In most cases, it is impossible to express all digits after the decimal point exactly, and rounding must be done because the DDR4 SDRAM specification establishes a minimum granularity for timing parameters of 1ps.

Rules for rounding must be defined to allow optimization of device performance without violating device parameters. These algorithms rely on results that are within correction factors on device testing and specification to avoid losing performance due to rounding errors.

These rules are:

- Clock periods such as $t_{CK\ (avg)min}$ are defined to 1ps of accuracy; for example, 0.9375ns is defined as 937ps and 1.0714ns is defined as 1071ps.
- Using real math, parameters like $t_{AA\ (min)}$, $t_{RCD\ (min)}$, etc. which are programmed in systems in numbers of clocks (nCK) but expressed in units of time (in ns) are divided by the clock period (in ns) yielding a unitless ratio, a correction factor of 2.5% is subtracted, then the result is set to the next higher integer number of clocks:
  nCK = ceiling [(parameter_in_ns/application_t_{CK}_ in_ns) - 0.025]
- Alternatively, programmers may prefer to use integer math instead of real math by expressing timing in ps, scaling the desired parameter value by 1000, dividing by the application clock period, adding an inverse correction factor of 97.4%, dividing the result by 1000, then truncating down to the next lower integer value:
  nCK = truncate [{(parameter_in_ps * 1000)/(application_t_{CK}_in_ps) + 974}/1000]
- Either algorithm yields identical results. In case of conflict between results, the preferred algorithm is the integer math algorithm.
- This algorithm applies to all timing parameters documented in a Serial Presence Detect (SPD) when converting from ns to nCK. Other timing parameters may use a simpler algorithm:
  nCK = ceiling (parameter_in_ns/application_t_{CK}_in_ns).

10.7 The DQ Input Receiver Compliance Mask for Voltage and Timing

The DQ input receiver compliance mask for voltage and timing is shown in Figure 26 below. The receiver mask (Rx Mask) defines area the input signal must not encroach in order for the DRAM input receiver to be able to successfully capture a valid input signal. Any input signal encroaching within the Rx Mask is subject to being invalid data. The Rx Mask is the receiver property for each DQ input pin and it is not the valid data-eye.

Figure 28 - DQ Receiver (Rx) Compliance mask

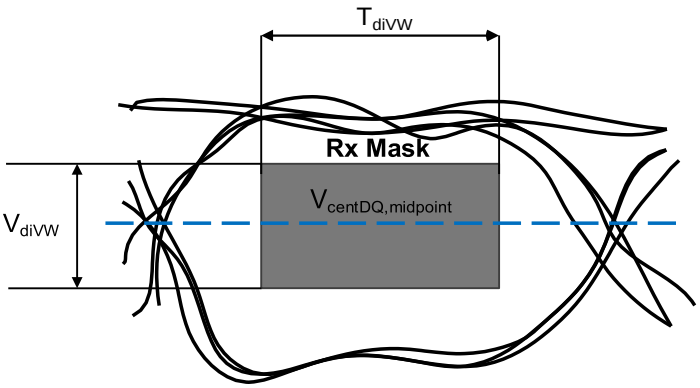
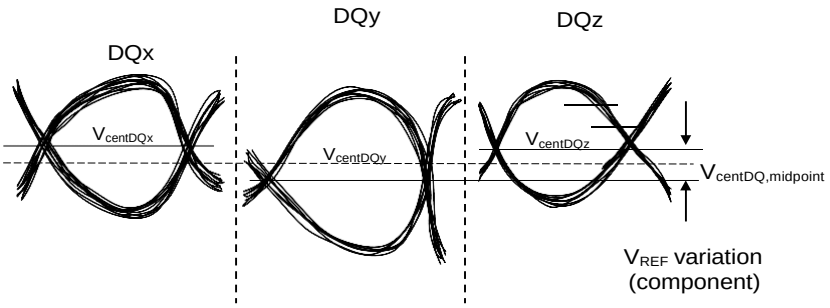


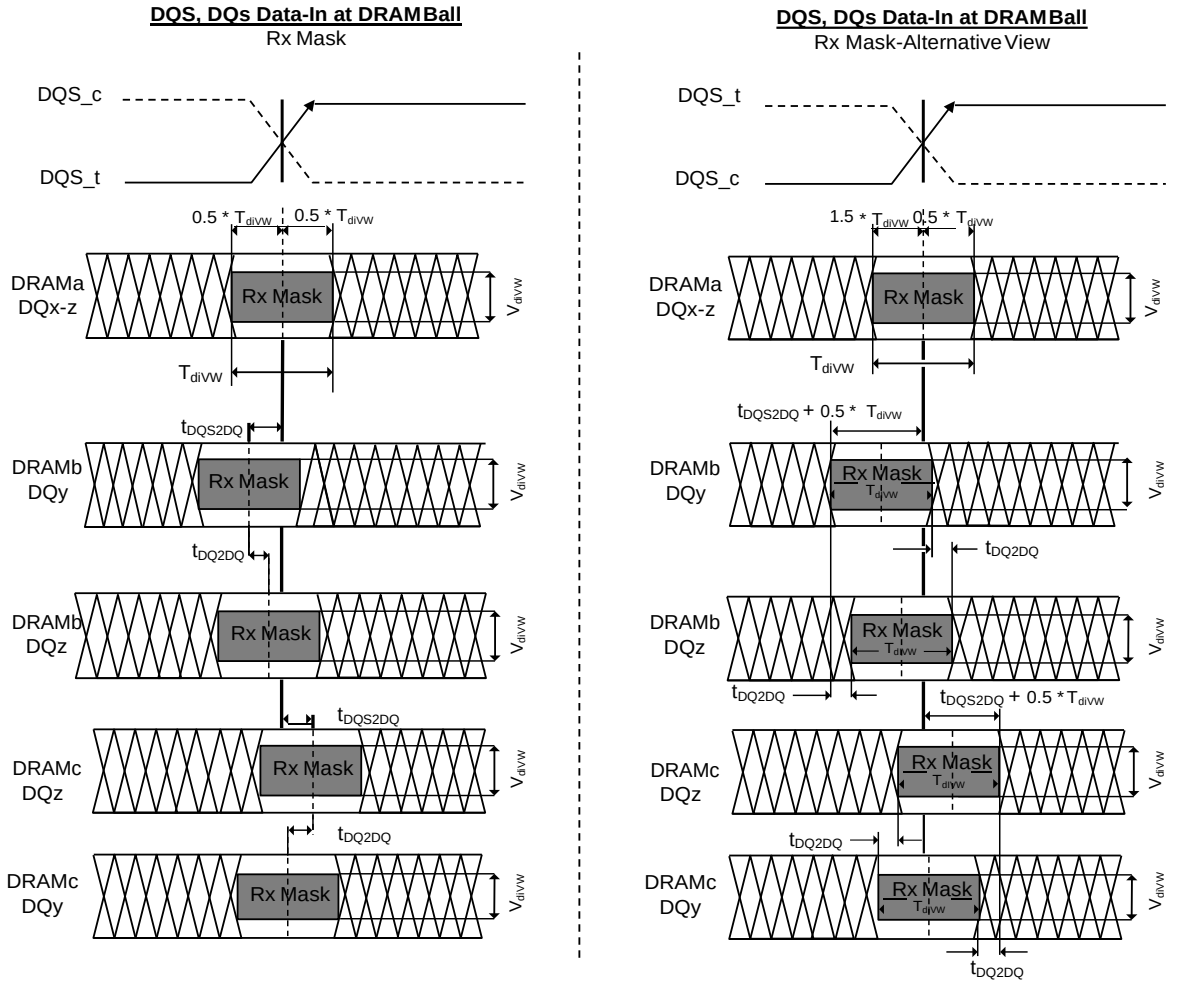
Figure 29 - Across Pin VREFDQ Voltage Variation



The V_{REFDQ} voltage is an internal reference voltage level that shall be set to the properly trained setting, which is generally $V_{centDQ,midpoint}$, in order to have valid Rx Mask values.

$V_{centDQ\ (pin\ avg)}$ is defined as the midpoint between the largest V_{REFDQ} voltage level and the smallest V_{REFDQ} voltage level across all DQ pins for a given DRAM component. Each DQ pin V_{REF} level is defined by the center, i.e. widest opening, of the cumulative data input eye as depicted in Figure 27. This clarifies that any DRAM component level variation must be accounted for within the DRAM Rx mask. The component level V_{REF} will be set by the system to account for R_{ON} and ODT settings.

Figure 30 - DQS to DQ and DQ to DQ Timings at DRAM Balls



Note:

- DQx represents an optimally centered mask.
- DQy represents earliest valid mask.
- DQz represents lasted valid mask.

Note:

- DRAMa represents a DRAM without any DQS/DQ skews.
- DRAMb represents a DRAM with early skews (negative t_{DQS2DQ}).
- DRAMc represents a DRAM with delayed skews (positive t_{DQS2DQ}

Note:

1. Figures show skew allowed between DRAM to DRAM and between DQ to DQ for a DRAM. Signals assume data centered aligned at DRAM Latch.
2. T_{diPW} is not shown; composite data-eyes shown would violate T_{diPW}.
3. $V_{centDQ,midpoint}$ is not shown but is assumed to be midpoint of V_{diVW}.

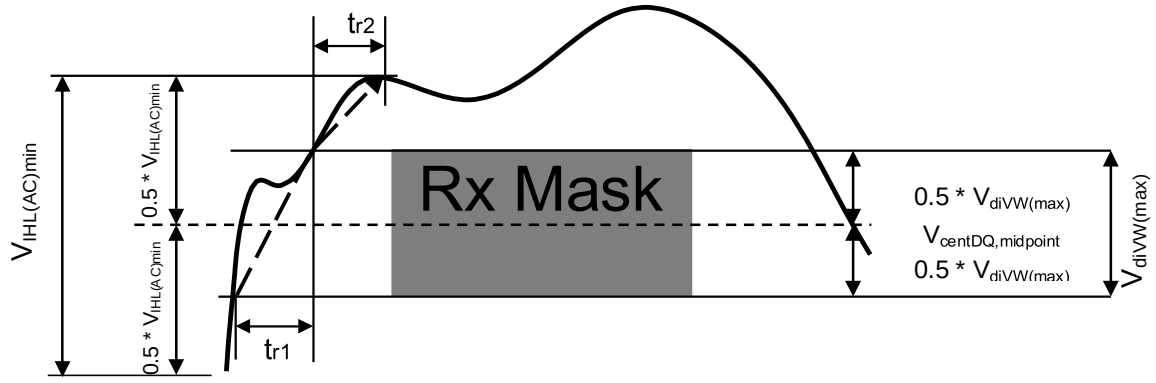
All of the timing term in Figure 28 are measured at the V_{diVW} voltage levels centered around $V_{centDQ,midpoint}$ and are referencedto the DQS_t/DQS_c center aligned to the DQ per pin.

The rising edge slew rates are defined by srr1 and srr2. The slew rate measurement points for a rising edge are shown in Figure 29 below: A LOW to HIGH transition tr1 is measured from 0.5 * $V_{diVW,max}$ below $V_{centDQ,midpoint}$ to the last transition through 0.5 * $V_{diVW,max}$ above $V_{centDQ,midpoint}$ to the first transition through the 0.5 * $V_{IHL(AC)min}$ above $V_{centDQ,midpoint}$.

Rising edge slew rate equations:

- srr1 = $V_{diVW,max}/t_{r1}$
- srr2 = $(V_{IHL(AC)min} - V_{diVW,max})/(2 * t_{r2})$

Figure 31 - Slew Rate Conditions for Rising Transition



The falling edge slew rates are defined by srf1 and srf2. The slew rate measurement points for a falling edge are shown in Figure 30 below: A HIGH to LOW transition t_{f1} is measured from 0.5 * $V_{diVW,max}$ above $V_{centDQ,midpoint}$ to the last transition through 0.5 * $V_{diVW,max}$ below $V_{centDQ,midpoint}$ while t_{f2} is measured from the last transition through 0.5 * $V_{diVW,max}$ below $V_{centDQ,midpoint}$ to the first transition through the 0.5 * $V_{IHL(AC)min}$ below $V_{centDQ\ (pin\ mid)}$.

Falling edge slew rate equations:

- srf1 = $V_{diVW,max}/t_{f1}$
- srf2 = $(V_{IHL(AC)min} - V_{diVW,max})/(2 * t_{f2})$

Figure 32 - Slew Rate Conditions for Falling Transition

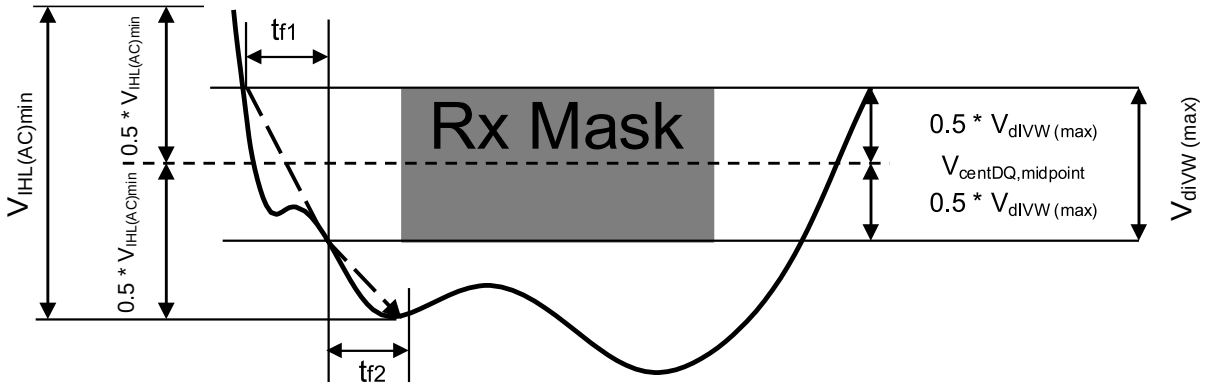


Table 58 - DRAM DQs in Receive Mode; UI = $t_{CK(avg)min}$/2

Symbol	Parameter	1600/1866/2133		2400		2666		3200		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
V_{dIVW}	Rx Mask voltage - pk-pk	-	136	-	130	-	120	-	110	mV	1,2,10
T_{dIVW}	Rx timing window	-	0.2	-	0.2	-	0.22	-	0.23	UI	1,2,10
$V_{IHL(AC)}$	DQ AC input swing pk-pk	186	-	160	-	150	-	140	-	mV	3,4,10
T_{diPW}	DQ input pulse width	0.58	-	0.58	-	0.58	-	0.58	-	UI	5,10
t_{DQS2DQ}	Rx Mask DQS to DQ offset	-0.17	0.17	-0.17	0.17	-0.19	0.19	-0.22	0.22	UI	6,10
t_{DQ2DQ}	Rx Mask DQ to DQ offset	-	0.1	-	0.1	-	0.105	-	0.125	UI	7
srr1 srf1	Input Slew Rate over V_{dIVW} if $t_{CK} \geq$ 0.937ns	1.0	9	1.0	9	1.0	9	1.0	9	V/ns	8,10
srf1 srf2	Input Slew Rate over V_{dIVW} if 0.937ns > $t_{CK} \geq$ 0.625ns	-	-	1.25	9	1.25	9	1.25	9	V/ns	8,10
srr2	Rising Input Slew Rate over 1/2 $V_{IHL(AC)}$	0.2 * srr1	9	0.2 * srr1	9	0.2 * srr1	9	0.2 * srr1	9	V/ns	9,10
srf2	Falling Input Slew Rate over 1/2 $V_{IHL(AC)}$	0.2 * srf1	9	0.2 * srf1	9	0.2 * srf1	9	0.2 * srf1	9	V/ns	9,10

Note:

1. Data Rx mask voltage and timing total input valid window where V_{dIVW} is centered around $V_{centDQ,midpoint}$ after V_{REFDQ} training is completed. The data Rx mask is applied per bit and should include voltage and temperature drift terms. The input buffer design specification is to achieve at least a BER = 1^{e-16} when the Rx mask is not violated.
2. Defined over the DQ internal V_{REF} range 1.
3. Overshoot and undershoot specifications apply.
4. DQ input pulse signal swing into the receiver must meet or exceed $V_{IHL(AC)min}$. $V_{IHL(AC)min}$ is to be achieved on an UI basis when a rising and falling edge occur in the same UI, i.e., a valid T_{diPW}.
5. DQ minimum input pulse width defined at the $V_{centDQ,midpoint,}$.
6. DQS to DQ offset is skew between DQS and DQs within a nibble (x4) or word (x8, x16) at the DDR4 SDRAM balls over process, voltage, and temperature.
7. DQ to DQ offset is skew between DQs within a nibble (x4) or word (x8, x16) at the DDR4 SDRAM balls for a given component over process, voltage, and temperature.
8. Input slew rate over V_{dIVW} mask centered at $V_{centDQ,midpoint}$. Slowest DQ slew rate to fastest DQ slew rate per transition edge must be within 1.7V/ns of each other.
9. Input slew rate between V_{dIVW} mask edge and $V_{IHL(AC)min}$ points.
10. All Rx mask specifications must be satisfied for each UI. For example, if the minimum input pulse width is violated when satisfying $T_{dIVW(min)}$, $V_{dIVW,max}$, and minimum slew rate limits, then either $T_{dIVW(min)}$ or minimum slew rates would have to be increased to the point where the minimum input pulse width would no longer be violated.

10.8 Command, Control, and Address Setup, Hold, and Derating

The total t_{IS} (setup time) and t_{IH} (hold time) required is calculated to account for slew rate variation by adding the data sheet t_{IS} (base) values, the $V_{IL(AC)}/V_{IH(AC)}$ points, and t_{IH} (base) values, the $V_{IL(DC)}/V_{IH(DC)}$ points; to the Δt_{IS} and Δt_{IH} derating values, respectively. The base values are derived with single-end signals at 1V/ns and differential clock at 2V/ns. Example: t_{IS} (total setup time) = t_{IS} (base) + Δt_{IS}. For a valid transition, the input signal has to remain above/ below $V_{IH(AC)}/V_{IL(AC)}$ for the time defined by t_{VAC}.

Although the total setup time for slow slew rates might be negative (for example, a valid input signal will not have reached $V_{IH(AC)}/V_{IL(AC)}$ at the time of the rising clock transition), a valid input signal is still required to complete the transition and to reach $V_{IH(AC)}/V_{IL(AC)}$. For slew rates that fall between the values listed in derating tables, the derating values may be obtained by linear interpolation.

Setup (t_{IS}) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(DC)max}$ and the first crossing of $V_{IH(AC)min}$ that does not ring back below $V_{IH(DC)min}$. Setup (t_{IS}) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(DC)min}$ and the first crossing of $V_{IL(AC)max}$ that does not ring back above $V_{IL(DC)max}$.

Hold (t_{IH}) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(DC)max}$ and the first crossing of $V_{IH(AC)min}$ that does not ring back below $V_{IH(DC)min}$.

Hold (t_{IH}) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(DC)min}$ and the first crossing of $V_{IL(AC)min}$ that does not ring back above $V_{IL(DC)max}$.

Table 59 - Command, Address, Control Setup and Hold Values

DDR4	1600	1866	2133	2400	2666	3200	Unit	Reference
t_{IS} (base, AC100)	115	100	80	62	-	-	ps	$V_{IHL(AC)}$
t_{IH} (base, DC75)	140	125	105	87	-	-	ps	$V_{IHL(DC)}$
t_{IS} (base, AC90)	-	-	-	-	55	40	ps	$V_{IHL(AC)}$
t_{IH} (base, DC65)	-	-	-	-	80	65	ps	$V_{IHL(DC)}$
t_{IS}/t_{IH} (V_{REF})	215	200	180	162	145	130	ps	$V_{IHL(DC)}$

Note:

1. Base AC/DC referenced for 1V/ns slew rate and 2V/ns clock slew rate.
2. Values listed are referenced only; applicable limits are defined elsewhere.

Table 60 - Command, Address, Control Input Voltage Values

DDR4	1600	1866	2133	2400	2666	3200	Unit	Reference
$V_{IH(AC)min}$	100	100	100	100	90	90	mV	$V_{IHL(AC)}$
$V_{IH(DC)min}$	75	75	75	75	65	65	mV	$V_{IHL(DC)}$
$V_{IL(DC)max}$	-75	-75	-75	-75	-65	-65	mV	$V_{IHL(AC)}$
$V_{IL(AC)max}$	-100	-100	-100	-100	-90	-90	mV	$V_{IHL(DC)}$

Note:

1. Command, Address, Control input levels relative to VREFCA.
2. Values listed are referenced only; applicable limits are defined elsewhere.

Table 61 - Derating Values DDR4-1600/1866/2133/2400 t_{IS}/t_{IH} - AC/DC Based

Δt_{IS}, Δt_{IH} derating in [ps] AC/DC Based[1]																	
		CK_t, CK_c Differential Slew Rate															
		10.0V/ns		8.0V/ns		6.0V/ns		4.0V/ns		3.0V/ns		2.0V/ns		1.5V/ns		1.0V/ns	
		Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}
ADDR, CNTL Input Slew Rate V/ns	7.0	76	54	76	55	77	56	79	58	82	60	86	64	94	73	111	89
	6.0	73	53	74	53	75	54	77	56	79	58	83	63	92	71	108	88
	5.0	70	50	71	51	72	52	74	54	76	56	80	60	88	68	105	85
	4.0	65	46	66	47	67	48	69	50	71	52	75	56	83	65	100	81
	3.0	57	40	57	41	58	42	60	44	63	46	67	50	75	58	92	75
	2.0	40	28	41	28	42	29	44	31	46	33	50	38	58	46	75	63
	1.5	23	15	24	16	25	17	27	19	29	21	33	25	42	33	58	50
	1.0	-10	-10	-9	-9	-8	-8	-6	-6	-4	-4	0	0	8	8	25	25
	0.9	-17	-14	-16	-14	-15	-13	-13	-10	-11	-8	-7	-4	1	4	18	21
	0.8	-26	-19	-25	-19	-24	-18	-22	-16	-20	-14	-16	-9	-7	-1	9	16
	0.7	-37	-26	-36	-25	-35	-24	-33	-22	-31	-20	-27	-16	-18	-8	-2	9
	0.6	-52	-35	-51	-34	-50	-33	-48	-31	-46	-29	-42	-25	-33	-17	-17	0
	0.5	-73	-48	-72	-47	-71	-46	-69	-44	-67	-42	-63	-38	-54	-29	-38	-13
	0.4	-104	-66	-103	-66	-102	-65	-100	-63	-98	-60	-94	-56	-85-	-48	-69	-31

Note:

1. $V_{IHL(AC)}$ = ± 100mV, $V_{IHL(DC)}$ = ± 75mV; relative to V_{REFCA}.

Table 62 - Derating Values DDR4-2666/2933/3200 t_{IS}/t_{IH} - AC/DC Based

Δt_{IS}, Δt_{IH} derating in [ps] AC/DC Based[1]																	
		CK_t, CK_c Differential Slew Rate															
		10.0V/ns		8.0V/ns		6.0V/ns		4.0V/ns		3.0V/ns		2.0V/ns		1.5V/ns		1.0V/ns	
		Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}
ADDR, CNTL Input Slew Rate V/ns	7.0	68	47	69	47	70	48	72	50	73	52	77	56	85	63	100	78
	6.0	66	45	67	46	68	47	69	49	71	50	75	54	83	62	98	77
	5.0	63	43	64	44	65	45	66	46	68	48	72	52	80	60	95	75
	4.0	59	40	59	40	60	41	62	43	64	45	68	49	75	56	90	71
	3.0	51	34	52	35	53	36	54	38	56	40	60	43	68	51	83	66
	2.0	36	24	37	24	38	25	39	27	41	29	45	33	53	40	68	55
	1.5	21	13	22	13	23	14	24	16	26	18	30	22	38	29	53	44
	1.0	-9	-9	-8	-8	-8	-8	-6	-6	-4	-4	0	0	8	8	23	23
	0.9	-15	-13	-15	-12	-14	-11	-12	-9	-10	-7	-6	-4	1	4	16	19
	0.8	-23	-17	-23	-17	-22	-16	-20	-14	-18	-12	-14	-8	-7	-1	8	14
	0.7	-34	-23	-33	-22	-32	-21	-30	-20	-28	-18	-25	-14	-17	-6	-2	9
	0.6	-47	-31	-47	-30	-46	-29	-44	-27	-42	-25	-38	-22	-31	-14	-16	1
	0.5	-67	-42	-66	-41	-65	-40	-63	-38	-61	-36	-58	-33	-50	-25	-35	-10
	0.4	-95	-58	-95	-57	-94	-56	-92	-54	-90	-53	-86	-49	-79	-41	-64	-26

Note:

1. $V_{IHL(AC)}$ = ± 90mV, $V_{IHL(DC)}$ = ± 65mV; relative to V_{REFCA}

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