Feb. 2023

SCP30N2G1GSL

2Gbit NAND + 1Gbit LPDDR2 MCP

Data Sheet

Rev. D

Revision History		
Date	**Version**	**Subjects(major changes since last revision)**
2021-12	A	Initial Release
2022-08	B	Add Industrial grade Add DRAM IDD spec
2022-09	C	Update NAND parameter page value
2023-02	D	Update DRAM IDD spec Update NAND device ID info.

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PRODUCT FEATURES

Multi-Chip Package
– NAND Flash Density: 2-Gbits
– Mobile LPDDR2 SDRAM Density: 1-Gbits

Device Packaging
– 162 balls FBGA
– Area: 10.5 mm x 8 mm; Height: 1 mm

Operating Voltage
– NAND: 1.7V to 1.95V
– Mobile LPDDR2 SDRAM:
VDD1 = 1.7V to 1.95V
VDD2, VDDCA, VDDQ = 1.14 to 1.3V

Operating Temperature (TC):-25 °C to +85 °C (Extended)
Operating Temperature (TC):-40 °C to +85 °C (Industrial)

NAND FLASH

■ **X8 I/O BUS**
- NAND Interface
- ADDRESS / DATA/COMMANDS Multiplexing

■ **SUPPLY VOLTAGE**
- 1.8 V device: VCC = 1.7 V -1.95 V

■ **PAGE READ / PROGRAM**
- (2048+128 spare) byte
- Synchronous Page Read Operation
- Random access: 30us (Max)
- Serial access: 45ns (1.7V)
- Page program time: 300us (Typ)

■ **PAGE COPY BACK**
- Support copy back program

■ **READ CACHE**
- Support read cache

■ **LEGACY/ONFI 1.0 COMMAND SET**
- Open NAND Flash Interface (ONFI) 1.0 compliant

■ **FAST BLOCK ERASE**
- Block size: 64 Pages
  X8 (128K + 8K) bytes
- Block erase time: 3.5ms (Typ)

■ **MEMORY CELL ARRAY**
- X8 : 1024 blocks Per Plane or (128MB + 8MB)

■ **Security**
- One Time Programmable (OTP) area
- Hardware program/erase disable during power transition

■ **ELECTRONIC SIGNATURE**

- Manufacturer Code

■ **STATUS REGISTER**
■ **HARDWARE DATA PROTECTION**
■ **DATA RETENTION**

- 100K Cycling Program / Erase cycles
- Data retention: 10 Years (4bit/528byte ECC(x8)
- Blocks zero and one are valid and will be valid for at least 1,000 program-erase cycles with ECC

Mobile DDR2 SDRAM (S4B)

- JEDEC LPDDR2-S4B compliance
- 8 banks x 4M x 32 organization
- Data Mask for Write Control (DM)
- 8 Banks controlled by BA0 & BA1 & BA2
- Programmable CAS Latency:
  Read latency: 8~3
  Write latency: 4~1
- Programmable Wrap and No Wrap Sequence: Sequential or Interleave
- Programmable Burst Length:
  4, 8 or 16 for Wrap Sequential
  4, 8 for Wrap Interleave
  4 for No Wrap
- Automatic and Controlled Precharge Command
- Power Down and Deep Power Down Mode
- Auto Refresh and Self Refresh
- Refresh Interval: 4096 cycles/32ms
- Double Data Rate (DDR)
- Bidirectional Data Strobe (DQS) for input and output data, active on both edges
- Differential clock inputs CLK and /CLK
- Power Supply:
  VDD1: 1.7V - 1.95V
  VDD2: 1.14V - 1.3V
  VDDQ: 1.14V - 1.3V
- Auto Temperature-Compensated Self Refresh (Auto TCSR)
- Partial-Array Self Refresh (PASR) Option: Full, 1/2, 1/4
- Drive Strength (DS) Option:
  34.3ohm,40ohm,48ohm,60ohm,80ohm,120ohm
  Default 40ohm
- Speed/Cycle Time
  2.5ns @ RL6 (LPDDR2-800)
  1.875ns @ RL8 (LPDDR2-1066)

Ordering Information

Product ID	NAND Flash		Mobile DDR2 SDRAM		Package	Operation Tempera-ture Range
	Configuration	Speed	Configuration	Clock Speed		
SCP30N2G1GSL-18AE	2Gb (256M X8 bits)	45ns	1G (32M X 32 bits)	533MHz	162 ball BGA (10.5mm x 8mm)	Extended
SCP30N2G1GSL-25AE	2Gb (256M X8 bits)	45ns	1Gb (32M X 32 bits)	400MHz	162 ball FBGA (10.5mm x 8mm)	Extended
SCP30N2G1GSL-18AI	2Gb (256M X8 bits)	45ns	1Gb (32M X 32 bits)	533MHz	162 ball FBGA (10.5mm x 8mm)	Industrial
SCP30N2G1GSL-25AI	2Gb (256M X8 bits)	45ns	1Gb (32M X 32 bits)	400MHz	162 ball FBGA (10.5mm x 8mm)	Industrial

Ball Configuration (Top View)

(BGA 162 Ball, 10.5mmx8mmx1.0mm Body, 0.5mm Ball Pitch)

	1	2	3	4	5	6	7	8	9	10
A	DNU	DNU	WPN	CLE	VCC	IO4	IO7	VCC	DNU	DNU
B	DNU	VCC	NC	ALE	REN	IO5	NC	NC	VSS_N	DNU
C	NC	IO1	IO3	WEN	RYBY	IO6				
D	NC	IO0	IO2	CEN	NC	NC				
E	VSS_N	NC	NC		VDD2	VDD1	DQ31	DQ29	DQ26	DNU
F	VDD1	VSS_D	NC		VSS_D	VSSQ	VDDQ	DQ25	VSSQ	VDDQ
G	VSS_D	VDD2	ZQ		VDDQ	DQ30	DQ27	DQS3_T	DQS3_C	VSSQ
H	VSS_D	CA9	CA8		DQ28	DQ24	DM3	DQ15	VDDQ	VSSQ
J	NC	CA6	CA7		VSSQ	DQ11	DQ13	DQ14	DQ12	VDDQ
K	VDD2	CA5	VREFCA		DQS1_C	DQS1_T	DQ10	DQ9	DQ8	VSSQ
L	NC	VSS_D	CK_C		DM1	VDDQ				
M	VSS_D	NC	CK_T		VSSQ	VDDQ	VDD2	VSS_D	VREFDQ	
N	CKE	NC	NC		DM0	VDDQ				
P	CS_N	NC	NC		DQS0_C	DQS0_T	DQ5	DQ6	DQ7	VSSQ
R	CA4	CA3	CA2		VSSQ	DQ4	DQ2	DQ1	DQ3	VDDQ
T	VSS_D	NC	CA1		DQ19	DQ23	DM2	DQ0	VDDQ	VSSQ
U	VSS_D	VDD2	CA0		VDDQ	DQ17	DQ20	DQS2_T	DQS2_C	VSSQ
V	VDD1	VSS_D	NC		VSS_D	VSSQ	VDDQ	DQ22	VSSQ	VDDQ
W	DNU	NC	NC		VDD2	VDD1	DQ16	DQ18	DQ21	DNU
Y	DNU	DNU							DNU	DNU

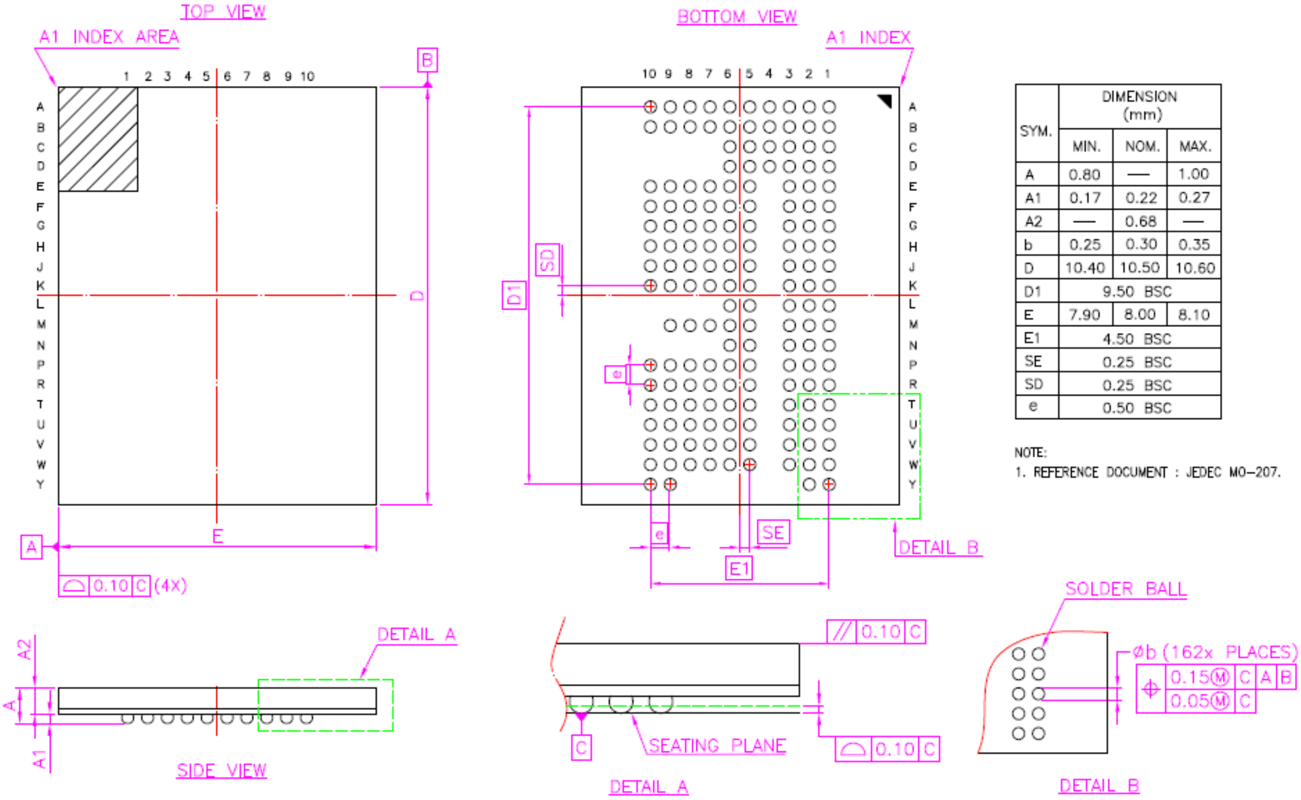
Ball Descriptions

Pin Name	Type	Function
NAND Flash		
VCC	Supply	**Supply Voltage.** The VCC supplies the power for all the operations (Read, Program, Erase). An internal lock circuit prevents the insertion of Commands when VCC is less than VLKO.
VSS_N	Supply	NAND Flash Ground relative to VCC
I/O0-I/O7	Input/output	The I/O pins are used for command input, address input, data input, and data output. The I/O pins float to High-Z when the device is deselected or the outputs are disabled.
ALE	Input	This input activates the latching of the I/O inputs inside the Address Register on the rising edge of Write Enable (WE#).
CLE	Input	This input activates the latching of the I/O inputs inside the Command Register on the rising edge of Write Enable (WE#).
CE#	Input	**Chip Enable.** This input controls the selection of the device. When the device is not busy CE# low selects the memory.
RE	Input	**Read Enable.** The RE# input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of RE# which also increments the internal column address counter by one.
WE#	Input	**Write Enable.** This input latches Command, Address and Data. The I/O inputs are latched on the rising edge of WE#.
WP#	Input	**Write Protect.** The WP# pin, when low, provides hardware protection against undesired data modification (program / erase).
R /B#	Output	**Ready Busy.** The Ready/Busy output is an Open Drain pin that signals the state of the memory.
Mobile DDR2 SDRAM		
CK_t, CK_c	Input	Clock: CK_t and CK_c are differential clock inputs. All Double Data Rate (DDR) CA
CKE	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates internal clock signals and therefore device input buffers and output drivers. Power savings modes are entered and exited through CKE transitions. CKE is considered part of the command code. CKE is sampled at the positive Clock edge.
CS_n	Input	Chip Select: CS_n is considered part of the command code. CS_n is sampled at the positive Clock edge.
CA[9:0]	Input	DDR Command/Address Inputs: Uni-directional command/address bus inputs. CA is considered part of the command code.
DQ[31:0]	I/O	Data Inputs/Output: Bi-directional data bus.

Pin Name	Type	Function
DQSn_t, DQSn_c	I/O	Data Strobe (Bi-directional, Differential): The data strobe is bi-directional (used for read and write data) and differential (DQS_t and DQS_c). It is output with read data and input with write data. DQS_t is edge-aligned to read data and centered with write data. DQS0_t and DQS0_c correspond to the data on DQ0-7; DQS1_t and DQS1_c correspond to the data on DQ8-15; DQS2_t and DQS0_c correspond to the data on DQ16-23; DQS3_t and DQS1_c correspond to the data on DQ24-31.
DMn	Input	Input Data Mask: DM is the input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS_t (or DQS_c). Although DM is for input only, the DM loading shall match the DQ and DQS_t (or DQS_c). DM0 is the input data mask signal for the data on DQ0-7; DM1 is the input data mask signal for the data on DQ8-15; DM2 is the input data mask signal for the data on DQ16-23; DM3 is the input data mask signal for the data on DQ24-31.
VDD1	Supply	Core Power Supply 1: Power supply for core.
VDD2	Supply	Core Power Supply 2: Power supply for core.
VDDCA	Supply	Input Receiver Power Supply: Power supply for CA[n:0], CKE, CS_n, CK_t, and CK_c input buffers.
VDDQ	Supply	I/O Power Supply: Power supply for Data input/output buffers.
VREF(CA)	Supply	Input Receiver Power Supply: Power supply for CA[n:0], CKE, CS_n, CK_t, and CK_c input buffers.
VREF(DQ)	Supply	Reference Voltage for DQ Input Receiver: Reference voltage for all Data input buffers.
VSS	Supply	Ground
VSSCA	Supply	Ground for CA Input Receivers

Packing Dimensions

162BGA 10.5x8mm



SYM.	DIMENSION (mm)		
	MIN.	NOM.	MAX.
A	0.80	—	1.00
A1	0.17	0.22	0.27
A2	—	0.68	—
b	0.25	0.30	0.35
D	10.40	10.50	10.60
D1	9.50 BSC		
E	7.90	8.00	8.10
E1	4.50 BSC		
SE	0.25 BSC		
SD	0.25 BSC		
e	0.50 BSC		

NOTE:
1. REFERENCE DOCUMENT : JEDEC MO-207.

NAND FLASH MEMORY OPERATIONS

1 SUMMARY DESCRIPTION

This device is offered in 1.8 VCC and VCCQ power supply, and with x8 I/O interface. Its NAND cell provides the most cost-effective solution for the solid state mass storage market. The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased. The page size for x8 is (2048 + spare) bytes.

Each block can be programmed and erased up to 100,000 cycles with ECC (error correction code) on. To extend the lifetime of NAND flash devices, the implementation of an ECC is mandatory.

The chip supports CE# don't care function. This function allows the direct download of the code from the NAND flash memory device by a microcontroller, since the CE# transitions do not stop the read operation.

The devices have a Read Cache feature that improves the read throughput for large files. During cache reading, the devices load the data in a cache register while the previous data is transferred to the I/O buffers to be read.

This device program operation typically writes in 300 µs and an erase operation can typically be performed in 3.5 ms on a 128-kB block (x8). In addition, thanks to multiplane architecture, it is possible to program two pages at a time (one per plane) or to erase two blocks at a time (again, one per plane). The multiplane architecture allows program time to be reduced by 40% and erase time to be reduced by 50%.

In multiplane operations, data in the page can be read out at 45 ns cycle time per byte. The I/O pins serve as the ports for command and address input as well as data input/output. This interface allows a reduced pin count and easy migration towards different densities, without any rearrangement of the footprint.

Commands, Data, and Addresses are asynchronously introduced using CE#, WE#, ALE, and CLE control pins.

The on-chip Program/Erase Controller automates all read, program, and erase functions including pulse repetition, where required, and internal verification and margining of data. A WP# pin is available to provide hardware protection against program and erase operations.

The output pin R/B# (open drain buffer) signals the status of the device during each operation. It identifies if the program/erase/read controller is currently active. The use of an open-drain output allows the Ready/Busy pins from several memories to connect to a single pull-up resistor. In a system with multiple memories the R/B# pins can be connected all together to provide a global status signal.

The Reprogram function allows the optimization of defective block management — when a Page Program operation fails the data can be directly programmed in another page inside the same array section without the time consuming serial data insertion phase.

Multiplane Copy Back is also supported. Data read out after Copy Back Read (both for single and multiplane cases) is allowed. In addition, Cache Program and Multiplane Cache Program operations improve the programing throughput by programing data using the cache register.

The devices provide two innovative features: Page Reprogram and Multiplane Page Reprogram. The Page

Reprogram re-programs one page. Normally, this operation is performed after a failed Page Program operation. Similarly, the Multiplane Page Reprogram reprograms two pages in parallel, one per plane. The first page must be in the first plane while the second page must be in the second plane. The Multiplane Page Reprogram operation is performed after a failed Multiplane Page Program operation. The Page Reprogram and Multiplane Page Reprogram guarantee improved performance, since data insertion can be omitted during reprogram operations.

The devices come with the following security features:

OTP (one time programmable) area, which is a restricted access area where sensitive data/code can be stored permanently.

Serial number (unique identifier), which allows the devices to be uniquely identified. Contact factory for support of this feature.

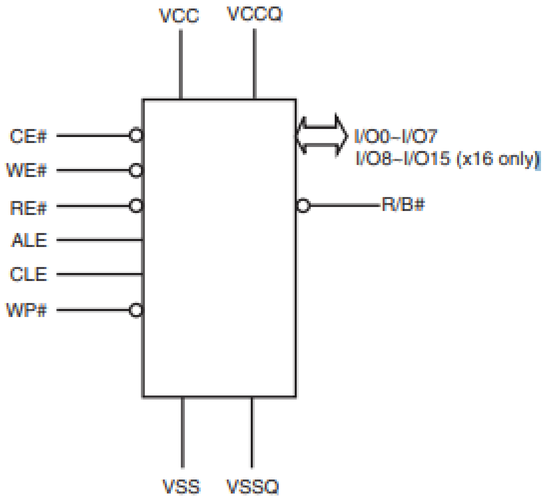


Figure 1: Logic Diagram

1.1 Functional block diagram

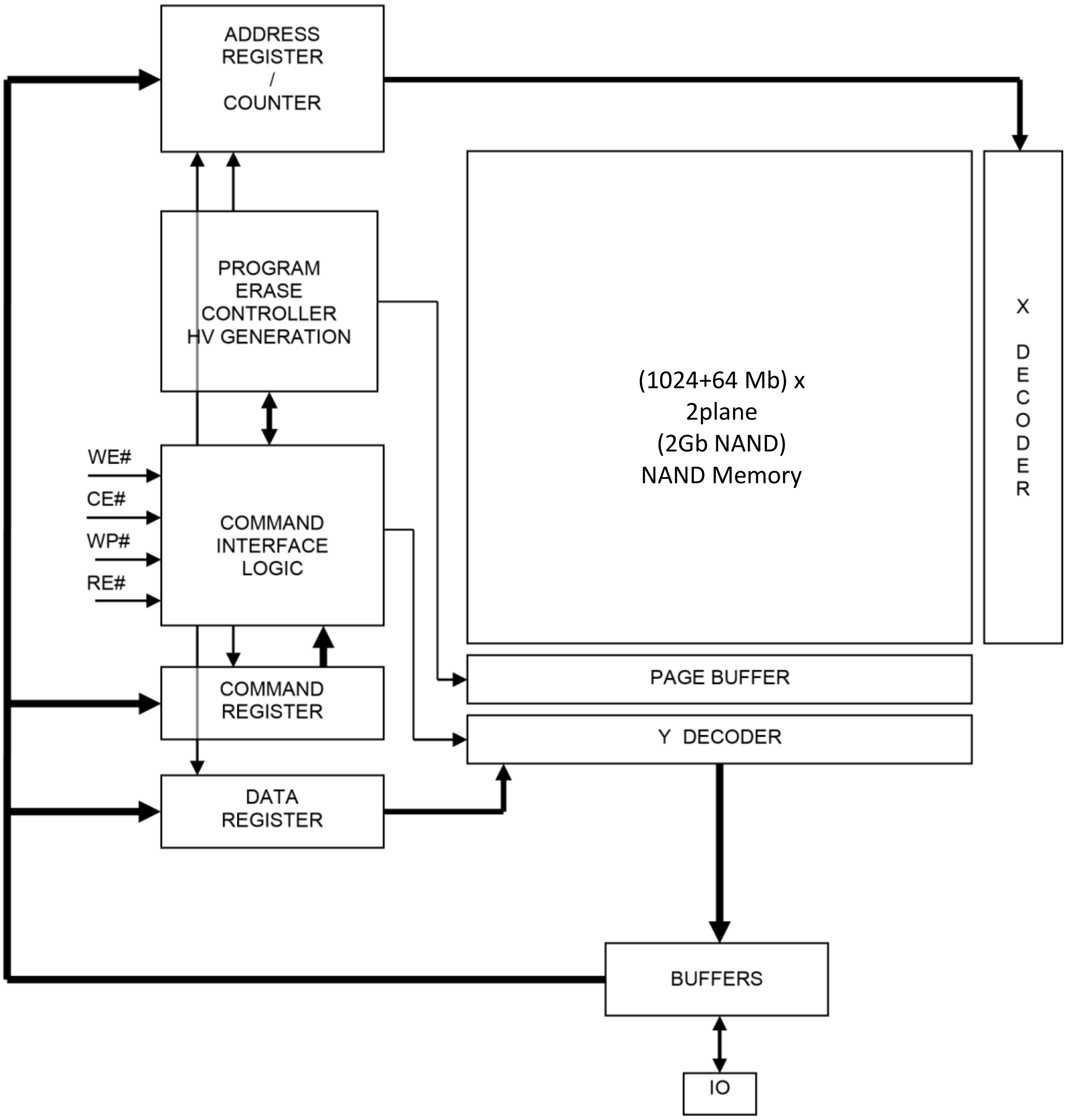


Figure 2: Functional block description

1.2 ARRAY ORGANIZATION

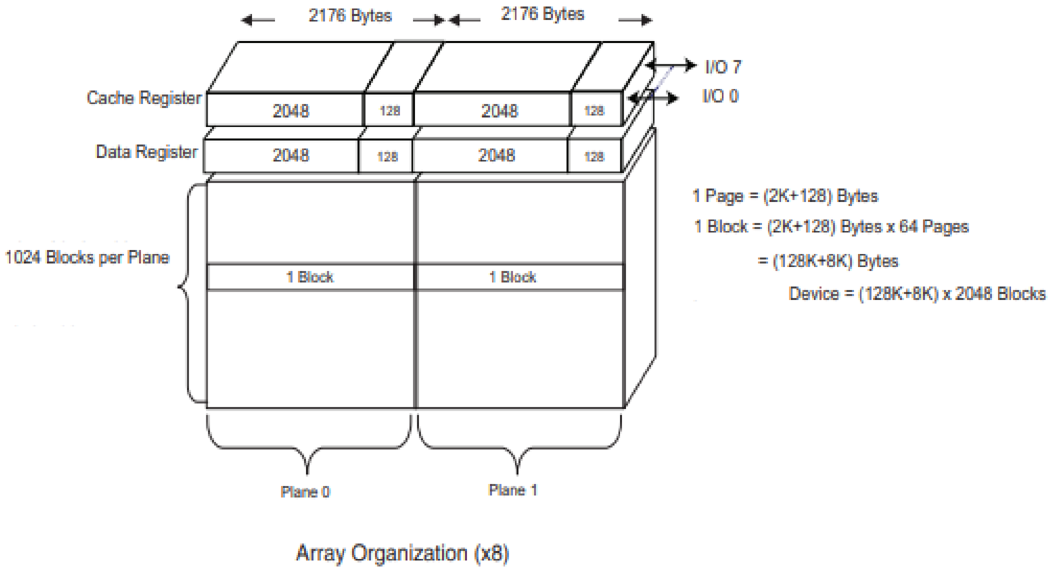


Figure 3: Array Organization

1.3 Address role

Bus cycle	I/O[15:8]	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7
				x8					
1st /Col Add. 1	-	A0	A1	A2	A3	A4	A5	A6	A7
2nd /Col Add. 2	-	A8	A9	A10	A11	Low	Low	Low	Low
3rd /Row Add. 1	-	A12	A13	A14	A15	A16	A17	A18	A19
4th /Row Add. 2	-	A20	A21	A22	A23	A24	A25	A26	A27
5th /Row Add. 3		A28	Low	Low	Low	Low	Low	Low	Low

Table 1: Address Cycle Map

Notes:
1. CAx = Column Address bit.
2. PAx = Page Address bit.
3. PLA0 = Plane Address bit zero.
4. BAx = Block Address bit.
5. Block address concatenated with page address and plane address = actual page address, also known as the row address.
6. I/O[15:8] are not used during the addressing sequence and should be driven Low.A0 – A11: byte (column) address in the page
For the x8 address bits, the following rules apply:
A0 - A11: column address in the page
A12 - A17: page address in the block
A18: plane address (for multiplane operations) / block address (for normal operations)
A19 - A28: block address

1.4 Command Set

FUNCTION	1st CYCLE	2nd CYCLE	3rd CYCLE	4th CYCLE	Acceptable command during busy
READ	00h	30h	-	-	
READ FOR COPY-BACK	00h	35h	-	-	
Page READ	00h	30h	-	-	
SPEICAL READ FOR COPY-BACK	00h	36h	-	-	
READ ID	90h	-	-	-	
READ ID2	30h-65h-00h	30h	-	-	
RESET	FFh	-	-	-	Yes
RESET CACHE	31h		-	-	
RESET CACHE ENHANCED	00h	31h	-	-	
RESET CACHE END	3Fh		-	-	
CACHE PGM (Start/continue)	80h	15h	-	-	
Multiplane CACHE PGM (Start/continue)	80h	11h	81h	15h	
COPY BACK PGM	85h	10h	-	-	
Multiplane COPY BACK PGM	85h	11h	81h	10h	
READ STATUS REGISTER	70h	-	-	-	Yes
READ STATUS ENHANCED	78h	-	-	-	
RANDOM DATA INPUT	85h	-	-	-	
RANDOM DATA OUTPUT	05h	E0h	-	-	
READ CACHE (SEQUENTIAL)	31h	-	-	-	
READ CACHE ENHANCED (RANDOM)	00h	31h	-	-	
READ PARAMETER PAGE	ECh	-	-	-	
READ ONFI SIGNATURE	90h	-	-	-	
One-time Programmable (OTP) Area Entry	29h-17h-04h-19h	-	-	-	
Multiplane PGM	80h	11h	81h	10h	
ONFI Multiplane PGM	80h	11h	80h	10h	
Multiplane PAGE REPGM	8Bh	11h	8Bh	10h	
BLOCK ERASE	60h	D0h	-	-	
Multiplane BLOCK ERASE	60h	60h	D0h	-	
ONFI Multiplane BLOCK EARSE	60h	D1h	60h	D0h	
PAGE PGM (start) / CACHE PGM (end)	80h	10h	-	-	

FUNCTION	1st CYCLE	2nd CYCLE	3rd CYCLE	4th CYCLE	Acceptable command during busy
ONFI Multiplane COPY BACK PGM	85h	11h	85h	10h	
ONFI Multiplane CACHE PGM (Start/continue)	80h	11h	80h	15h	
CACHE PGM (End)	80h	10h	-	-	
Multiplane CACHE PGM (END)	80h	11h	81h	10h	
ONFI Multiplane CACHE PGM (END)	80h	11h	80h	10h	

2 DEVICE PARAMETERS

2.1 ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Vcc = 1.8V	Unit
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO}	Input or Output Voltage	–0.6 to 2.7	V
V_{CC}	Supply Voltage	–0.6 to 2.7	V

Notes:
1. Except for the rating "Operating Temperature Range", stresses above those listed in the table **Absolute Maximum Ratings** ***may cause permanent damage to the***
device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification
is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.
2. Minimum Voltage may undershoot to -2V during transition and for less than 20 ns during transitions.
3. Maximum Voltage may overshoot to VCC +2.0V during transition and for less than 20 ns during transitions.

2.2 RECOMMENDED OPERATING CONDITIONS

(Voltage reference to GND, T_C = -40 to +85℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	VCC	1.7	1.8	1.95	V
Supply Voltage	VSS	0	0	0	V

2.3 DC AND OPERATION CHARACTERISTICS

Parameter		Symbol	Test Conditions	Vcc=1.8Volt			Unit
				Min	Typ	Max	
Operating Current	Read	I_{CC1}	t_{RC} = t_{RC}(min), CE#=V_{IL}, I_{OUT}=0mA	-	15	30	mA
	Program	I_{CC2}	-	-	15	30	mA
	Erase	I_{CC3}	-	-	15	30	mA
Stand-by Current (TTL)		I_{CC4}	CE#=V_{IH}, WP#=0V/V_{CC}	-	-	1	mA
Stand-By Current (CMOS)		I_{CC5}	CE#=V_{CC}-0.2, WP#=0/V_{CC}	-	10	50	uA
Input Leakage Current		I_{LI}	V_{IN}=0 to Vcc (max)	-	-	±10	uA
Output Leakage Current		I_{LO}	V_{OUT}=0 to Vcc (max)	-	-	±10	uA
Input High Voltage		V_{IH}	-	0.8 x V_{CC}	-	V_{CC} +0.3	V

Parameter	Symbol	Test Conditions	Vcc=1.8Volt			Unit
			Min	Typ	Max	
Input Low Voltage	V_{IL}	-	-0.3	-	0.2 x V_{CC}	V
Output High Voltage Level	V_{OH}	I_{OH} = -100uA	V_{CC}-0.1	-	-	V
Output Low Voltage Level	V_{OL}	I_{OL} = 100uA	-	-	0.1	V
Output Low Current (RB#)	I_{OL} (RB#)	V_{OL}=0.1V	3	4	-	mA
Erase and Program lockout Voltage	V_{LKO}	-	-	1.1	-	V

2.4 VALID BLOCK

Symbol	Min.	Typ.	Max.	Unit
NVB	2008	-	2048	Blocks

NOTE:
The First block (Block 0) is guaranteed to be a valid block at the time of shipment.
The specification for the minimum number of valid blocks is applicable over lifetime.

2.5 AC TEST CONDITION

(T_C= -40 to +85℃, V_{CC}=1.7V~1.95V)

Parameter	Condition
Input Pulse Levels	0V to V_{CC}
Input Rise and Fall Times	5 ns
Input and Output Timing Levels	V_{CC} /2
Output Load	1 TTL Gate and C_L=30pF

2.6 PIN CAPACITANCE

(T_C=25℃, V_{CC}=1.8V, f=1.0MHz)

Item	Symbol	Test Condition	Min.	Max.	Unit
Input / Output Capacitance	CI/O	V_{IL} = 0V	-	10	pF
Input Capacitance	C_{IN}	V_{IN} = 0V	-	10	pF

2.7 MODE SELECTION

CLE	ALE	CE#	WE#	RE#	WP#	MODE

CLE	ALE	CE#	WE#	RE#	WP#	MODE	
H	L	L	Rising	H	X	Read Mode	Command Input
L	H	L	Rising	H	X		Address Input
H	L	L	Rising	H	H	Write Mode	Command Input
L	H	L	Rising	H	H		Address Input
L	L	L	Rising	H	H	Data Input	
L	L	L	H	Falling	X	Data Output (on going)	
X	X	X	H	H	X	Data Output (suspended)	
X	X	X	H	H	X	Busy time in Read	
X	X	X	X	X	H	Busy time in Program	
X	X	X	X	X	H	Busy time in Erase	
X	X	X	X	X	L	Write Protect	
X	X	H	X	X	0V / V_{CC}	Stand By	

NOTE:
1. ***X can be VIL or VIH.***
2. ***WP# should be biased to CMOS high or CMOS low for standby.***
3. ***During Busy Time in Read, RE# must be held high to prevent unintended data out.***

2.8 Program / Erase Characteristics

Parameter		Symbol	Min	Typ	Max	Unit
Program Time/Multiplane Program Time		t_{PROG}	-	300	700	us
During Busy time for Multiplane Programe		t_{DBSY}	-	0.5	1	us
Cache program short busy time		t_{PCBSY}	-	5	t_{PROG}	us
Number of partial Program Cycles in the same page	Main + Spare Array	NOP	-	-	4	Cycle
Block Erase Time		t_{BERS}	-	3.5	10	ms
Read Cache busy time		t_{RCBSY}		5	t_R	us

Table: Address Cycle Map

NOTE:
1. ***Typical program time is defined as the time within which more than 50% of the whole pages are programmed (VCC = 1.8V, 25°C).***
2. ***Copy Back Read and Copy Back Program for a given plane must be between odd address pages or between even address pages for the device to meet the program time (tPROG) specification. Copy Back Program may not meet this specification when copying from an odd address page (source page) to an even address page (target page) or from an even address page (source page) to an odd address page (target page).***

2.9 AC Timing Characteristics for Command / Address / Data Input

Parameter	Symbol	Min.	Max.	Unit
CLE Setup Time	t_{CLS}	25	-	ns
CLE Hold Time	t_{CLH}	10	-	ns
CE# Setup Time	t_{CS}	35	-	ns
CE# Hold Time	t_{CH}	10	-	ns
WE# Pulse Width	t_{WP}	25	-	ns
ALE Setup Time	t_{ALS}	25	-	ns
ALE Hold Time	t_{ALH}	10	-	ns
Data Setup Time	t_{DS}	20	-	ns
Data Hold Time	t_{DH}	10	-	ns
Write Cycle Time	t_{WC}	45	-	ns
WE# High Hold Time	t_{WH}	15	-	ns
Address to Data Loading Time	t_{ADL}	100	-	ns

2.10 AC Characteristics for Operation

Parameter	Symbol	Min.	Max.	Unit
CE# high to output High Z	t_{CHZ}	-	30	ns
Data transfer from cell to register	t_{R}	-	30	us
RE# pulse width	t_{RP}	25	-	ns
ALE to RE# delay	t_{AR}	10	-	ns
CE Low to RE# Low	t_{CR}	10	-	ns
CE to RE# delay	t_{CLR}	10	-	ns
CE# high to output hold	t_{CCH}	15	-	ns
CE# high to ALE or CLE don't care	t_{CBD}	10	-	ns
Output High-Z to RE# low	t_{IR}	0	-	ns
Read cycle time	t_{RC}	45	-	ns
RE# access time	t_{REA}	-	30	ns
RE# high hold time	t_{REH}	15	-	ns
RE# high to output hold	t_{RHOH}	15	-	ns
RE# high to WE# low	t_{RHW}	100	-	ns
RE# high to output High-Z	t_{RHZ}	-	100	ns
RE# low to output hold	t_{RLOH}	-	-	ns
Ready to RE# low	t_{RR}	20	-	ns
Device resetting time (Read/Program/Erase)	t_{RST}	-	5/10/500	us
WE# high to busy	t_{WB}	-	100	ns
WE# high to RE# low	t_{WHR}	60	-	ns
WE# high to RE# low for Random data out	t_{WHR2}	200	-	ns
Write protect time	t_{WW}	100	-	ns

NOTE:
1. The time to Ready depends on the value of the pull-up resistor tied to R/B# pin.
2. If Reset Command (FFh) is written at Ready state, the device goes into Busy for maximum 5 μs.
3. CE# low to high or RE# low to high can be at different times and produce three cases. Depending on which signal comes high first, either tCOH or tRHOH will be met.

3 BUS OPERATION

3.1 Command Input.

Command Input bus operation is used to give a command to the memory device. Command are accepted with Chip Enable low, Command Latch Enable High, Address Latch Enable low and Read Enable High and latched on the rising edge of Write Enable. Moreover for commands that starts a modify operation (write/erase) the Write Protect pin must be high. See Figure Command Latch Cycle and Table Program/Erase Characteristics for details of the timings requirements. Command codes are always applied on IO<7:0>.

3.2 Address Input.

Address Input bus operation allows the insertion of the memory address. To insert the **28 addresses** needed to access the 5 **clock cycles (x8 version)** are needed. Addresses are accepted with Chip Enable low, Address Latch Enable High, Command Latch Enable low and Read Enable High and latched on the rising edge of Write Enable. Moreover for commands that starts a modify operation (write/erase) the Write Protect pin must be high. See Figure Address Latch Cycle and Table Program/Erase Characteristics for details of the timings requirements. Addresses are always applied on IO<7:0>.

3.3 Data Input.

Data Input bus operation allows to feed to the device the data to be programmed. The data insertion is serially and timed by the Write Enable cycles. Data are accepted only with Chip Enable low, Address Latch Enable low, Command Latch Enable low, Read Enable High, and Write Protect High and latched on the rising edge of Write Enable. See Figure Input Data Latch Cycle and Table Program/Erase Characteristics for details of the timings requirements.

3.4 Data Output.

The Data Output bus operation allows data to be read from the memory array and to check the Status Register content, and the ID data. Data can be serially shifted out by toggling the Read Enable pin with Chip Enable low, Write Enable high, Address Latch Enable low, and Command Latch Enable low.

3.5 Write Protect.

The Hardware Write Protection is activated when the Write Protect pin is low. In this condition, modify operations do not start and the content of the memory is not altered. The Write Protect pin is not latched by Write Enable to ensure the protection even during power up.

3.6 Standby.

In Standby the device is deselected, outputs are disabled and Power Consumption reduced.

4 DEVICE OPERATION

4.1 Page Read.

Upon initial device power up, the device defaults to Read mode. This operation is also initiated by writing 00h and 30h to the command register along with 5 address cycles. In two consecutive read operations, the second one does need 00h command, which 5 address cycles and 30h command initiates that operation. Second read operation always requires setup command if first read operation was executed using also random data out command.

Two types of operations are available: random read, serial page read. The random read mode is enabled when the page address is changed. The 2176 bytes of data within the selected page are transferred to the data registers in less than 25 us(tR). The system controller may detect the completion of this data transfer (tR) by analyzing the output of R/B pin. Once the data in a page is loaded into the data registers, they may be read out in 45 ns cycle time by sequentially pulsing RE#. The repetitive high to low transitions of the RE# clock make the device output the data starting from the selected column address up to the last column address.

The device may output random data in a page instead of the consecutive sequential data by writing random data output command.

The column address of next data, which is going to be out, may be changed to the address which follows random data output command.

Random data output can be operated multiple times regardless of how many times it is done in a page.

After power up, device is in read mode so 00h command cycle is not necessary to start a read operation. Any operation other than read or random data output causes device to exit read mode. Check Figure Read Operation (Read One Page), Figure Read Operation Intercepted by CE#, Figure Random Data Output as references.

4.2 Read Cache

The Read Cache function permits a page to be read from the page register while another page is simultaneously read from the Flash array. A Read Page command, as defined in 4.1, shall be issued prior to the initial sequential or random Read Cache command in a read cache sequence.

The Read Cache function may be issued after the Read function is complete (SR[6] is set to one). The host may enter the address of the next page to be read from the Flash array. Data output always begins at column address 00h. If the host does not enter an address to retrieve, the next sequential page is read. When the Read Cache function is issued, SR[6] is cleared to zero (busy). After the operation is begun SR[6] is set to one (ready) and the host may begin to read the data from the previous Read or Read Cache function. Issuing an additional Read Cache function copies the data most recently read from the array into the page register. When no more pages are to be read, the final page is copied into the page register by issuing the 3Fh command. The host may begin to read data from the page register when SR[6] is set to one (ready). When the 31h and 3Fh commands are issued, SR[6] shall be cleared to zero (busy) until the page has finished being copied from the Flash array. The host shall not issue a sequential Read Cache (31h) command after the last page of the device is read. Figure Read Cache Timings, Start of Cache Operation defines the Read Cache behavior and timings for the beginning of the cache operations subsequent to a Read command being issued. SR[6] conveys whether the next selected page can be read from the page register. Figure Read Cache Timings, End of Cache Operation defines the Read Cache behavior and timings for the end of cache operation.

Note: The Read Cache and Read Cache End commands reset the column counter, thus, when RE# is toggled to output the data of a given page, the first output data is related to the first byte of the page (column address 00h). Random Data Output command can be used to switch column address.

4.3 Page Program.

The device is programmed basically by page, but it does allow multiple partial page programming of a word or consecutive bytes up to 2176 (X8 device), in a single page program cycle.

A page program cycle consists of a serial data loading period in which up to 2176 bytes (X8 device) of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell.

The serial data loading period begins by inputting the Serial Data Input command (80h), followed by the 5 cycle address inputs and then serial data. The words other than those to be programmed do not need to be loaded. The device supports random data input in a page. The column address of next data, which will be entered, may be changed to the address which follows random data input command (85h). Random data input may be operated multiple times regardless of how many times it is done in a page.

The Page Program confirm command (10h) initiates the programming process. The internal write state controller automatically executes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the RB# output, or the Status bit (I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit (I/O 0) may be checked. The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register. Figure Page Program Operation and Figure Random Data In detail the sequence.

4.4 Copy-Back Program.

The copy-back program is configured to quickly and efficiently rewrite data stored in one page without utilizing an external memory. Since the time-consuming cycles of serial access and re-loading cycles are removed, the system performance is improved. The benefit is especially obvious when a portion of a block is updated and the rest of the block is also needed to be copied to the newly assigned free block. The operation for performing a copy-back program is a sequential execution of page-read without serial access and copying-program with the address of destination page. A read operation with "35h" command and the address of the source page moves the whole 2176byte (X8 device) data into the internal data buffer. As soon as the device returns to Ready state, optional data read-out is allowed by toggling RE#, or Copy Back command (85h) with the address cycles of destination page may be written. The Program Confirm command (10h) is required to actually begin the programming operation. Data input cycle for modifying a portion or multiple distant portions of the source page is allowed as shown in Figure Copy Back Program With Random Data Input.

4.4.1 Multiplane Copy-Back Program.

Multiplane Copy Back Program must be preceded by two single page Copy Back Read command sequences (1st page must be read from the 1st plane and 2nd page from the 2nd plane).

Multiplane Copy Back cannot cross plane boundaries — the contents of the source page of one device plane can be copied only to a destination page of the same plane.

The Multiplane Copy Back Program sequence represented in Figure Multiplane Copy Back Program shows the legacy protocol. In this case, the block address bits for the first plane are all zero and the second address issued selects the block for both planes. Figure Multiplane Copy Back Program describes the sequence using the ONFI protocol. For both addresses issued in this protocol, the block address bits must be the same except for the bit(s) that select the plane.

If a Multiplane Copy Back Program operation is interrupted by hardware reset, power failure or other means, the host must ensure that the interrupted pages are not used for further reading or programming operations until the next uninterrupted block erases are complete for the applicable blocks.

4.4.2 Special Read for Copy Back.

This device support Special Read for Copy Back. If Copy Back Read (described in Copy Back Program and “Multiplane Copy Back Program) is triggered with confirm command ‘36h’ instead ‘35h’, Copy Back Read from target page(s) will be executed with an increased internal (VPASS) voltage.

This special feature is used in order to minimize the number of read errors due to over-program or read disturb — it shall be used only if ECC read errors have occurred in the source page using Page Read or Copy Back Read sequences.

Excluding the Copy Back Read confirm command, all other features described in Copy Back Program and Multiplane Copy Back Program for standard copy back remain valid (including the figures referred to in those sections).

4.5 Cache Program

4.5.1 4.5.1 Cache program

Cache Program is an extension of the standard page program which is executed with two 2112 bytes(x8 device) registers. The Cache program operation cannot cross a block boundary. The cache program allows new data to be input while the previous data that was transferred to the data register is programmed into the memory array.

After the serial data input command (80h) is loaded to the command register, followed by 5 cycles of address, a full or partial page of data is latched into the cache register.

Once the cache write command (15h) is loaded to the command register, the data in the cache register is transferred into the data register for cell programming. At this time the device remains in Busy state for a short time (tPCBSY). After all data of the cache register are transferred into the data register, the device returns to the Ready state, and allows loading the next data into the cache register through another cache program command sequence (80h-15h).

The busy time following the first sequence 80h–15h equals the time needed to transfer the data of cache register to the data register. Cell programming of the data of data register and loading of the next data into the cache register is consequently processed through a pipeline model.

In case of any subsequent sequence 80h–15h, transfer from the cache register to the data register is held off until cell programming of current data register contents is complete; till this moment the device will stay in a busy state (tPCBSY).

Read Status commands (70h) may be issued to check the status of the different registers, and the pass/fail status of the cached program operations. More in detail:

The Cache-Busy status bit I/O<6> indicates when the cache register is ready to accept new data.

the status bit I/O<5> can be used to determine when the cell programming of the current data register contents is complete

The cache program error bit I/O<1> can be used to identify if the previous page (page N-1) has been successfully programmed or not in cache program operation. The latter can be polled upon I/O<6> status bit changing to "1".

The error bit I/O<0> is used to identify if any error has been detected by the program / erase controller while programming page N. The latter can be polled upon I/O<5> status bit changing to "1".

I/O<1> may be read together with I/O<0>.

If the system monitors the progress of the operation only with R/B#, the last page of the target program sequence must be programmed with Page Program Confirm command (10h). If the Cache Program command (15h) is used instead, the status bit I/O<5> must be polled to find out if the last programming is finished before starting any other operation. Figure Cache Program Start/Cache Program End detail the sequence.

4.5.2 Multiplane Cache program

The Multiplane Cache Program enables high program throughput by programming two pages in parallel, while exploiting the data and cache registers of both planes to implement cache.

The command sequence can be summarized as follows:

■ Serial Data Input command (80h), followed by the five cycle address inputs and then serial data for the 1st page. Address for this page must be within 1st plane (PLA0 = 0). The data of 1st page other than those to be programmed do not need to be loaded. The device supports Random Data Input exactly like Page Program operation.

■ The Dummy Page Program Confirm command (11h) stops 1st page data input and the device becomes busy for a short time (tDBSY).

■ Once device returns to ready again, 81h command must be issued, followed by 2nd page address

(5 cycles) and its serial data input. Address for this page must be within 2nd plane (PLA0 = 1). The data of 2nd page other than those to be programmed do not need to be loaded.

■ Cache Program confirm command (15h). Once the cache write command (15h) is loaded to the command register, the data in the cache registers is transferred into the data registers for cell programming. At this time the device remains in the Busy state for a short time (tCBSYW). After all data from the cache registers are transferred into the data registers, the device returns to the Ready state, and allows loading the next data into the cache register through another Cache Program command sequence.

The sequence 80h-...- 11h...-...81h...-...15h can be iterated, and each time the device will be busy for the tCBSYW time needed to complete programming the current data register contents, and transferring the new data from the cache registers. The sequence to end Multiplane Cache Program is 80h-...- 11h...-...81h...-...10h.

The Multiplane Cache Program is available only within two paired blocks in separate planes. Figure Multiplane Cache Program shows the legacy protocol for the Multiplane Cache Program operation. In this case, the block address bits for the first plane are all zero and the second address issued selects the block for both planes. Figure Multiplane Cache Program(ONFI) shows the ONFI protocol for the Multiplane Cache Program operation. For both addresses issued in this protocol, the block address bits must be the same except for the bit(s) that select the plane.

The user can check operation status by R/B# pin or Read Status Register commands (70h or 78h). If the user opts for 70h, Read Status Register will provide “global” information about the operation in the two planes.

■ I/O6 indicates when both cache registers are ready to accept new data.

■ I/O5 indicates when the cell programming of the current data registers is complete.

■ I/O1 identifies if the previous pages in both planes (pages N-1) have been successfully programmed or not. This status bit is valid upon I/O6 status bit changing to 1.

■ I/O0 identifies if any error has been detected by the program/erase controller while programming the two pages N. This status bit is valid upon I/O5 status bit changing to 1.

If the system monitors the progress of the operation only with R/B#, the last pages of the target program sequence must be programmed with Page Program Confirm command (10h). If the Cache Program command (15h) is used instead, the status bit I/O5 must be polled to find out if the last programming is finished before starting any other operation. Refer to “4.7 Read Status Register” for further information.

If a Multiplane Cache Program operation is interrupted by hardware reset, power failure or other means, the host must ensure that the interrupted pages are not used for further reading or programming operations until the next uninterrupted block erases are complete for the applicable blocks.

4.6 . Block Erase

4.6.1 Block Erase

The Erase operation is done on a block basis. Block address loading is accomplished in two cycles initiated by an Erase Setup command (60h). Only address A18 to A28 (X8) is valid while A12 to A17 (X8) are ignored. The Erase Confirm command (D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions.

At the rising edge of WE# after the erase confirm command input, the internal write controller handles erase and erase-verify.

Once the erase process starts, the Read Status Register command (70h or 78h) may be entered to read the status register. The system controller can detect the completion of an erase by monitoring the RB# output, or the Status bit (I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while erasing is in progress. When the erase operation is completed, the Write Status Bit (I/O 0) may be checked.

If a Block Erase operation is interrupted by hardware reset, power failure or other means, the host must ensure that the interrupted block is erased under continuous power conditions before that block can be trusted for further programming and reading operations.

4.6.2 Multiplane Block Erase

The Block Erase operation is done on a block basis. Block address loading is accomplished in three cycles initiated by an Erase Setup command (60h). Only the block address bits are valid while the page address bits are ignored.

Multiplane Block Erase allows the erase of two blocks in parallel, one block per memory plane.

The Block erase setup command (60h) must be repeated two times, followed by 1st and 2nd block address respectively (3 cycles each). As for block erase, D0h command makes embedded operation start. In this case, multiplane erase does not need any Dummy Busy Time between 1st and 2nd block insertion.

For the Multiplane Block Erase operation, the address of the first block must be within the first plane

(PLA0 = 0) and the address of the second block in the second plane (PLA0 = 1). See Figure Multiplane Block Erase for a description of the legacy protocol. In this case, the block address bits for the first plane are all zero and the second address issued selects the block for both planes. Figure Multiplane Block Erase describes the sequences using the ONFI protocol. For both addresses issued in this protocol, the block address bits must be the same except for the bit(s) that select the plane.

The user can check operation status by monitoring R/B# pin or reading the Status Register (command 70h or 78h). The Read Status Register command is also available during Dummy Busy time (tDBSY). In case of failure in either erase, the fail bit of the Status Register will be set. Refer to “Read Status Register” for further information.

If a Multiplane Block Erase operation is interrupted by hardware reset, power failure or other means, the host must ensure that the interrupted blocks are erased under continuous power conditions before those blocks can be trusted for further programming and reading operations.

4.7 Read Status Register.

The Status Register is used to retrieve the status value for the last operation issued.

Read Status Enhanced is used to retrieve the status value for a previous operation in the specified plane.

Figure Read Status Enhanced Timing defines the Read Status Enhanced behavior and timings. The plane and die address must be specified in the command sequence in order to retrieve the status of the die and the plane of interest.

Refer to Table Status Register Coding for specific Status Register definitions. The command register remains in Status Read mode until further commands are issued.

The Status Register is dynamic; the user is not required to toggle RE# / CE# to update it.

4.8 Read Status Register field definition

Table below lists the meaning of each bit of Read Status Enhanced

IO	Page Program	Block Erase	Read	Cache Read	Cache Program / Cache reprogram	CODING
0	Pass / Fail	Pass / Fail	NA	NA	Pass/Fail	N page Pass: ‘0’ Fail: ‘1’
1	NA	NA	NA	NA	Pass/Fail	N-1page Pass: ‘0’ Fail: ‘1’
2	NA	NA	NA	NA	NA	-
3	NA	NA	NA	NA	NA	-
4	NA	NA	NA	NA	NA	-
5	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	Ready /Busy	Active: ‘0’ Idle:’1’
6	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	Data cache Read/Busy Busy: ‘0’ Ready:’1’
7	Write Protect	Write Protect	Write Protect	Write Protect	Write Protect	Protected: ‘0’ Not Protected: ‘1’

Table 2: Status Register Coding

4.9 Read ID.

The device contains a product identification mode, initiated by writing **90h** to the command register, followed by an address input of 00h.

DENSITY	ORG.	VCC	1st	2nd	3rd	4th	5th
2G bits	X8	1.8V	01h	AAh	90h	15h	46h

Table 3: Read ID for supported configurations

DEVICE IDENTIFIER BYTE	DESCRIPTION
1st	Manufacturer Code

DEVICE IDENTIFIER BYTE	DESCRIPTION
2nd	Device Identifier
3rd	Internal chip number, cell type.etc.
4th	Page Size, Block Size, Spare Size, Serial Access Time, Organization
5th	ECC, Multiplane information

Table 4: Read ID bytes meaning

	Description	DQ7	DQ6	DQ5-4	DQ3-2	DQ1-0
Internal Chip Number	1 2 4 8					00 01 10 11
Cell Type	2 Level Cell 4 Level Cell 8 Level Cell 16 Level Cell				00 01 10 11	
Number of simultaneously programmed pages	1 2 4 8			00 01 10 11		
Interleaved program between multiple dice	Not Supported Supported		0 1			
Cache Program	Not Supported Supported	0 1				

Table 5: 3rd byte of Device Identifier Description

	Description	I/O7	I/O 6	I/O 5-4	I/O 3	I/O 2	DQ1-0
Page size (without spare area)	1kB 2kB 4kB 8kB						00 01 10 11
Block size (without spare area)	64 kB 128 kB 256 kB 512 kB			00 01 10 11			
Spare Area Size (byte/512 byte)	8 16					0 1	
Serial Access Time	45 ns 25 ns Reserved Reserved	0 0 1 1			0 1 0 1		
Organization	x8		0				

Table 6: 4th byte of Device Identifier Description

	Description	I/O7	I/O 6-4	I/O 3-2	DQ1-0
ECC Level	1 bit / 512 bytes 2 bit / 512 bytes 4 bit / 512 bytes 8 bit / 512 bytes				0 0 0 1 1 0 1 1
Plane Number	1 2 4 8			0 0 0 1 1 0 1 1	
Plane Size (without spare area)	64 Mb 128 Mb 256 Mb 512 Mb 1 Gb 2 Gb 4 Gb		0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0		
Reserved		0			

Table 7: 5th Byte of Read ID Description

4.10 Reset.

The Reset feature is executed by writing FFh to the command register. If the device is in the Busy state during random read, program, or erase mode, the Reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data may be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value E0h when WP# is high or value 60h when WP# is low. If the device is already in reset state a new Reset command will not be accepted by the command register. The R/B# pin transitions to low for tRST after the Reset command is written. Refer to Figure Reset Operation Timing for further details. The Status Register can also be read to determine the status of a Reset operation.

4.11 Read Parameter Page

The device supports the ONFI Read Parameter Page operation, initiated by writing ECh to the command register, followed by an address input of 00h. The host may monitor the R/B# pin or wait for the maximum data transfer time (tR) before reading the Parameter Page data. The command register remains in Parameter Page mode until further commands are issued to it. If the Status Register is read to determine when the data is ready, the Read Command (00h) must be issued before starting read cycles.

Note: For UNIIC MCP, for a particular condition, the Read Parameter Page command does not give the correct values. To overcome this issue, the host must issue a Reset command before the Read Parameter Page command.

Issuance of Reset before the Read Parameter Page command will provide the correct values and will not output 00h values.

4.12 Parameter Page Data Structure Definition

Byte	O/M	Description	Value
		Revision information and features block	
0-3	M	Parameter page signature Byte 0: 4Fh, "O" Byte 1: 4Eh, "N" Byte 2: 46h, "F" Byte 3: 49h, "I"	4Fh, 4Eh, 46h, 49h
4-5	M	Revision number 2-15 Reserved (0) 1 1 = supports ONFI version 1.0 0 Reserved (0)	02h, 00h
6-7	M	Features supported 5-15 Reserved (0) 4 1 = supports odd to even page Copyback 3 1 = supports interleaved operations 2 1 = supports non-sequential page Programming 1 1 = supports multiple LUN operations 0 1 = supports 16-bit data bus width	1Ch, 00h
8-9	M	Optional commands supported 6-15 Reserved (0) 5 1 = supports Read Unique ID 4 1 = supports Copyback 3 1 = supports Read Status Enhanced 2 1 = supports Get Features and Set Features 1 1 = supports Read Cache 18ntegrit 0 1 = supports Page Cache Program command	3Bh, 00h
10-31		Reserved (0)	00h
	Manufacture information block		
32-43	M	Device manufacturer (12 ASCII characters)	53h, 4Bh, 20h, 48h, 59h, 4Eh, 49h, 58h, 20h, 20h, 20h, 20h
44-63	M	Device model (20 ASCII characters)	48h, 32h, 37h, 53h, 32h, 47h, 38h, 46h, 32h, 44h, 4Bh, 41h, 2Dh, 42h, 4Dh, 20h, 20h, 20h, 20h, 20h
64	M	JEDEC manufacturer ID	ADh
65-66	O	Date code	00h
67-79		Reserved (0)	00h
	Memory organization block		

Byte	O/M	Description	Value
80-83	M	Number of data bytes per page	00h, 08h, 00h, 00h
84-85	M	Number of spare bytes per page	80h, 00h
86-89	M	Number of data bytes per partial page	00h, 00h, 00h, 00h
90-91	M	Number of spare bytes per partial page	00h, 00h
92-95	M	Number of pages per block	40h, 00h, 00h, 00h
96-99	M	Number of blocks per logical unit (LUN)	00h, 08h, 00h, 00h
100	M	Number of logical units (LUNs)	01h
101	M	Number of address cycles 4-7 Column address cycles 0-3 Row address cycles	23h
102	M	Number of bits per cell	01h
103-104	M	Bad blocks maximum per LUN	28h, 00h
105-106	M	Block endurance	05h, 04h
107	M	Guaranteed valid blocks at beginning of target	01h
108-109	M	Block endurance for guaranteed valid blocks	05h, 04h
110	M	Number of programs per page	04h
111	M	Partial programming attributes 5-7 Reserved 4 1 = partial page layout is partial page data followed by partial page spare 1-3 Reserved 0 1 = partial page programming has constraints	00h
112	M	Number of bits ECC correctability	04h
113	M	Number of interleaved address bits 4-7 Reserved (0) 0-3 Number of interleaved address bits	01h
114	O	Interleaved operation attributes 4-7 Reserved (0) 3 Address restrictions for program cache 2 1 = program cache supported 1 1 = no block address restrictions 0 Overlapped / concurrent interleaving support	04h
115-127		Reserved (0)	00h
	Electrical parameters block		
128	M	I/O pin capacitance	0Ah
129-130	M	Timing mode support	

Byte	O/M	Description	Value
		6-15 Reserved (0) 5 1 = supports timing mode 5 4 1 = supports timing mode 4 3 1 = supports timing mode 3 2 1 = supports timing mode 2 1 1 = supports timing mode 1 0 1 = supports timing mode 0, shall be 1	03h, 00h
131-132	O	Program cache timing mode support 6-15 Reserved (0) 5 1 = supports timing mode 5 4 1 = supports timing mode 4 3 1 = supports timing mode 3 2 1 = supports timing mode 2 1 1 = supports timing mode 1 0 1 = supports timing mode 0	03h, 00h
133-134	M	t_{PROG} Maximum page program time (µs)	BCh, 02h
135-136	M	t_{BERS} Maximum block erase time (µs)	10h, 27h
137-138	M	t_R Maximum page read time (µs)	1Eh, 00h
139-140	M	t_{CCS} Minimum Change Column setup time (ns)	3Ch, 00h
141-163		Reserved (0)	00h
	Vendor block		
164-165	M	Vendor specific Revision number	00h
166-253		Vendor specific	00h
254-255	M	Integrity CRC	1Fh, AAh
	Redundant Parameter Pages		
256-511	M	Value of bytes 0-255	Repeat Value of bytes 0-255
512-767	M	Value of bytes 0-255	Repeat Value of bytes 0-255
768+	O	Additional redundant parameter pages	FFh

Table 8: Parameter page data

Note : “O” stands for Optional, “M” for Mandatory

4.13 One-Time Programmable (OTP) Entry

The device contains a one-time programmable (OTP) area, which is accessed by writing 29h-17h-04h-19h to the command register. The device is then ready to accept Page Read and Page Program commands (refer to Page Read and “Page Program”). The OTP area is of a single erase block size, and hence only row addresses between 00h and 3Fh are allowed. The host must issue the Reset command (refer to “Reset”) to exit the OTP area and access the normal flash array. The Block Erase command is not allowed in the OTP area. Refer to Figure OTP Entry Timing for more detail on the OTP Entry command sequence.

5 TIMING DIAGRAMS

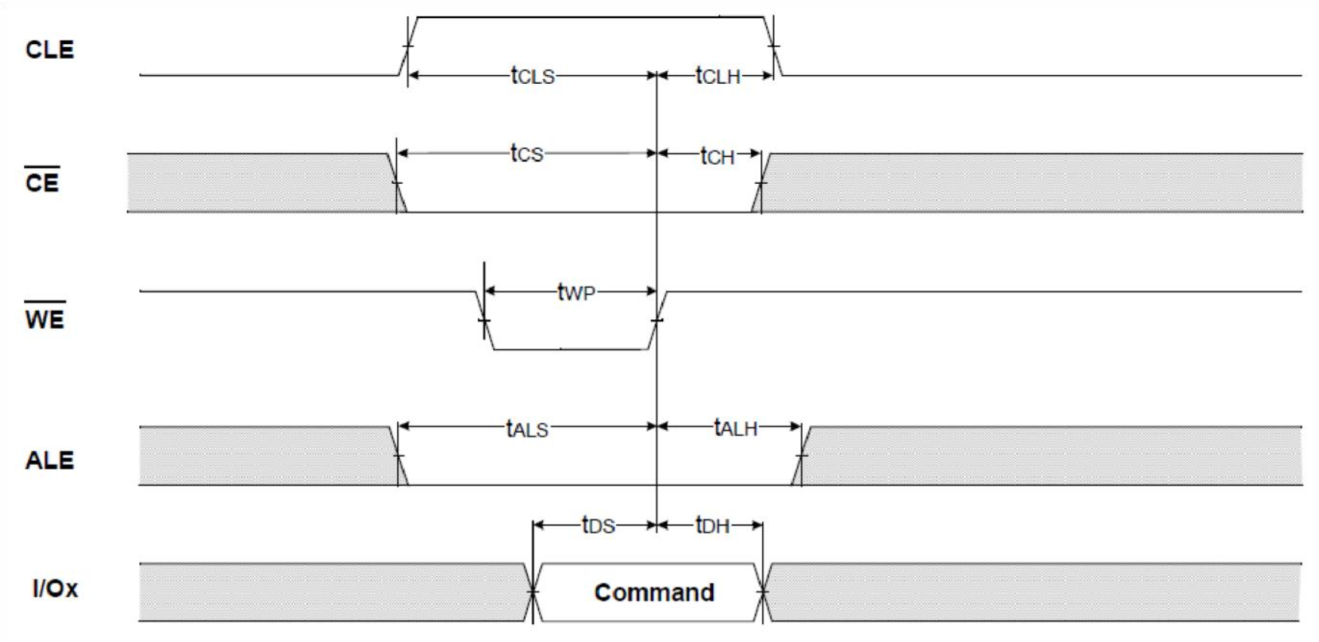


Figure 4: Command Latch Cycle

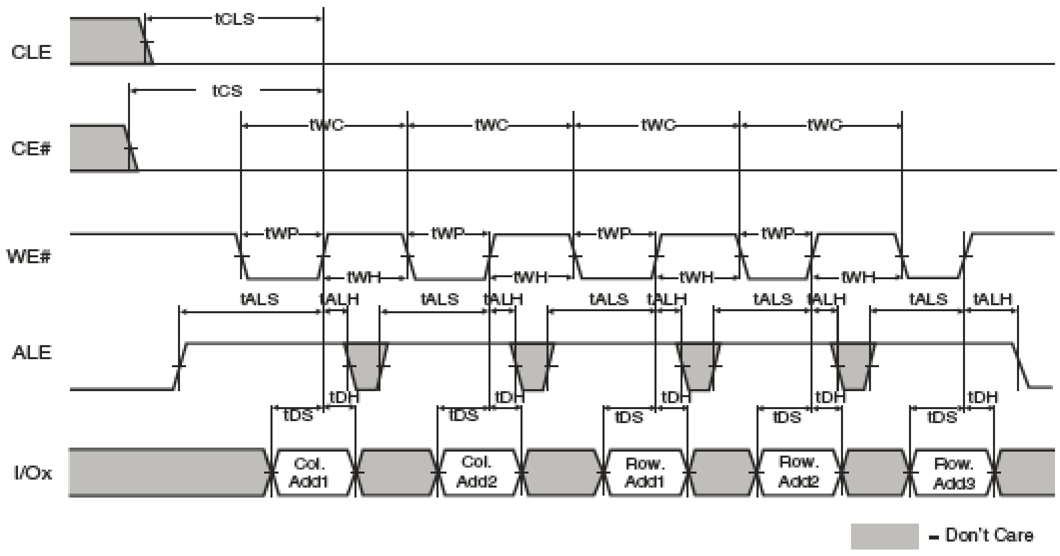


Figure 5: Address Latch Cycle

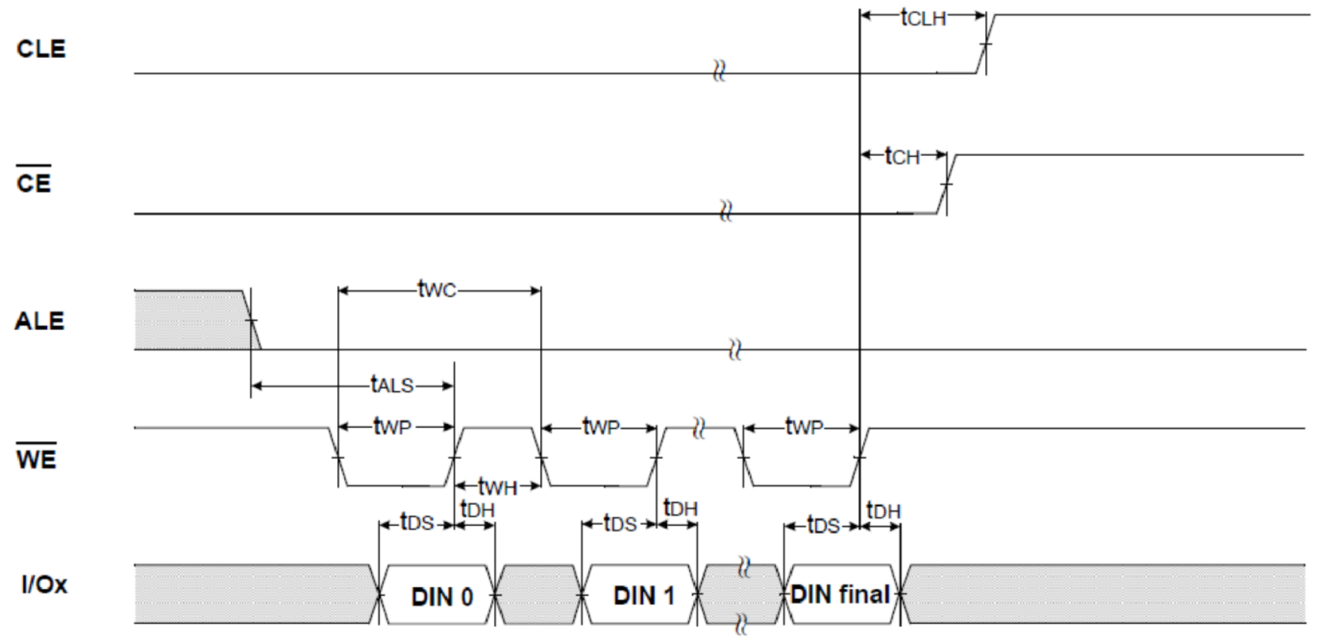
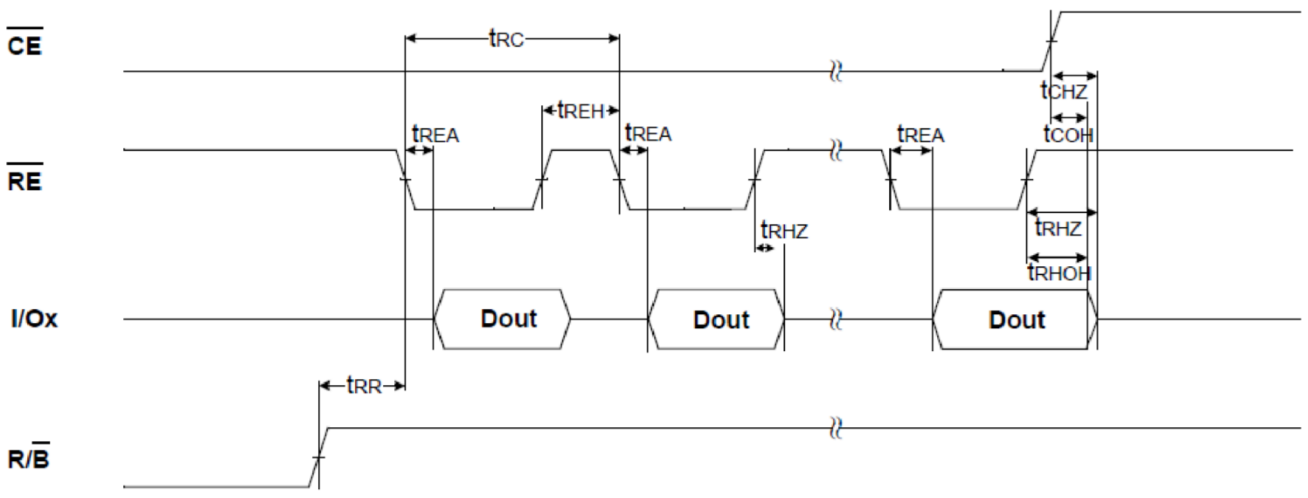
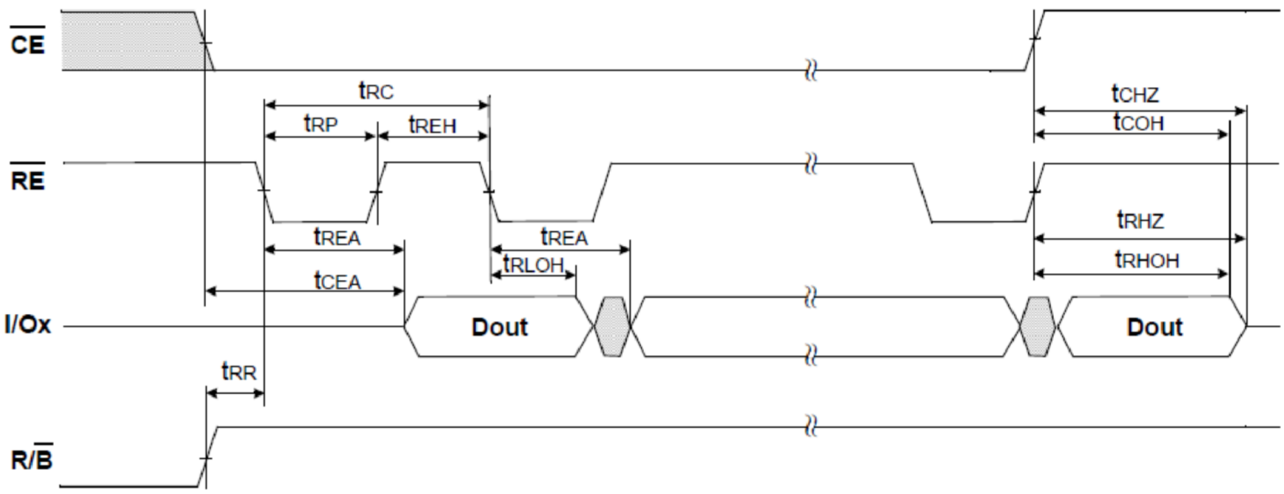


Figure 6: Input Data Latch Cycle



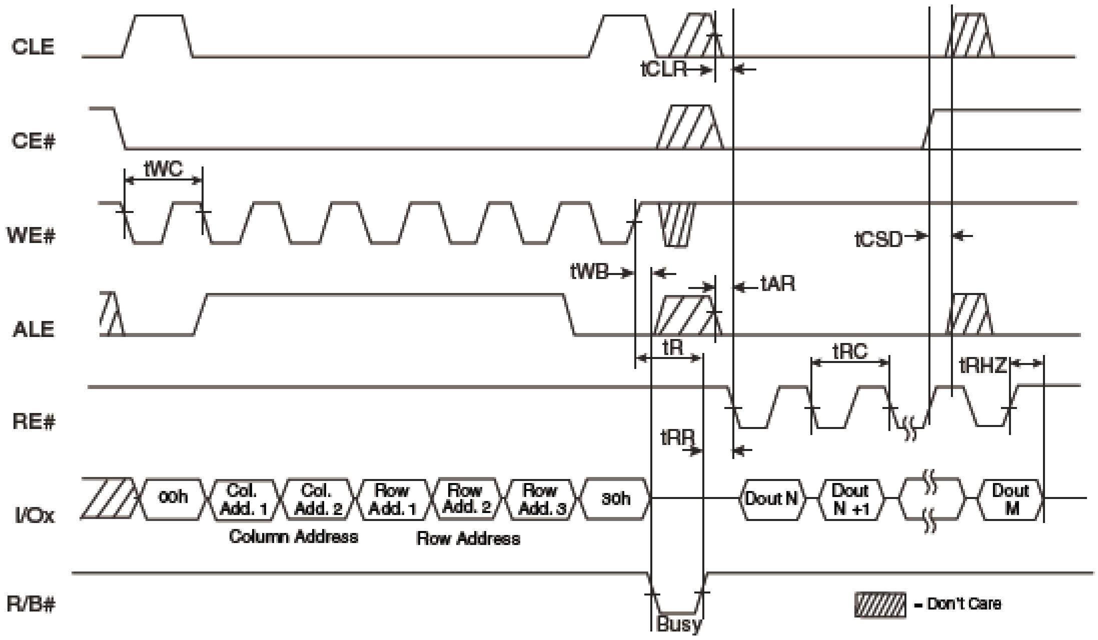
NOTES : Transition is measured at ±200mV from steady state voltage with load.
This parameter is sampled and not 100% tested.
tRLOH is valid when frequency is higher than 33MHz.
tRHOH starts to be valid when frequency is lower than 33MHz.

Figure 7: Sequential Out Cycle after Read (CLE=L, WE#=H, ALE=L, WP#=H)



NOTES : Transition is measured at ±200mV from steady state voltage with load.
This parameter is sampled and not 100% tested.
tRLOH is valid when frequency is higher than 33MHz.
tRHOH starts to be valid when frequency is lower than 33MHz.

Figure 8: **Sequential Out Cycle after Read (EDO Type, CLE=L, WE#=H, ALE=L)**



Note:
1. *If Status Register polling is used to determine completion of the read operation, the Read Command (00h) must be issued before data can be read from the page buffer.*

Figure 9: **Read Operation (Read One Page)**

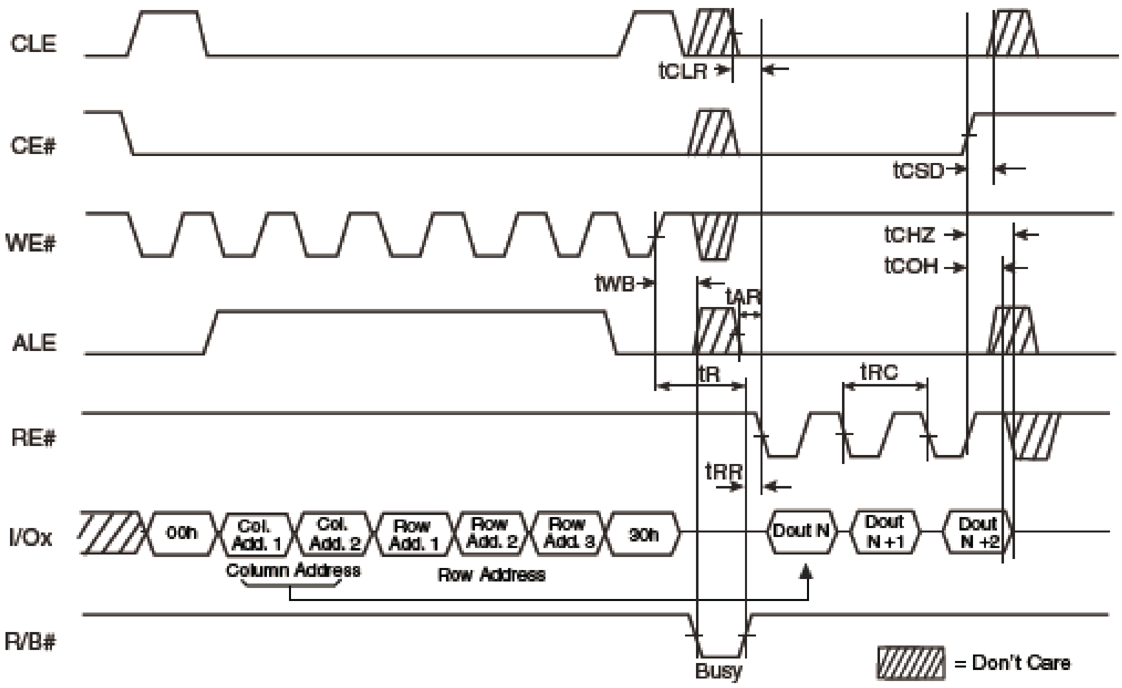


Figure 10: **Read Operation Intercepted By CE#**

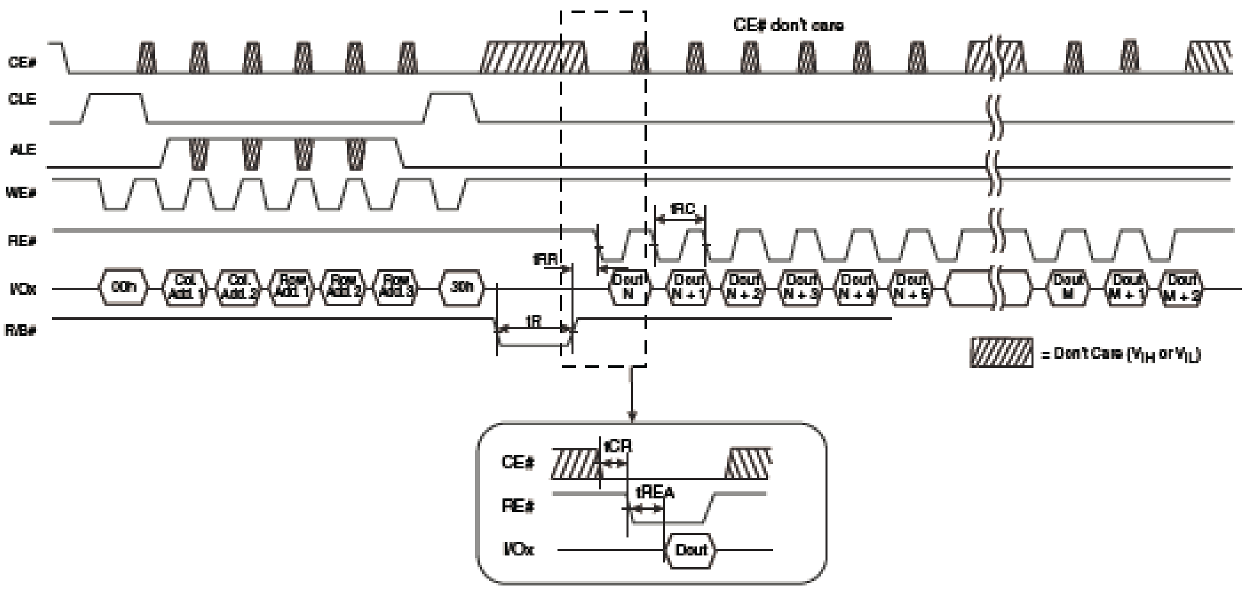


Figure 11: **Page read operation timing with CE# don't care**

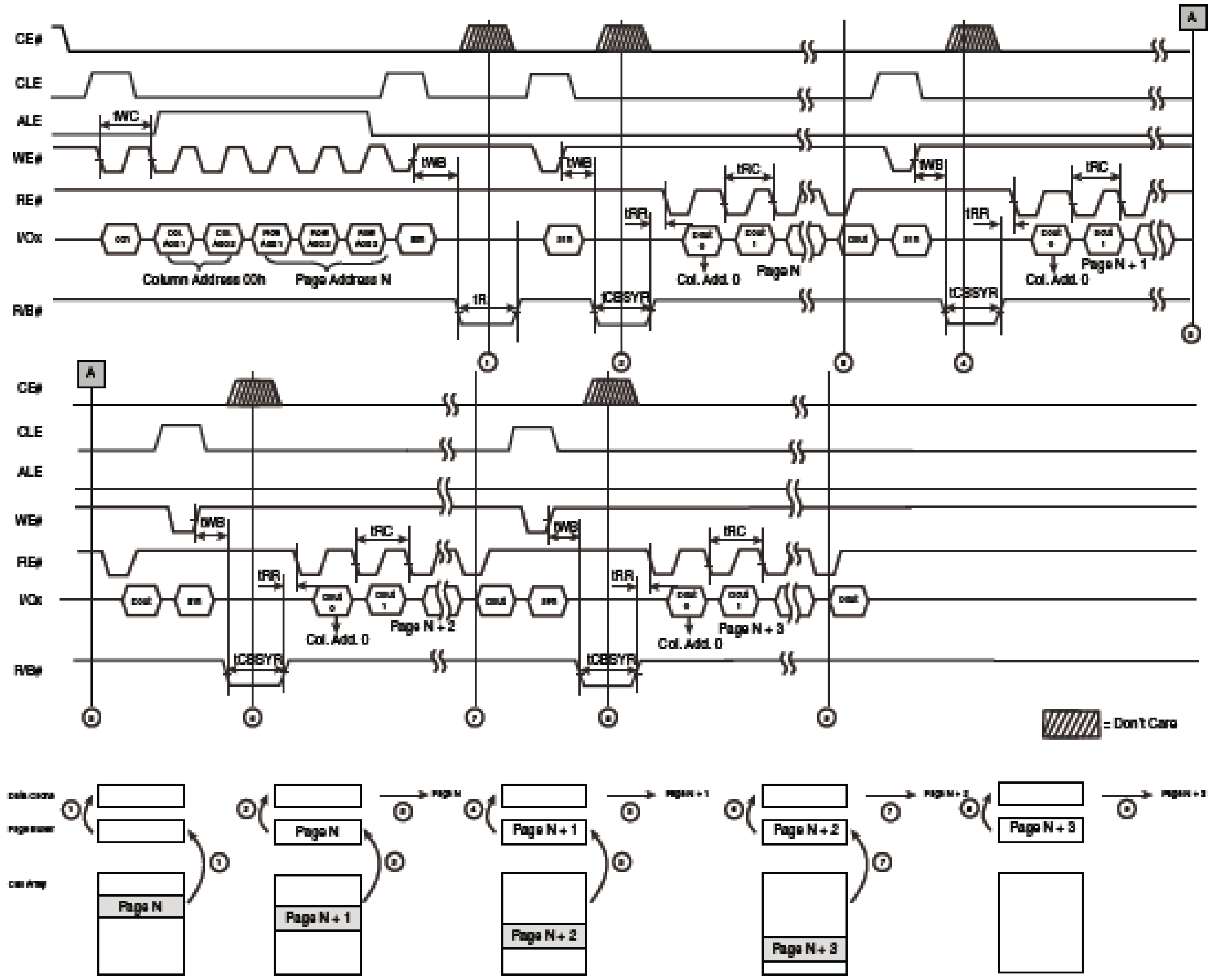


Figure 12: Read Cache Operation Timing

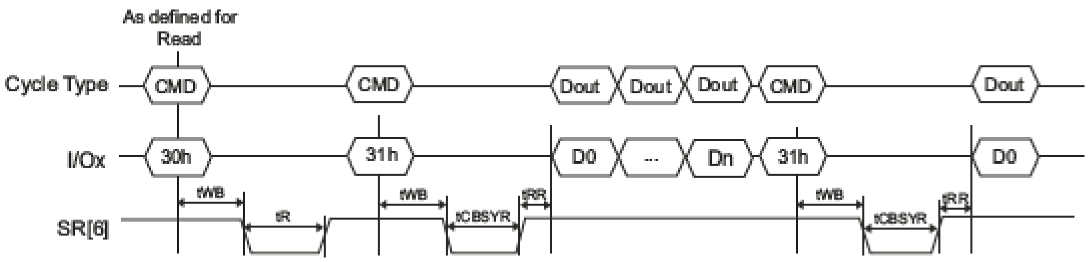


Figure 13: "Sequential" Read Cache Timing, Start (and Continuation) of Cache Operation

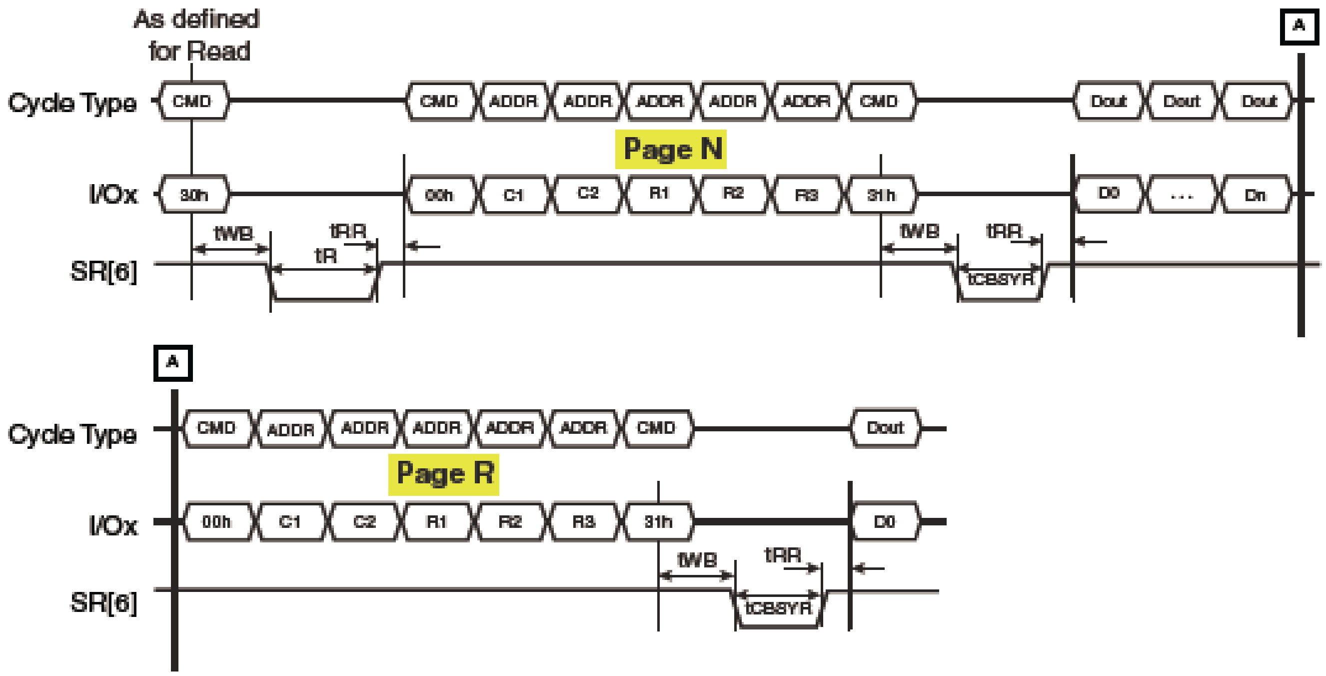


Figure 14: "Random" Read Cache Timing, Start (and Continuation) of Cache Operation

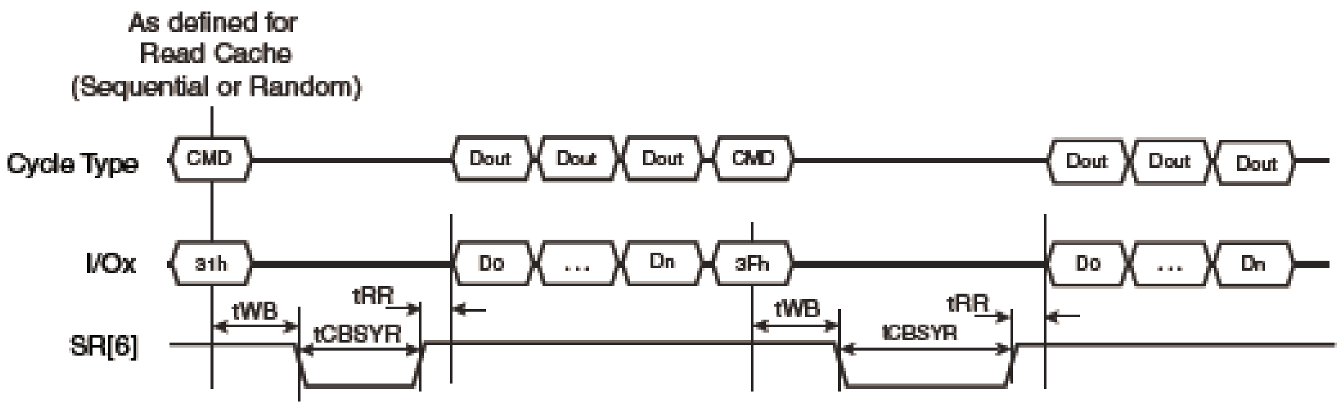


Figure 15: Read Cache Timing, End Of Cache Operation

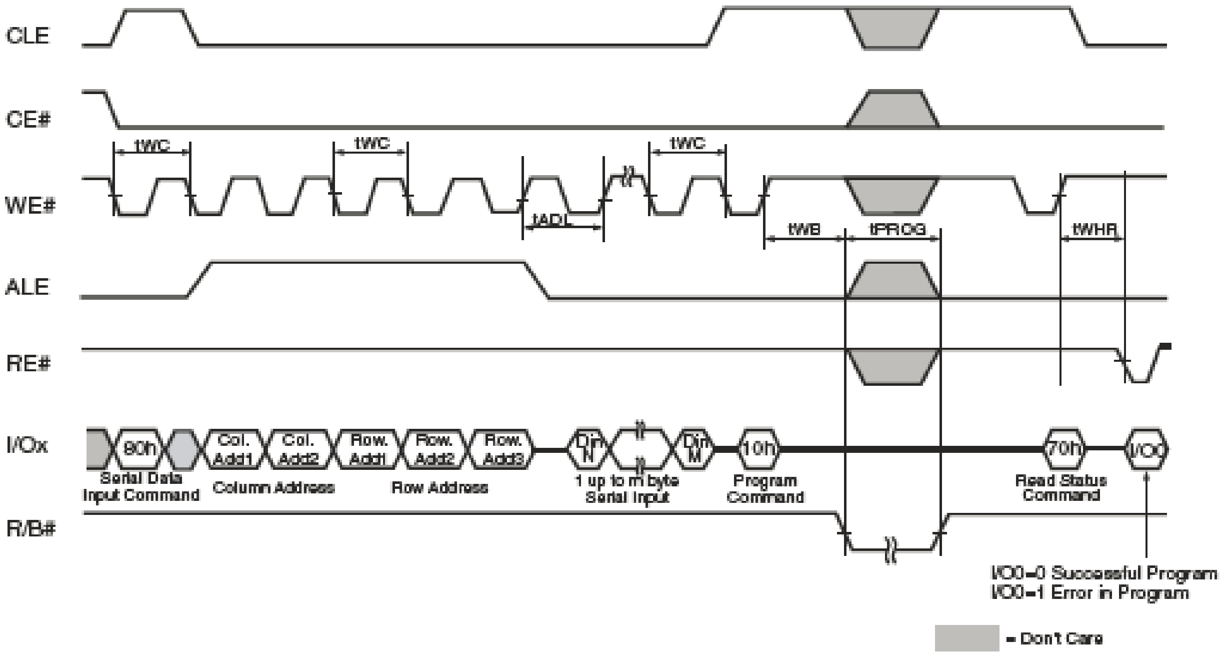


Figure 16: **Page Program Operation**

Note:

1. tADL is the time from the WE# rising edge of final address cycle to the WE# rising edge of first data cycle.

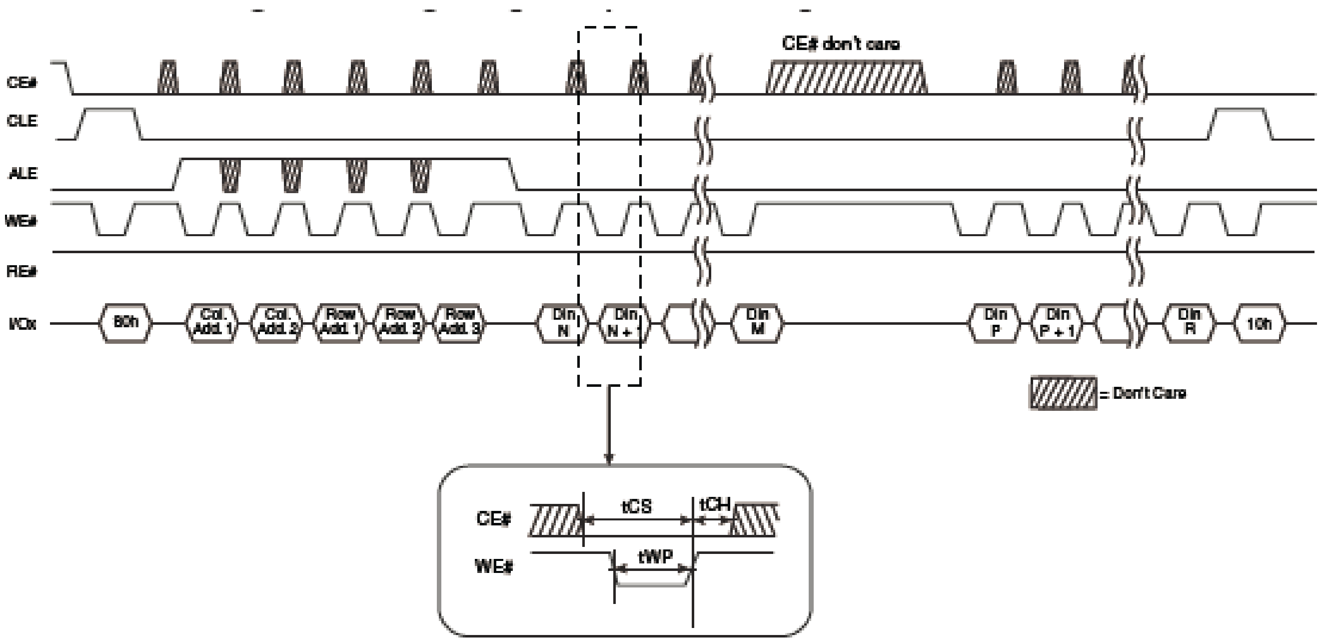
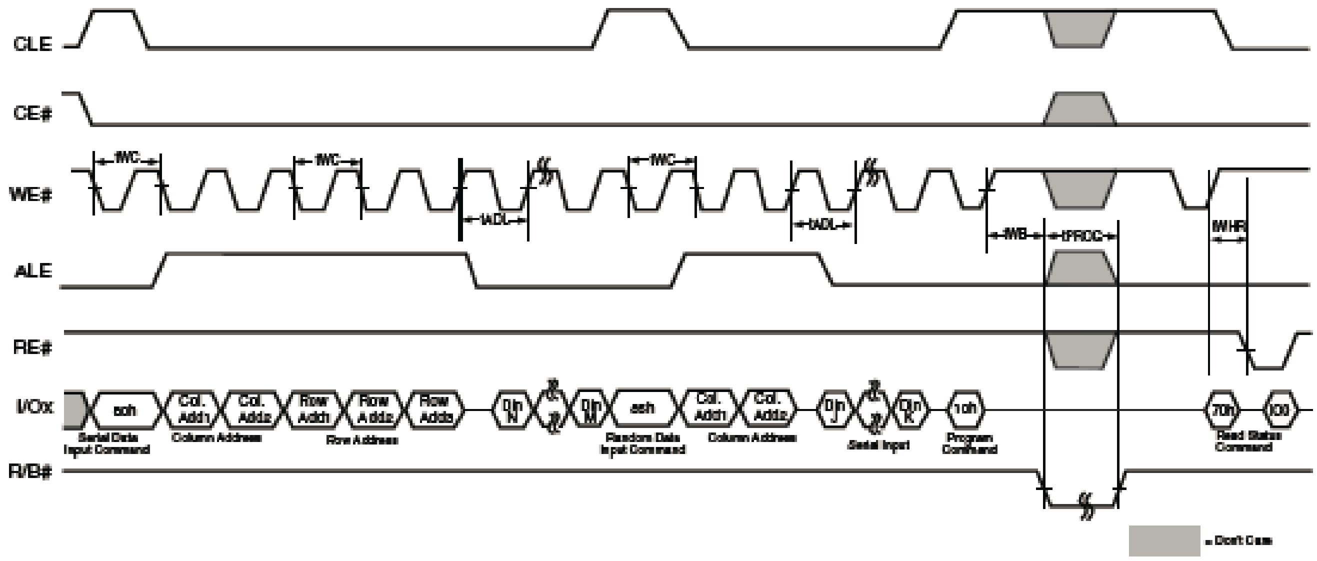


Figure 17: **Page Program Operation Timing with CE# Don′t Care**



Note:
1. tADL is the time from the WE# rising edge of final address cycle to the WE# rising edge of first data cycle.

Figure 18: **Random Data Input**

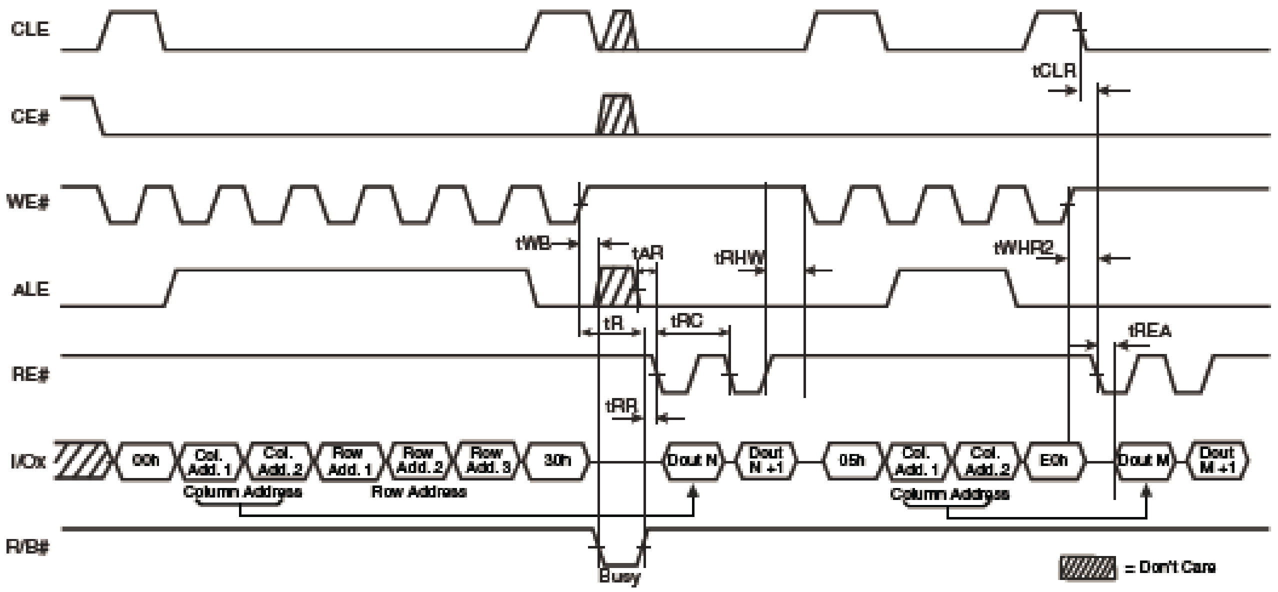


Figure 19: **Random Data Output**

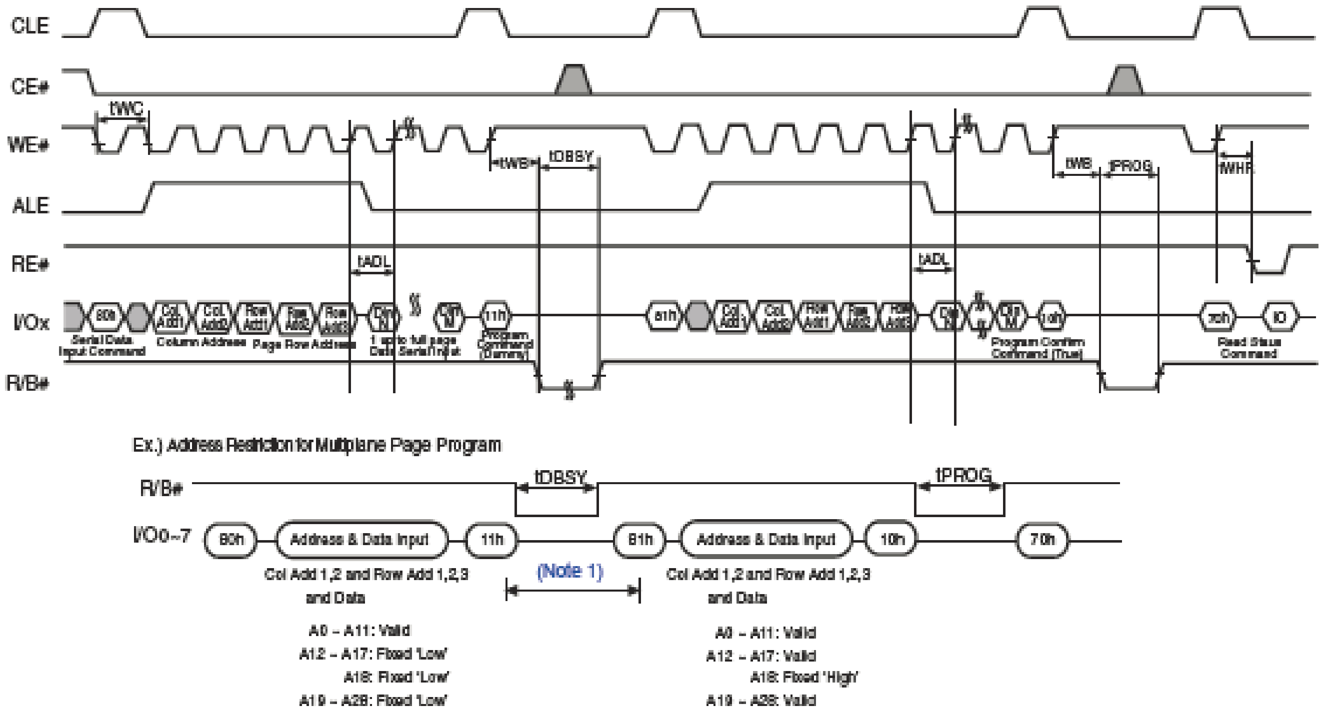


Figure 20: Multiplane Page Program

Notes:
1. Any command between 11h and 81h is prohibited except 70h, 78h, and FFh.
2. A18 is the plane address bit for x8 devices.

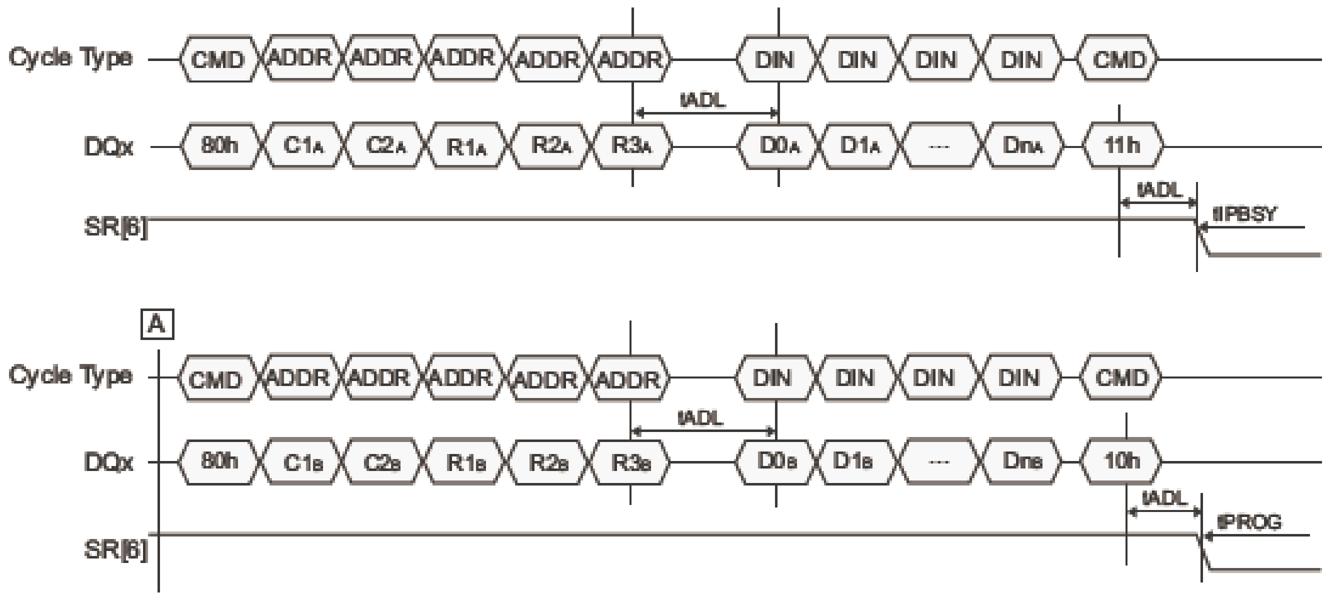


Figure 21: Multiplane Page Program(ONFI 1.0 Protocol)

Notes:
1. C1A-C2A Column address for page A. C1A is the least significant byte.
2. R1A-R3A Row address for page A. R1A is the least significant byte.
3. D0A-DnA Data to program for page A.
4. C1B-C2B Column address for page B. C1B is the least significant byte.
5. R1B-R3B Row address for page B. R1B is the least significant byte.
6. D0B-DnB Data to program for page B.
7. The block address bits must be the same except for the bit(s) that select the plane.

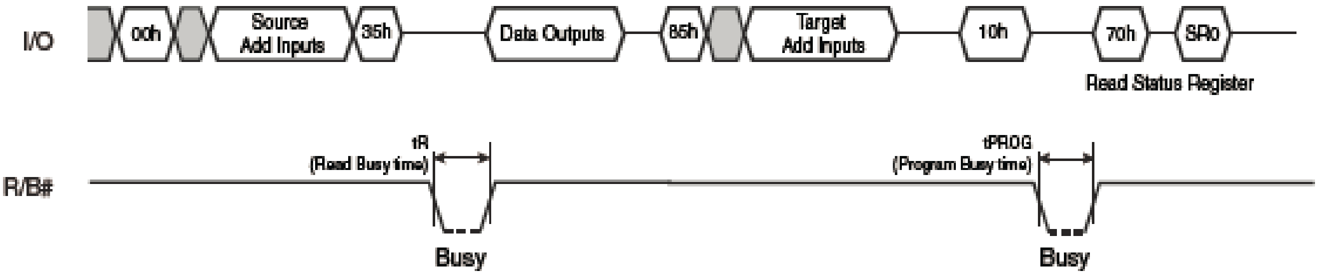


Figure 22: **Copy Back read with optional data readout**

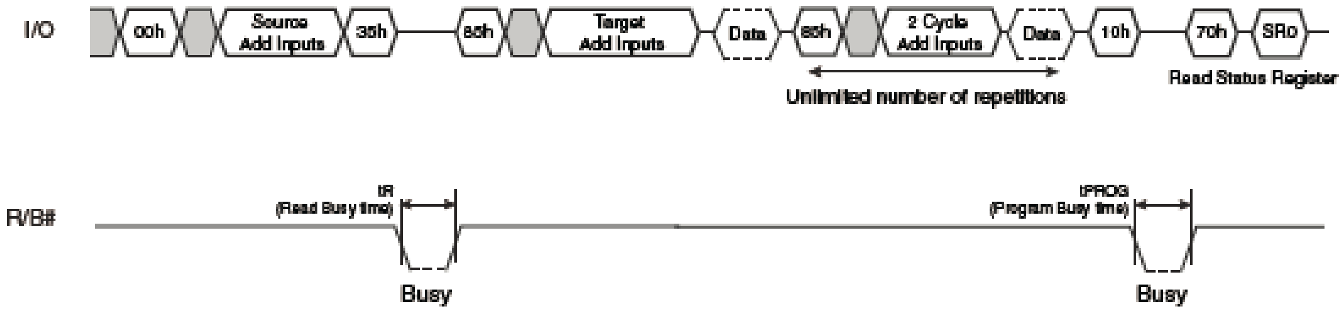


Figure 23: **Copy Back Program with Random Data Input**

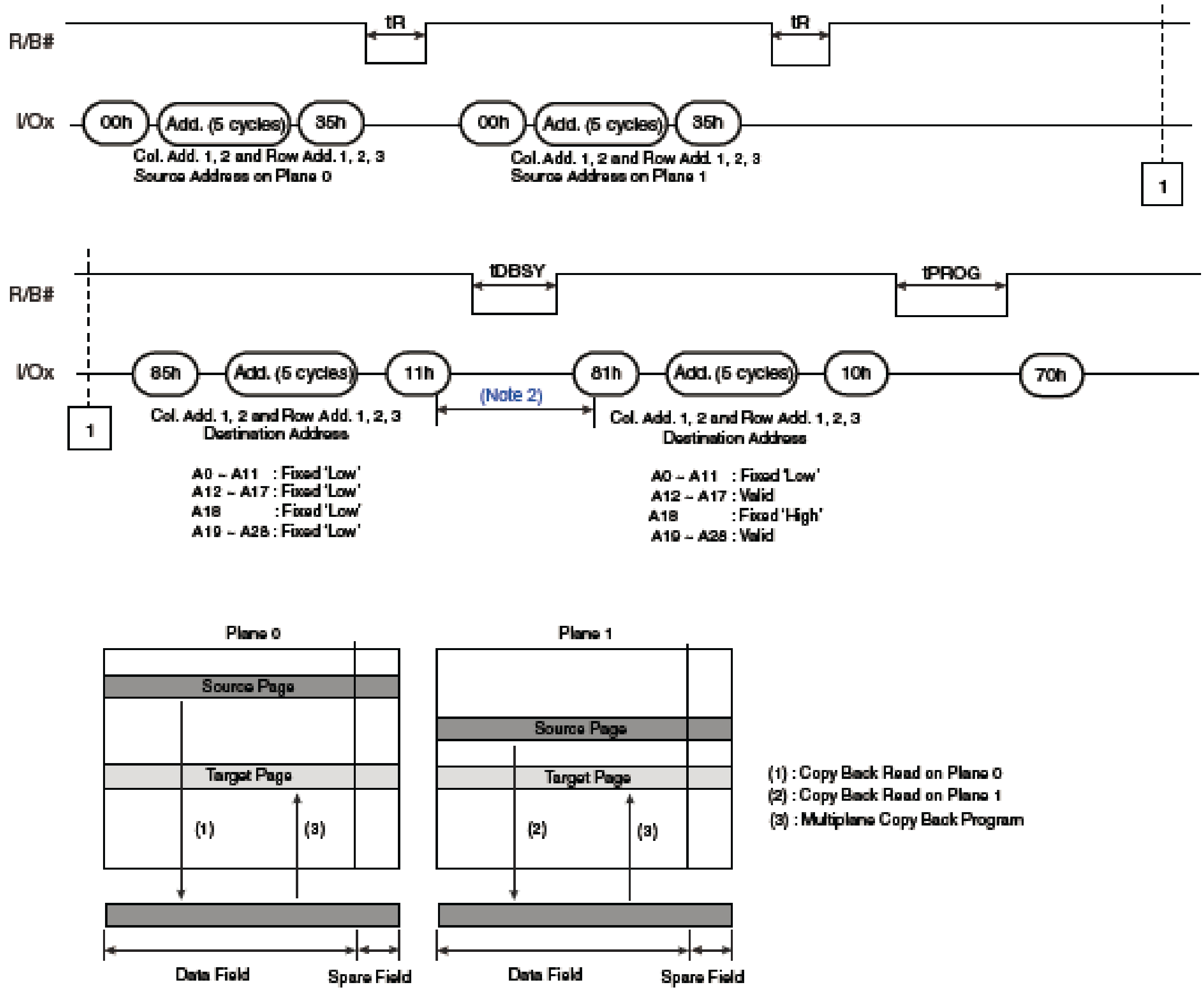


Figure 24: **Multiplane Copy Back Program**

Notes:
1. Copy Back Program operation is allowed only within the same memory plane.
2. Any command between 11h and 81h is prohibited except 70h, 78h, and FFh.
3. A18 is the plane address bit for x8 devices.

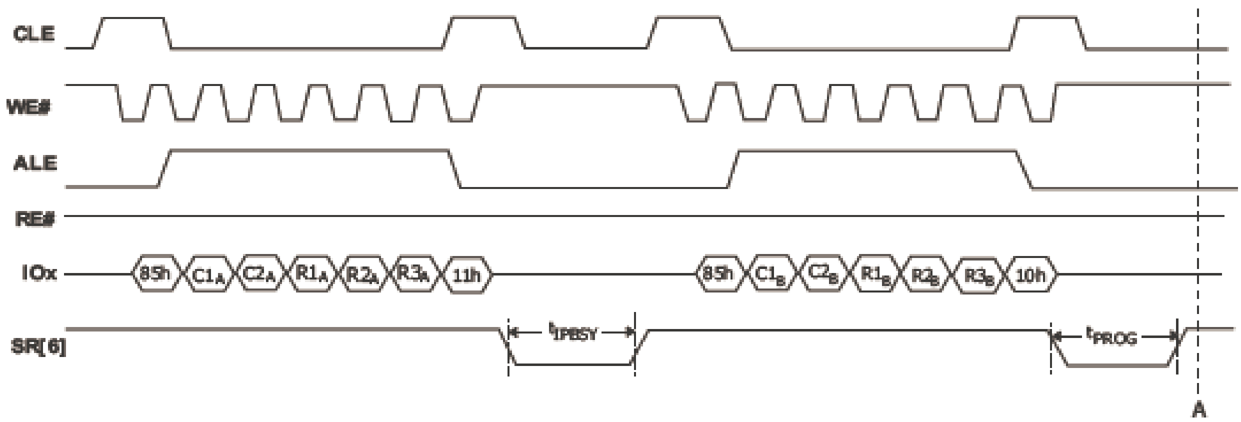


Figure 25: **Multiplane Copy Back Program (ONFI 1.0 Protocol)**

Notes:

1. C1A-C2A Column address for page A. C1A is the least significant byte.
2. R1A-R3A Row address for page A. R1A is the least significant byte.
3. C1B-C2B Column address for page B. C1B is the least significant byte.
4. R1B-R3B Row address for page B. R1B is the least significant byte.
5. The block address bits must be the same except for the bit(s) that select the plane.

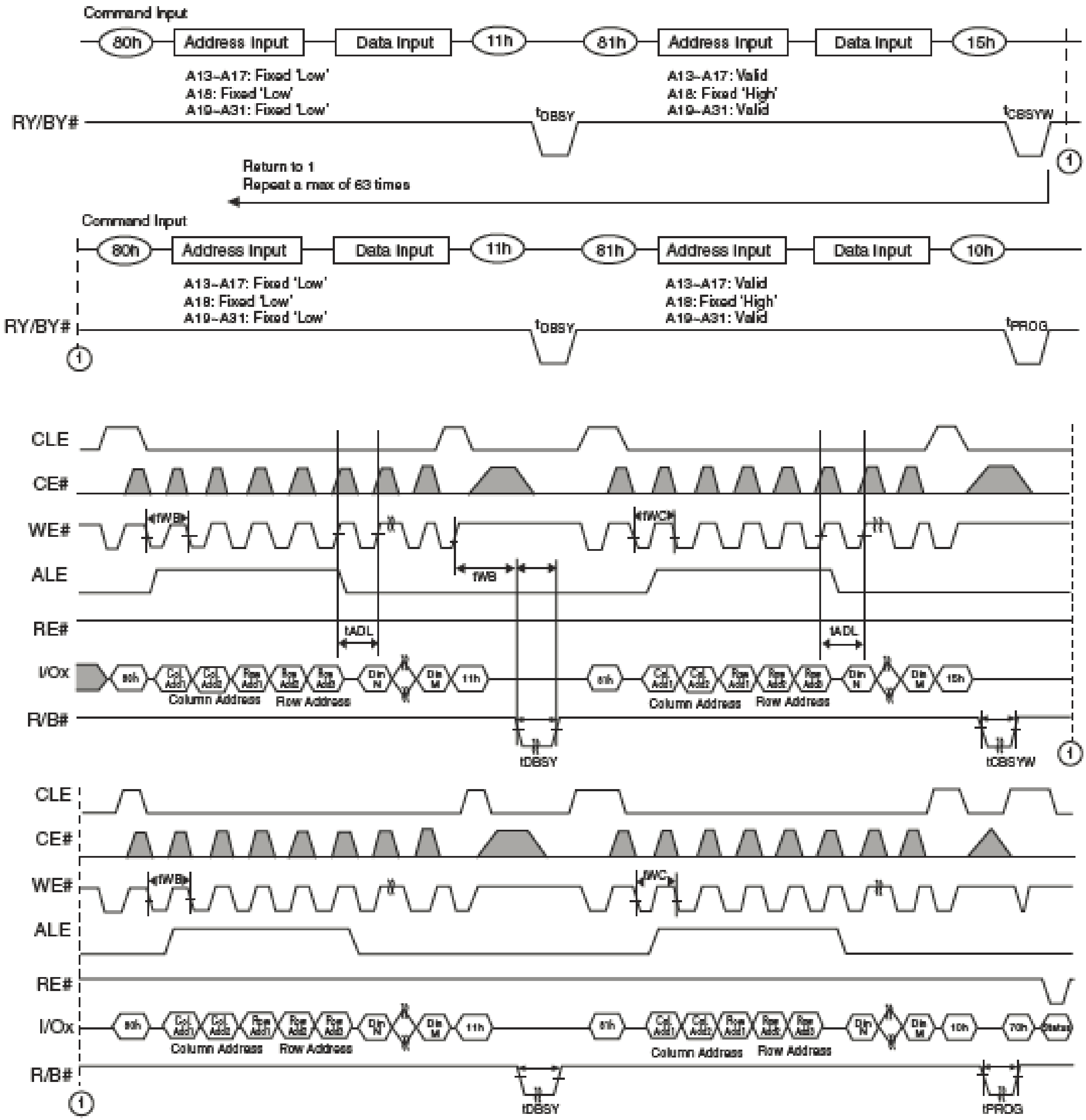


Figure 26: Multiplane Cache Program

Notes:
1. Read Status Register (70h) is used in the figure. Read Status Enhanced (78h) can be also used.
2. A18 is the plane address bit for x8 devices.

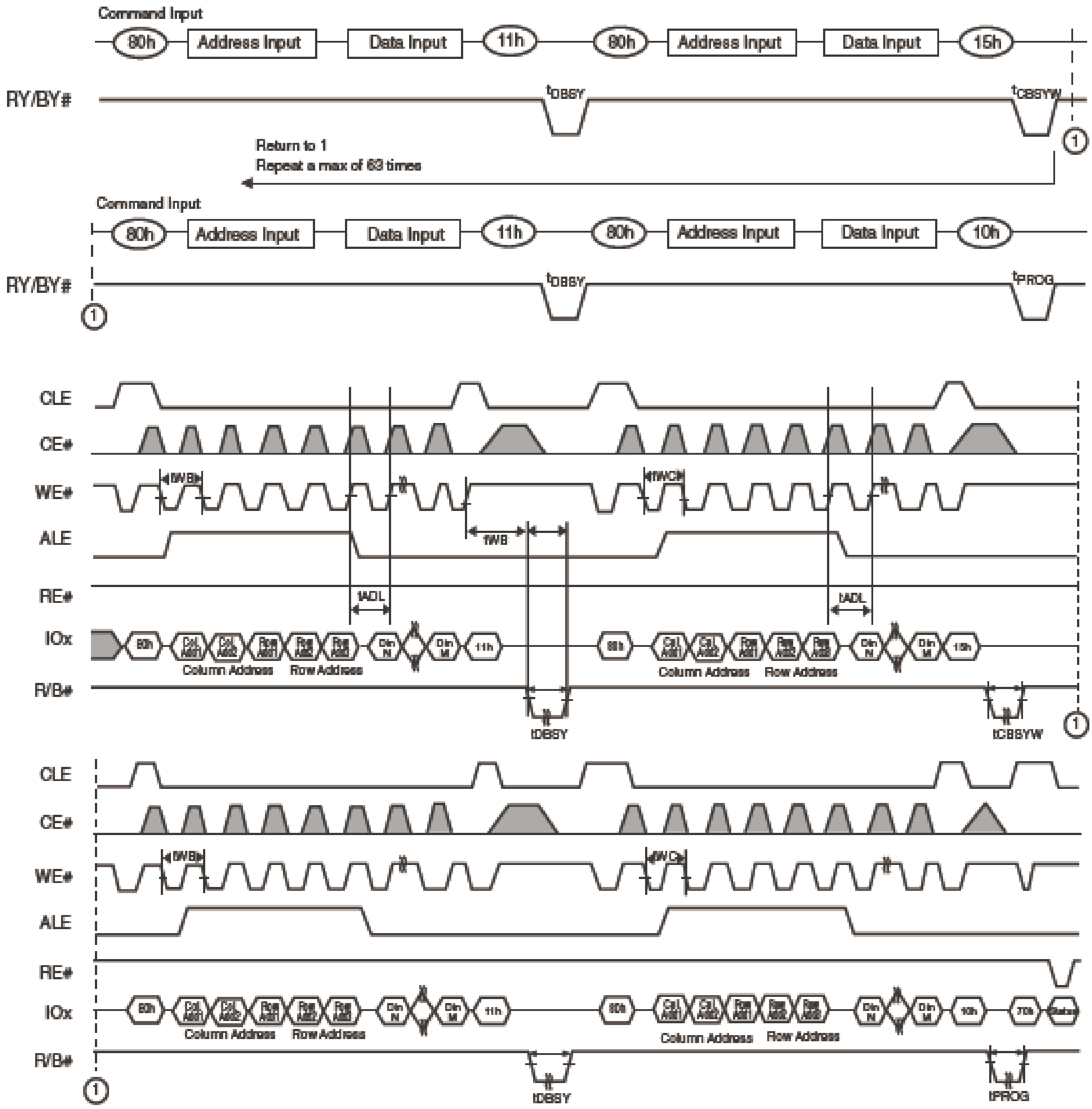


Figure 27: Multiplane Cache Program(ONFI 1.0 Protocol)

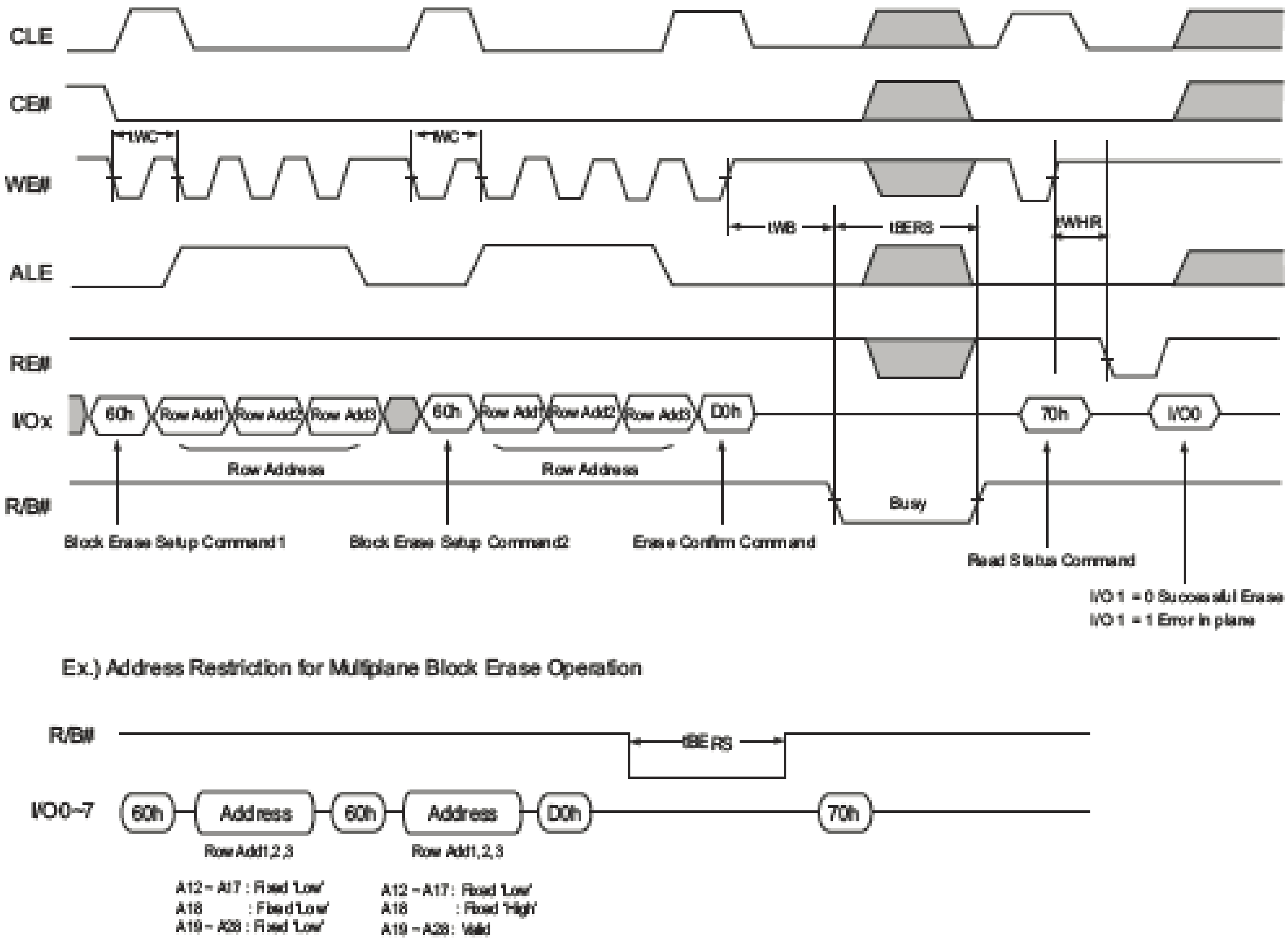


Figure 28: **Multiplane Block Erase Operation**

Note:

1. A18 is the plane address bit for x8 devices.

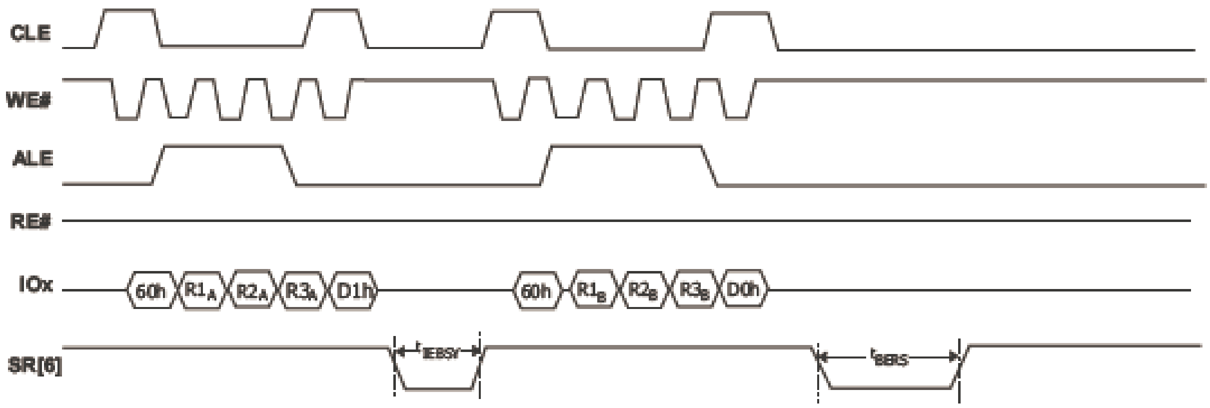


Figure 29: **Multiplane Block Erase (ONFI 1.0 Protocol)**

Notes:

1. R1A-R3A Row address for block on plane 0. R1A is the least significant byte.

2. R1B-R3B Row address for block on plane 1. R1B is the least significant byte.

3. The block address bits must be the same except for the bit(s) that select the plane.

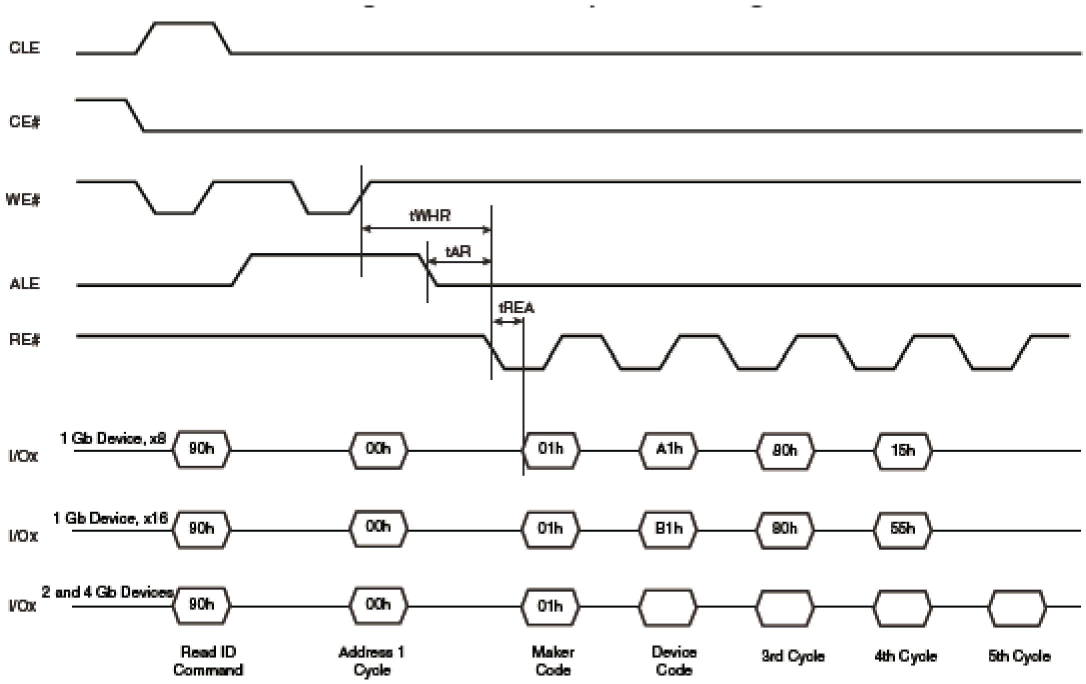


Figure 30: **READ ID Operation**

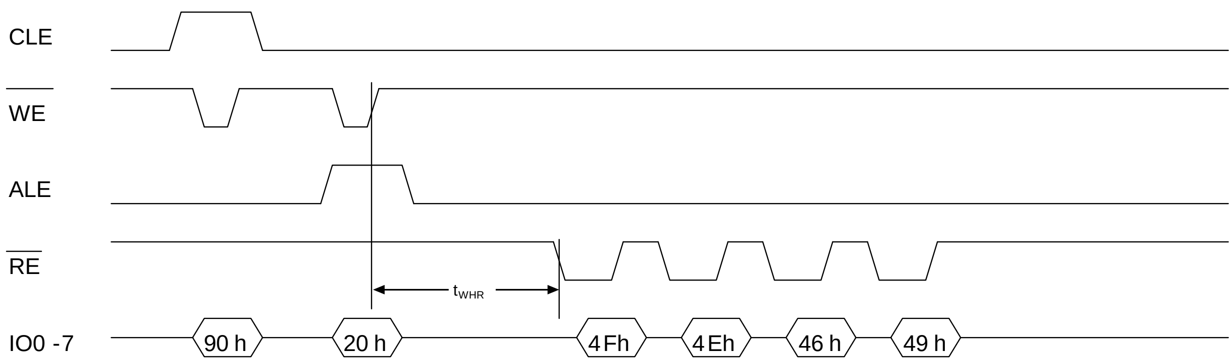


Figure 31: **ONFI signature timing diagram**

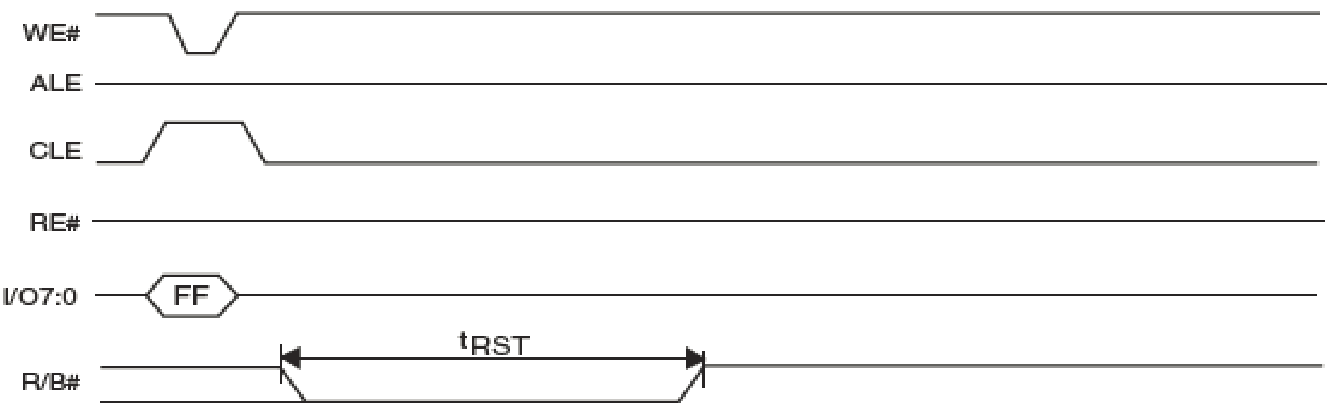


Figure 32: **Reset operation timing**

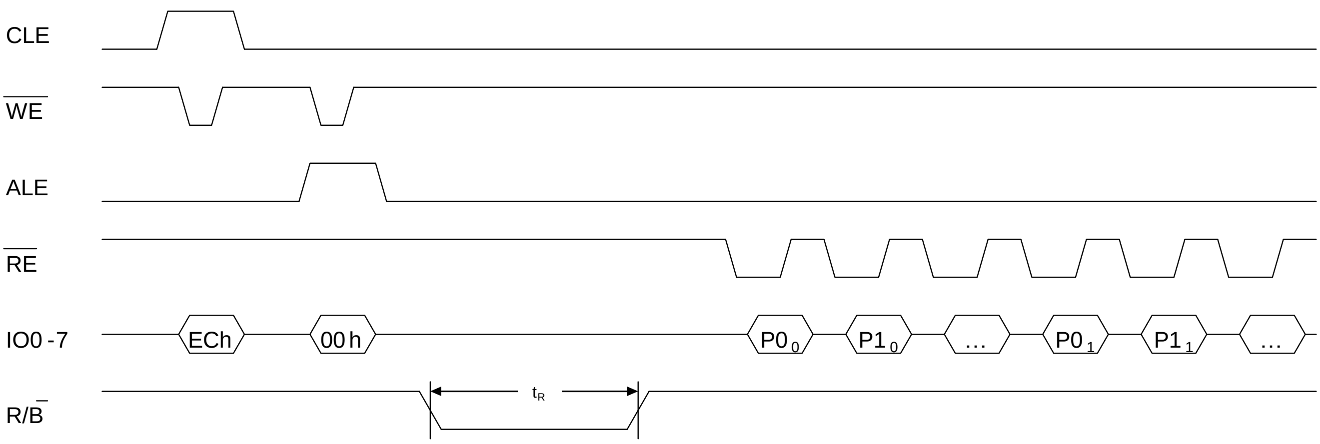


Figure 33: **Read Parameter Page timings**

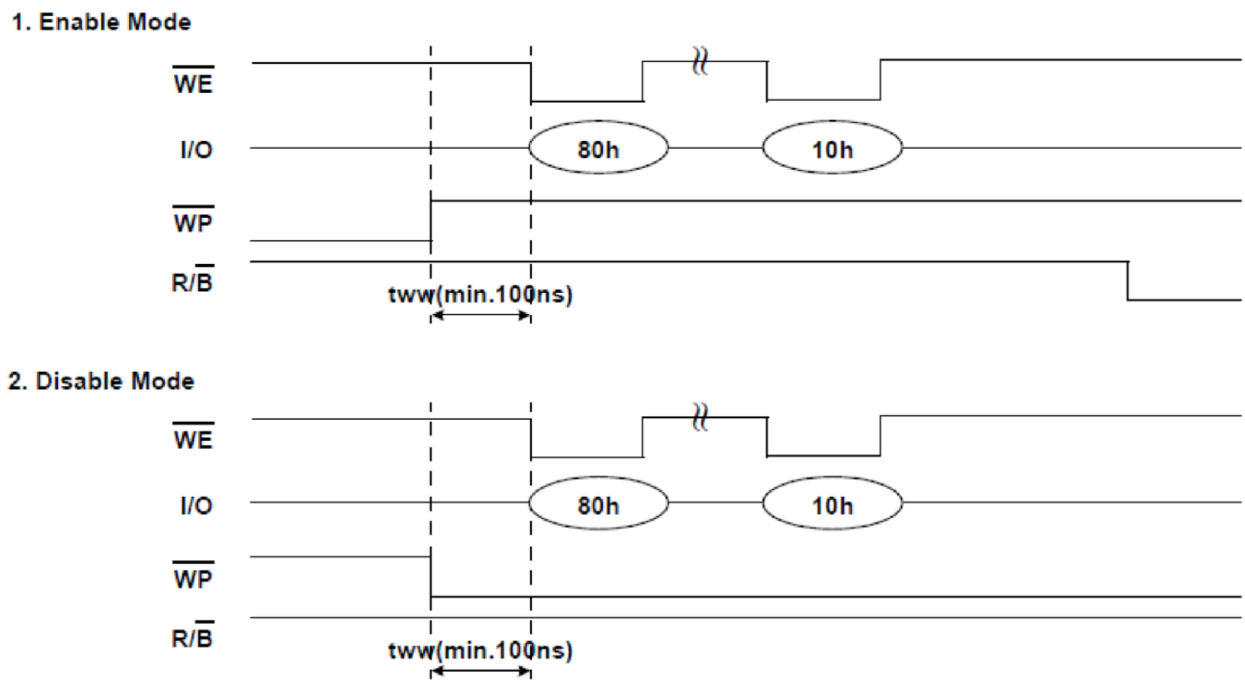


Figure 34: **tWW in Program Operation**

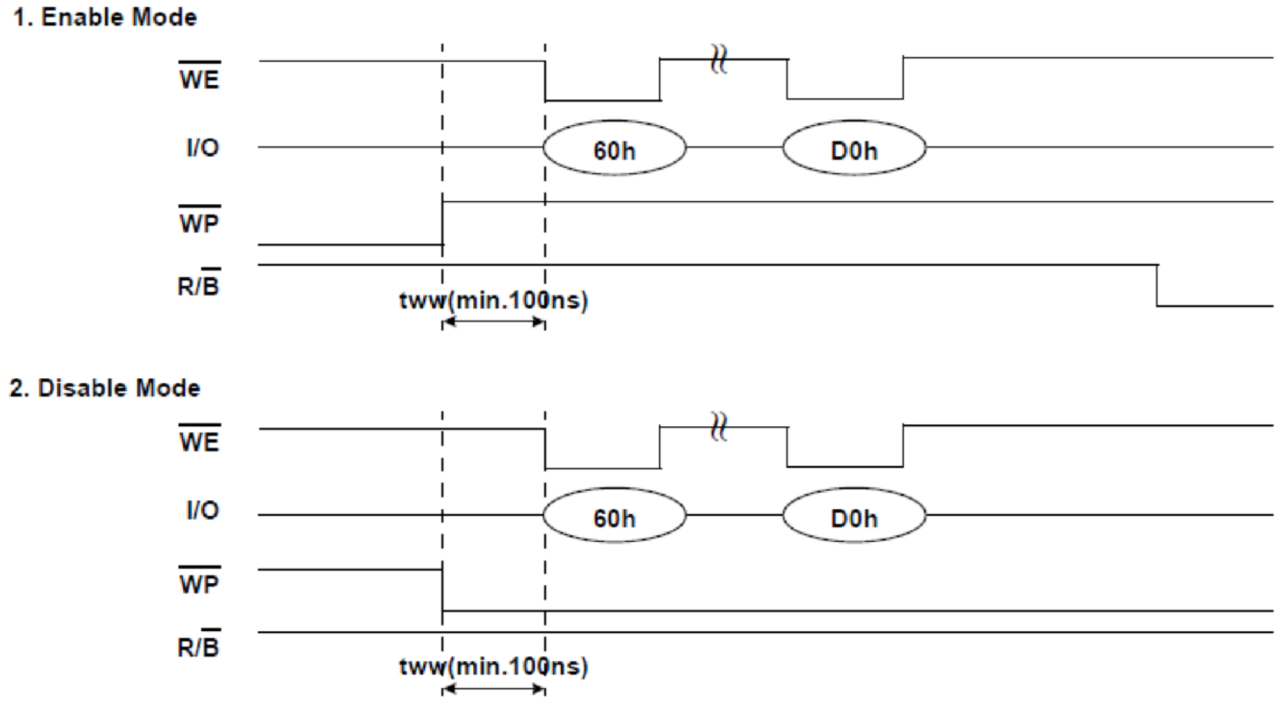


Figure 35: tWW in Erase Operation

Note : V_{TH} = 1.2 Volts.

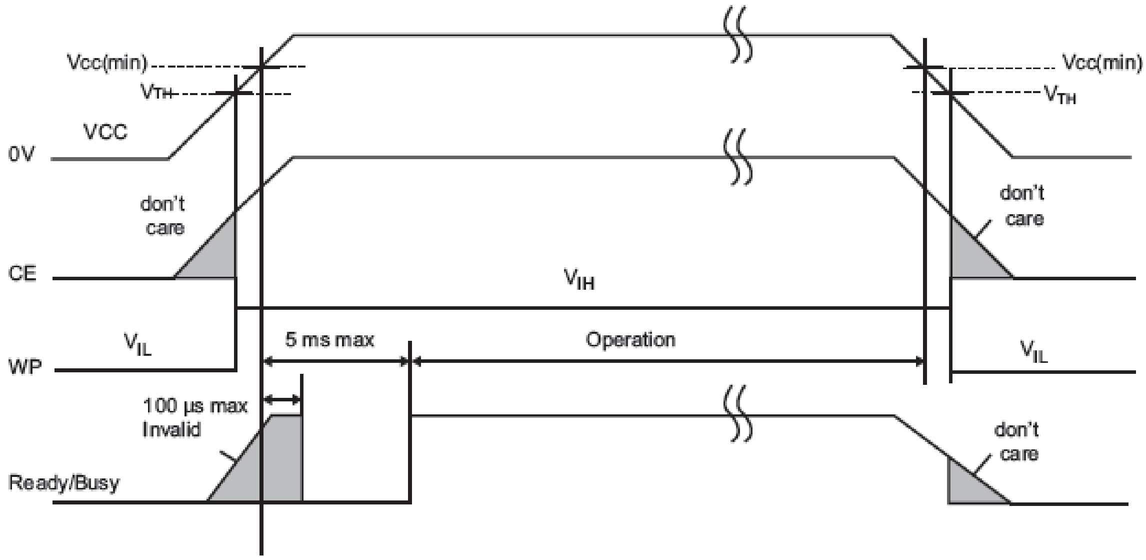


Figure 36: Power on and Data Protection Timing

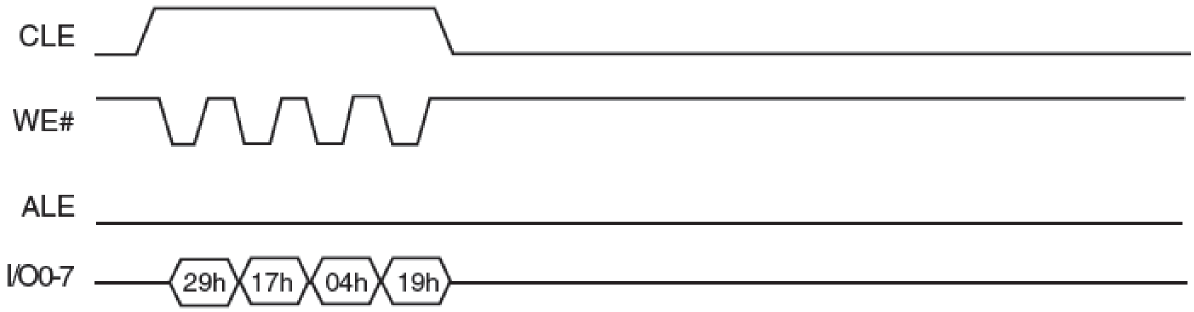


Figure 37: **OTP Entry Timing**

6 BAD BLOCK MANAGEMENT

Devices with Bad Blocks have the same quality level and the same AC and DC characteristics as devices where all the blocks are valid. A Bad Block does not affect the performance of valid blocks because it is isolated from the bit line and common source line by a select transistor. The devices are supplied with all the locations inside valid blocks erased (FFh). The Bad Block Information is written prior to shipping. Any block where the 1st byte in the spare area of the 1st or 2nd or last page does not contain FFh is a Bad Block. That is, if the first page has an FF value and should have been a non-FF value, then the non-FF value in the second page or the last page will indicate a bad block.The Bad Block Information must be read before any erase is attempted, as the Bad Block Information may be erased. For the system to be able to recognize the Bad Blocks based on the original information, it is recommended to create a Bad Block table following the flowchart shown in Figure Bad Block Management Flowchart. The host is responsible to detect and track bad blocks, both factory bad blocks and blocks that may go bad during operation. Once a block is found to be bad, data should not be written to that block.The 1st block, which is placed on 00h block address is guaranteed to be a valid block.

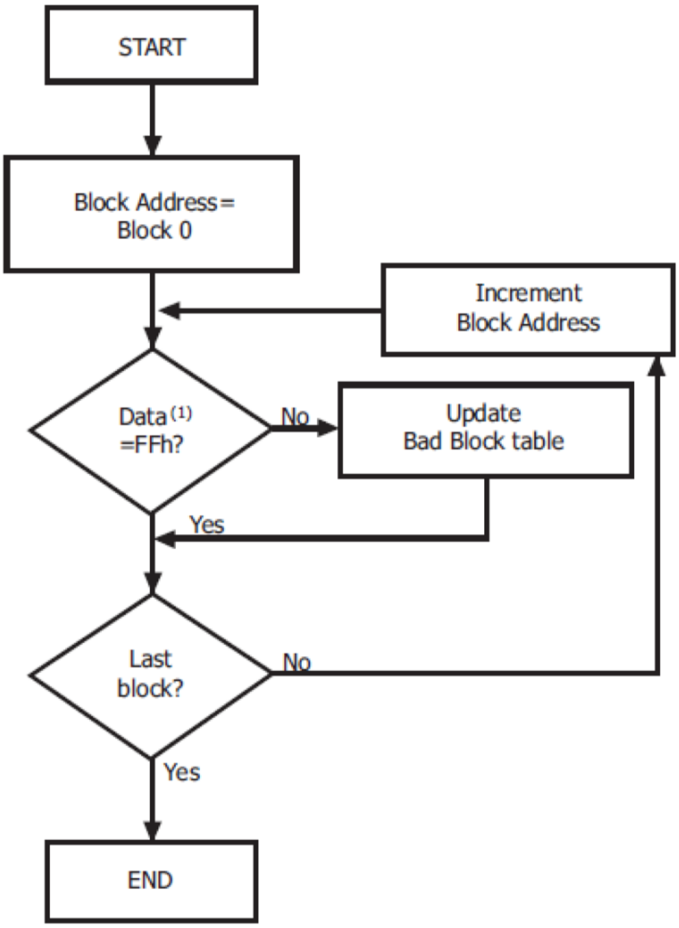


Figure 38: **Bad Block Management Flowchart**

MOBILE DDR2 SDRAM MEMORY OPERATION

7 DESCRIPTION

The SCP30N2G1GSL is a 8 bank low power DDR2 DRAM organized as 8 banks x 4M x 32.

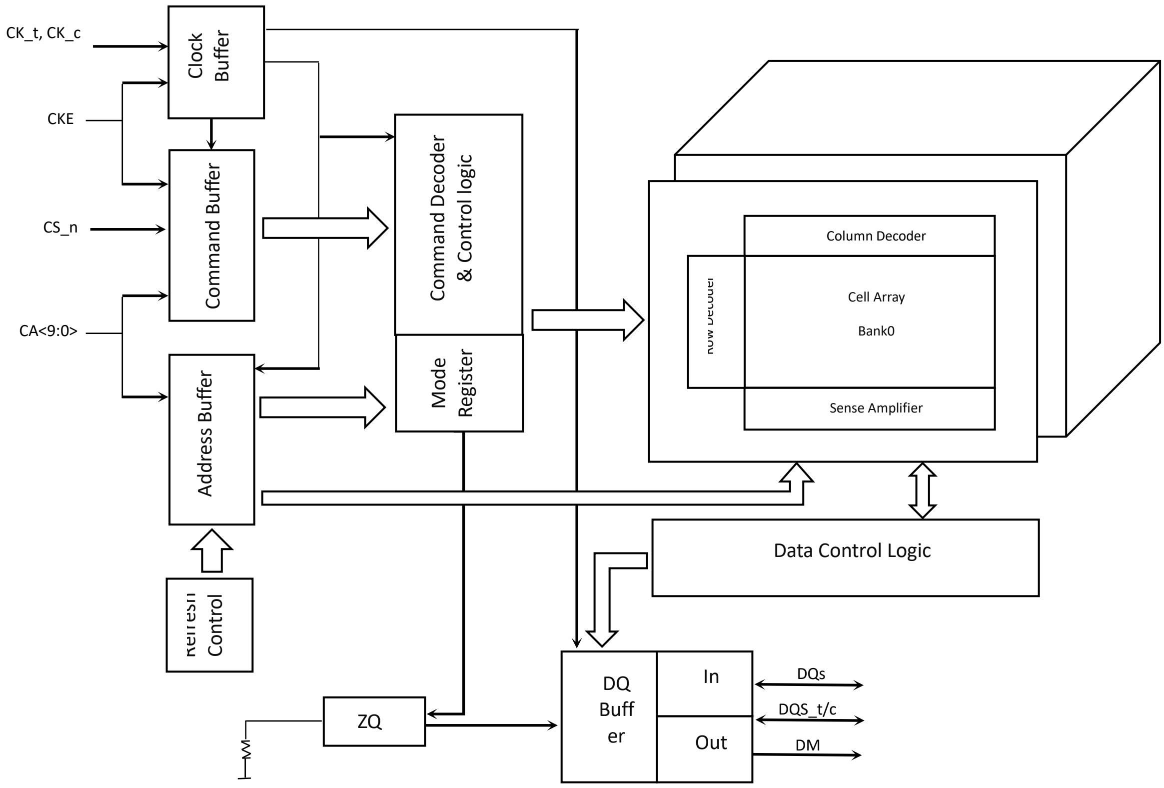
It achieves high speed data transfer rates by employing a chip architecture that prefetches multiple bits and then synchronizes the output data to a system clock.

All of the control, address, circuits are synchronized with both edge of an externally supplied clock. I/O transactions are possible on both edges of DQS.

Operating the four memory banks in an interleaved fashion allows random access operation to occur at a higher rate is possible with standard DRAMs. A sequential and gapless data rate is possible depending on burst length, Read/Write latency and speed grade of the device.

Additionally, the device supports low power saving features like PASR, Auto-TCSR, deep power down, as well as options for different drive strength. It’s ideally suitable for low power application.

7.1 Block Diagram



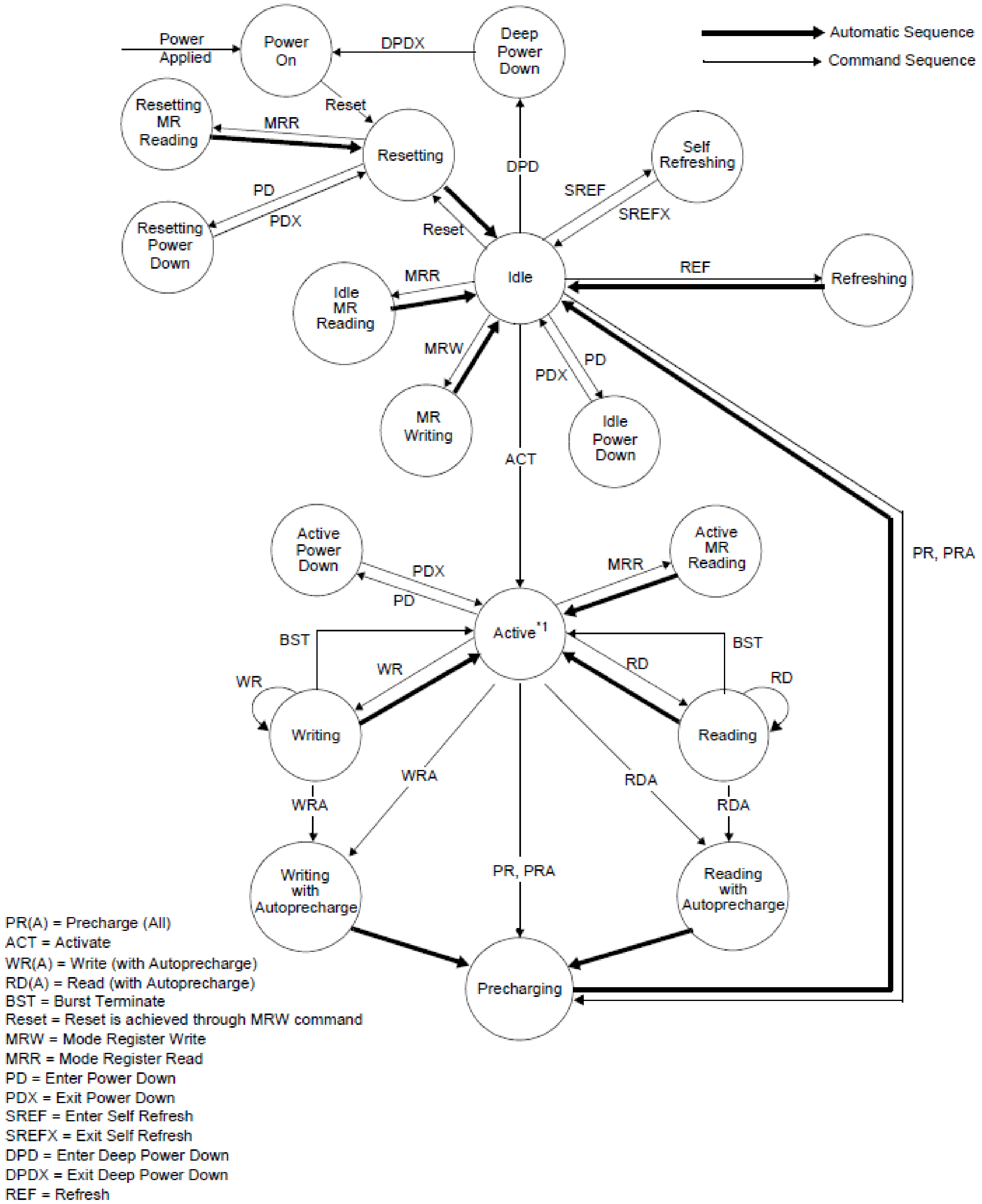
8 FUNCTION DESCRIPTION

LPDDR2-S4 devices use a double data rate architecture on the DQ pads to achieve high speed operation. The double data rate architecture is essentially a 4n prefetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pads. A single read or write access for the LPDDR2-S4 effectively consists of a single 4n-bit-wide, one-clock-cycle data transfer at the internal SDRAM core and four corresponding n-bit-wide, one-half-clock-cycle data transfers at the I/O pads.

Read and write accesses are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence.

Prior to normal operation, the LPDDR2 device must be initialized. The following section provides detailed information covering device initialization, register definition, command description and device operation.

8.1 Simplified LPDDR2 Bus Interface State Diagram



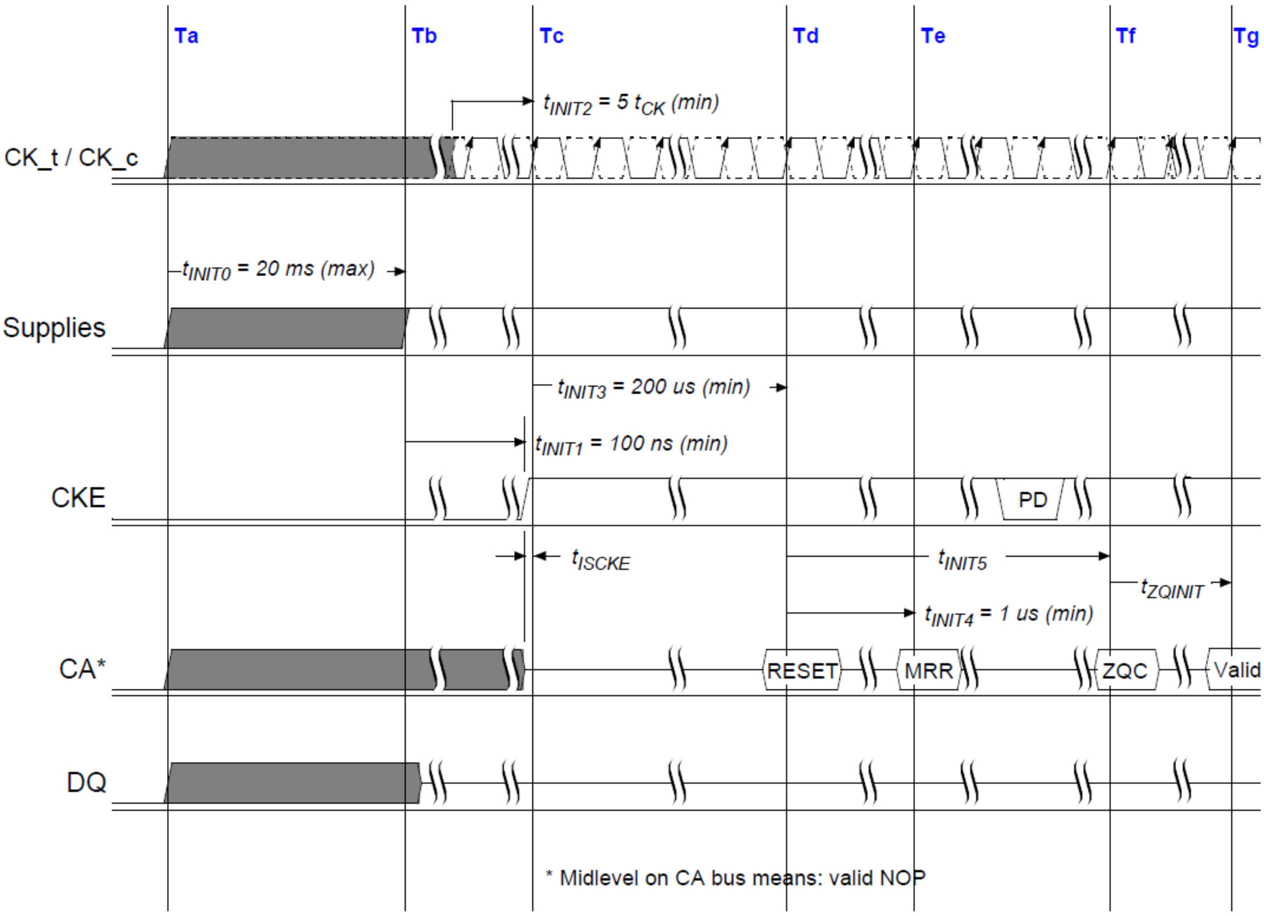
Note: For LPDDR2-SDRAM in the Idle state, all banks are precharged.

8.2 Power-up, Initialization, and Power-Off

8.2.1 Timing Parameters for initialization

Symbol	Value		Unit	Comment
	min	max		
tINIT0		20	mS	Maximum Power Ramp Time
tINIT1	100		nS	Minimum CKE low time after completion of power ramp
tINIT2	5		tCK	Minimum stable clock before first CKE high
tINIT3	200		uS	Minimum Idle time after first CKE assertion
tINIT4	1		uS	Minimum Idle time after Reset command
tINIT5		10	uS	Maximum duration of Device Auto-Initialization
tZQINIT	1		uS	ZQ Initial Calibration for LPDDR2-S4
tCKb	18	100	uS	Clock cycle time during boot

8.2.2 Power Ramp and Initialization Sequence



8.2.3 Power Ramp and Device Initialization

The following sequence shall be used to power up an LPDDR2 device. Unless specified otherwise, these steps are mandatory.

8.2.3.1 Power Ramp

While applying power (after Ta), CKE shall be held at a logic low level (≤ 0.2 x VDD2), all other inputs shall be between VILmin and VIHmax. The LPDDR2 device will only guarantee that outputs are in a high impedance state while CKE is held low.

On or before the completion of the power ramp (Tb) CKE must be held low.

DQ, DM, DQS_t and DQS_c voltage levels must be between VSSQ and VDDQ during voltage ramp to avoid latchup. CK_t, CK_c, CS_n, and CA input levels must be between VSS and VDD2 during voltage ramp to avoid latch-up.

The following conditions apply:

Ta is the point where any power supply first reaches 300mV.

After Ta is reached, VDD1 must be greater than VDD2 - 200mV.

After Ta is reached, VDD1 and VDD2 must be greater than VDD2 - 200mV.

After Ta is reached, VDD1 and VDD2 must be greater than VDDQ - 200mV.

After Ta is reached, VREF must always be less than all other supply voltages.

The voltage difference between any of VSS, VSSQ pads may not exceed 100mV.

The above conditions apply between Ta and power-off (controlled or uncontrolled).

Tb is the point when all supply voltages are within their respective min/max operating conditions. Reference voltages shall be within their respective min/max operating conditions a minimum of 5 clocks before CKE goes high.

For supply and reference voltage operating conditions, see 9.2.1.1 “Recommended DC Operating Conditions” table.

Power ramp duration t_{INIT0} (Tb - Ta) must be no greater than 20 mS.

8.2.3.2 CKE and clock

Beginning at Tb, CKE must remain low for at least tINIT1 = 100 nS, after which it may be asserted high. Clock must be stable at least tINIT2 = 5 x tCK prior to the first low to high transition of CKE (Tc). CKE, CS_n and CA inputs must observe setup and hold time (tIS, tIH) requirements with respect to the first rising clock edge (as well as to the subsequent falling and rising edges).

The clock period shall be within the range defined for tCKb (18 nS to 100 nS), if any Mode Register Reads are performed. Mode Register Writes can be sent at normal clock operating frequencies so long as all AC Timings are met. Furthermore, some AC parameters (e.g. tDQSCK) may have relaxed timings (e.g. tDQSCKb) before the system is appropriately configured.
While keeping CKE high, issue NOP commands for at least tINIT3 = 200 μS. (Td).

8.2.3.3 Reset command

After t_{INIT3} is satisfied, a MRW(Reset) command shall be issued (Td). The memory controller may optionally issue a Precharge-All command prior to the MRW Reset command. Wait for at least t_{INIT4} = 1 μS while keeping CKE asserted and issuing NOP commands.

8.2.3.4 Mode Registers Reads and Device Auto-Initialization (DAI) polling:

After tINIT4 is satisfied (Te) only MRR commands and power-down entry/exit commands are allowed. Therefore, after Te, CKE may go low in accordance to Power-Down entry and exit specification (see section 8.4.24 “Power-Down”).

The MRR command may be used to poll the DAI-bit to acknowledge when Device Auto-Initialization is complete or the memory controller shall wait a minimum of t_{INIT5} before proceeding.

As the memory output buffers are not properly configured yet, some AC parameters may have relaxed timings before the system is appropriately configured.

After the DAI-bit (MR#0, “DAI”) is set to zero “DAI complete” by the memory device, the device is in idle state (Tf). The state of the DAI status bit can be determined by an MRR command to MR#0.

The LPDDR2 SDRAM device will set the DAI-bit no later than t_{INIT5} (10 μS) after the Reset command. The memory controller shall wait a minimum of t_{INIT5} or until the DAI-bit is set before proceeding.

After the DAI-Bit is set, it is recommended to determine the device type and other device characteristics by issuing MRR commands (MR0 “Device Information” etc.).

8.2.3.5 ZQ Calibration:

After t_{INIT5} (Tf), an MRW ZQ Initialization Calibration command may be issued to the memory (MR10). This command is used to calibrate the LPDDR2 output drivers (RON) over process, voltage, and temperature. Optionally, the MRW ZQ Initialization Calibration command will update MR0 to indicate RZQ pad connection. In systems in which more than one LPDDR2 device exists on the same bus, the controller must not overlap ZQ Calibration commands. The device is ready for normal operation after t_{ZQINIT}.

8.2.3.6 . Normal Operation:

After t_{ZQINIT} (Tg), MRW commands may be used to properly configure the memory, for example the output buffer driver strength, latencies etc. Specifically, MR1, MR2, and MR3 shall be set to configure the memory for the target frequency and memory configuration.

The LPDDR2 device will now be in IDLE state and ready for any valid command.

After Tg, the clock frequency may be changed according to the clock frequency change procedure described in section 8.4.26 “Input Clock Stop and Frequency Change”.

8.2.4 Initialization after Reset (without Power ramp)

If the RESET command is issued outside the power up initialization sequence, the reinitialization procedure shall begin with step 3 (Td).

8.2.5 Power-off Sequence

The following sequence shall be used to power off the LPDDR2 device.

While removing power, CKE shall be held at a logic low level (≤ 0.2 x VDD2), all other inputs shall be between VILmin and VIHmax. The LPDDR2 device will only guarantee that outputs are in a high impedance state while CKE is held low.

DQ, DM, DQS_t and DQS_c voltage levels must be between VSSQ and VDDQ during power off sequence to avoid latch-up. CK_t, CK_c, CS_n and CA input levels must be between VSS and VDD2 during power off sequence to avoid latch-up.

Tx is the point where any power supply decreases under its minimum value specified in 9.2.1.1 “Recommended DC Operating Conditions” table.

Tz is the point where all power supplies are below 300 mV. After Tz, the device is powered off.

The time between Tx and Tz (tPOFF) shall be less than 2s.

The following conditions apply:

Between Tx and Tz, VDD1 must be greater than VDD2 - 200 mV.

Between Tx and Tz, VDD1 and VDD2 must be greater than VDD2 - 200 mV.

Between Tx and Tz, VDD1 and VDD2 must be greater than VDDQ - 200 mV.

Between Tx and Tz, VREF must always be less than all other supply voltages.

The voltage difference between any of VSS, VSSQ, and VSS pads may not exceed 100 mV.

For supply and reference voltage operating conditions, see 9.2.1.1 “Recommended DC Operating Conditions” table.

8.2.6 Timing Parameters Power-Off

Maximum Power-Off Ramp Time is called tPOFF, it is 2s maximum.

8.2.7 Uncontrolled Power-Off Sequence

The following sequence shall be used to power off the LPDDR2 device under uncontrolled condition.

Tx is the point where any power supply decreases under its minimum value specified in the DC operating condition table. After turning off all power supplies, any power supply current capacity must be zero, except for any static charge remaining in the system.

Tz is the point where all power supply first reaches 300 mV. After Tz, the device is powered off.

The time between Tx and Tz (tPOFF) shall be less than 2s. The relative levels between supply voltages are uncontrolled during this period.

VDD1 and VDD2 shall decrease with a slope lower than 0.5 V/μS between Tx and Tz.

Uncontrolled power off sequence can be applied only up to 400 times in the life of the device.

8.3 Mode Register Definition

8.3.1 Mode Register Assignment and Definition

Each register is denoted as “R” if it can be read but not written, “W” if it can be written but not read, and “R/W” if it can be read and written.

Mode Register Read command shall be used to read a register. Mode Register Write command shall be used to write a register.

Mode Register Assignment

MR#	MA[7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
0	00H	Device Info.	R	(RFU)			RZQI		DNVI	DI	DAI
1	01H	Device Feature 1	W	nWR (for AP)			WC	BT	BL		
2	02H	Device Feature 2	W	(RFU)				RL & WL			
3	03H	I/O Config-1	W	(RFU)				DS			
4	04H	Refresh Rate	R	TUF	(RFU)				Refresh Rate		
5	05H	Basic Config-1	R	LPDDR2 Manufacturer ID							
6	06H	Basic Config-2	R	Revision ID1							
7	07H	Basic Config-3	R	Revision ID2							
8	08H	Basic Config-4	R	I/O width		Density				Type	
9	09H	Test Mode	W	Vendor-Specific Test Mode							
10	0AH	I/O Calibration	W	Calibration Code							
11-15	0BH~0FH	(reserved)	-	(RFU)							
16	10H	PASR_Bank	W	Bank Mask							
17	11H	(Reserved)	W	(RFU)							
18-19	12H~13H	(Reserved)	-	(RFU)							
20-31	14h - 1Fh	Reserved for NVM									
32	20H	DQ Calibration Pattern A	R	See 8.3.14 **“DQ Calibration”**							
33-39	21H~27H	(Do Not Use)	-								
40	28H	DQ Calibration Pattern B	R	See 8.3.15 **“DQ Calibration”**							
41-47	29H~2FH	(Do Not Use)	-								
48-62	30H~3EH	(Reserved)	-	(RFU)							
63	3FH	Reset	W	X							
64-126	40H~7EH	(Reserved)	-	(RFU)							
127	7FH	(Do Not Use)	-								
128-190	80H~BEH	(Reserved for Vendor Use)	-	(RFU)							
191	BFH	(Do Not Use)	-								
192-254	C0H~FEH	(Reserved for Vendor Use)	-	(RFU)							
255	FFH	(Do Not Use)	-								

Notes:
1. RFU bits shall be set to ‘0’ during Mode Register writes.
2. RFU bits shall be read as ‘0’ during Mode Register reads.
3. All Mode Registers that are specified as RFU or write-only shall return undefined data when read and DQS shall be toggled.
4. All Mode Registers that are specified as RFU shall not be written.
5. Writes to read-only registers shall have no impact on the functionality of the device.

8.3.2 MR0_Device Information (MA[7:0] = 00H

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)			RZQI		DNVI	DI	DAI

DAI (Device Auto-Initialization Status)	Read-only	OP0	**0b**: DAI complete **1b**: DAI still in progress
DI (Device Information)	Read-only	OP1	**0b**: S4 SDRAM
DNVI (Data Not Valid Information)	Read-only	OP2	**0b**: LPDDR2 SDRAM will not implement DNV functionalit
RZQI (Built in Self Test for RZQ Information)	Read-only	OP[4:3]	**00b:** RZQ self test not executed. **01b:** ZQ-pad may connect to VDDCA or float **10b:** ZQ-pad may short to GND **11b:** ZQ-pad self test completed, no error condition detected (ZQ-pad may not connect to VDDCA or float nor short to GND)

Notes:

1. RZQI will be set upon completion of the MRW ZQ Initialization Calibration command.
2. If ZQ is connected to VDD2 to set default calibration by user, OP[4:3] shall be read as 01. If user does not want to connect ZQ pad to VDD2, but OP[4:3] is read as 01 or 10, it might indicate a ZQ-pad assembly error. It is recommended that the assembly error being corrected first.
3. In the case of possible assembly error (either OP[4:3]=01 or OP[4:3]=10 as defined above), the LPDDR2 device will default to factory trim settings for RON, and will ignore ZQ calibration commands. In either case, the system may not function as intended.
4. In the case of the ZQ self-test returning a value of 11b, this result indicates that the device has detected a resistor connection to the ZQ pad. However, this result cannot be used to validate the ZQ resistor value or that the ZQ resistor tolerance meets the specified limits (i.e., 240 Ohm ± 1%).

8.3.3 MR1_Device Feature 1 (MA[7:0] = 01H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
nWR (for AP)			WC	BT	BL		

BL	Write-only	OP[2:0]	**010b**: BL4 (default) **011b**: BL8 **100b**: BL16 **All others:** reserved	
BT	Write-only	OP3	**0b**: Sequential (default) **1b**: Interleaved	
WC	Write-only	OP4	**0b**: Wrap (default) **1 b**: No wrap (allowed for SDRAM BL4 only)	
nWR	Write-only	OP[7:5]	**001b:** nWR=3 (default) **010b**: nWR=4 **011b:** nWR=5 **100b**: nWR=6 **101b**: nWR=7 **110b**: nWR=8 **All others:** reserved	1

Note:
1. Programmed value in nWR register is the number of clock cycles which determines when to start internal precharge operation for a write burst with AP enabled. It is determined by RU(tWR/tCK).

8.3.3.1 Burst Sequence by Burst Length (BL), Burst Type (BT), and Warp Control (WC)

C3	C2	C1	C0	WC	BT	BL	Burst Cycle Number and Burst Address Sequence															
							1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
X	X	0_B	0_B	wrap	any	4	0	1	2	3												
X	X	1_B	0_B				2	3	0	1												
X	X	X	0_B	nw	any		y	y+1	y+2	y+3												
X	0_B	0_B	0_B	wrap	seq	8	0	1	2	3	4	5	6	7								
X	0_B	1_B	0_B				2	3	4	5	6	7	0	1								
X	1_B	0_B	0_B				4	5	6	7	0	1	2	3								
X	1_B	1_B	0_B				6	7	0	1	2	3	4	5								
X	0_B	0_B	0_B		int		0	1	2	3	4	5	6	7								
X	0_B	1_B	0_B				2	3	0	1	6	7	4	5								
X	1_B	0_B	0_B				4	5	6	7	0	1	2	3								
X	1_B	1_B	0_B				6	7	4	5	2	3	0	1								
X	X	X	0_B	nw	any		illegal (not allowed)															
0_B	0_B	0_B	0_B	wrap	seq	16	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0_B	0_B	1_B	0_B				2	3	4	5	6	7	8	9	A	B	C	D	E	F	0	1
0_B	1_B	0_B	0_B				4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3
0_B	1_B	1_B	0_B				6	7	8	9	A	B	C	D	E	F	0	1	2	3	4	5
1_B	0_B	0_B	0_B				8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7
1_B	0_B	1_B	0_B				A	B	C	D	E	F	0	1	2	3	4	5	6	7	8	9
1_B	1_B	0_B	0_B				C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B
1_B	1_B	1_B	0_B				E	F	0	1	2	3	4	5	6	7	8	9	A	B	C	D
X	X	X	0_B		int		illegal (not allowed)															
X	X	X	0_B	nw	any		illegal (not allowed)															

Notes:
1. C0 input is not present on CA bus. It is implied zero.
2. For BL=4, the burst address represents C[1: 0].
3. For BL=8, the burst address represents C[2:0].
4. For BL=16, the burst address represents C[3:0].
5. For no-wrap (nw), BL4, the burst shall not cross the page boundary and shall not cross sub-page boundary. The variable y may start at any address with C0 equal to 0 and may not start at any address shown in table below.

8.3.3.2 Non Wrap Restrictions

	1Gb
Not across full page boundary	
x32	1FE, 1FF, 000, 001
Not across sub page boundary	
x32	None

NOTE 1 Non-wrap BL=4 data-orders shown above are prohibited.

8.3.4 MR2_Device Feature 2 (MA[7:0] = 02H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)				RL & WL			

RL & WL	Write-only	OP[3:0]	**0001b:** RL = 3 / WL = 1 (default) **0010b:** RL = 4 / WL = 2 **0011b:** RL = 5 / WL = 2 **0100b:** RL = 6 / WL = 3 **0101b:** RL = 7 / WL = 4 **0110b:** RL = 8 / WL = 4 **All others:** reserved

8.3.5 MR3_I/O Configuration 1 (MA[7:0] = 03H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)				DS			

DS	Write-only	OP[3:0]	**0000$_b$:** reserved **0001$_b$:** 34.3-ohm typical **0010$_b$:** 40-ohm typical (default) **0011$_b$:** 48-ohm typical **0100$_b$:** 60-ohm typical **0101$_b$:** reserved **0110$_b$:** 80-ohm typical **0111$_b$:** 120-ohm typical **All others:** reserved

8.3.6 MR4_Device Temperature (MA[7:0] = 04H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
TUF	(RFU)				SDRAM Refresh Rate		

SDRAM Refresh Rate	Read-only	OP[2:0]	**000b**: SDRAM Low temperature operating limit exceeded **001b**: 4x tREFI, 4x tREFW **010b**: 2x tREFI, 2x tREFW **011b**: 1x tREFI, 1x tREFW (≤ 85°C) **100b**: Reserved **101b**: 0.25x tREFI, 0.25x tREFW, do not de-rate SDRAM AC timing **110b**: 0.25x tREFI, 0.25x tREFW, de-rate SDRAM AC timing **111b**: SDRAM High temperature operating limit exceeded
Temperature Update Flag (TUF)	Read-only	OP7	**0b**: OP[2:0] value has not changed since last read of MR4. **1b**: OP[2:0] value has changed since last read of MR4.

Notes:
1. A Mode Register Read from MR4 will reset OP7 to '0'.
2. OP7 is reset to '0' at power-up.
3. If OP2 equals '1', the device temperature is greater than 85°C.
4. OP7 is set to '1' if OP2:OP0 has changed at any time since the last read of MR4.
5. LPDDR2 might not operate properly when OP[2:0] = 000b or 111b.
6. For specified operating temperature range and maximum operating temperature, refer to "Operating Temperature Conditions" table.
7. LPDDR2 devices must be derated by adding 1.875 nS to the following core timing parameters: tRCD, tRC, tRAS, tRP, and tRRD. tDQSCK shall be de-rated according to the tDQSCK de-rating value in "LPDDR2 AC Timing" table. Prevailing clock frequency spec and related setup and hold timings shall remain unchanged.
8. The recommended frequency for reading MR4 is provided in "Temperature Sensor" section.

8.3.7 MR5_Basic Configuration 1 (MA[7:0] = 05H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
LPDDR2 Manufacturer ID							

LPDDR2 Manufacturer ID	Read-only	OP[7:0]	0001 1010b:UniIC

8.3.8 MR6_Basic Configuration 2 (MA[7:0] = 06H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID1							

Revision ID1	Read-only	OP[7:0]	00000000b: A-version

Note: MR6 is Vendor Specific.

8.3.9 MR7_Basic Configuration 3 (MA[7:0] = 07H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID2							

Revision ID2	Read-only	OP[7:0]	00000000b: A-version

Note: MR7 is Vendor Specific.

8.3.10 MR8_Basic Configuration 4 (MA[7:0] = 08H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
I/O width		Density				Type	

Type	Read-only	OP[1:0]	**00b**: S4 SDRAM
Density	Read-only	OP[5:2]	**0011b**: 1G
I/O width	Read-only	OP[7:6]	**00b**: x32

8.3.11 MR9_Test Mode (MA[7:0] = 09H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Vendor-specific Test Mode							

8.3.12 MR10_Calibration (MA[7:0] = 0AH)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Calibration Code							

Calibration Code	Write-only	OP[7:0]	**0xFF:** Calibration command after initialization **0xAB:** Long calibration **0x56:** Short calibration **0xC3:** ZQ Reset **others:** Reserved

Notes:
1. Host processor shall not write MR10 with “Reserved” values.
2. LPDDR2 devices shall ignore calibration command when a “Reserved” value is written into MR10.
3. See AC timing table for the calibration latency.
4. If ZQ is connected to VSS through RZQ, either the ZQ calibration function (see section 8.4.23 “Mode Register Write ZQ Calibration Command”) or default calibration (through the ZQreset command) is supported. If ZQ is connected to VDD2, the device operates with default calibration, and ZQ calibration commands are ignored. In both cases, the ZQ connection shall not change after power is applied to the device.
5. The MRW ZQ Initialization Calibration command will update MR0 to indicate RZQ pad connection.

8.3.13 MR16_PASR_Bank Mask (MA[7:0] = 10H)

	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
S4 DRAM	**Bank Mask(8Banks)**							

Bank[7:0]Mask	Write-only	OP<7:0>	0b:Refresh enable to the bank(=unmasked default) 1b:Refresh blocked(=masked) OP0:bank0 OP1:bank1 OP2:bank2 OP3:bank3 OP4:bank4 OP5:bank5 OP6:bank6 OP7:bank7

Note: The MR16 is used to control which bank or banks are to be masked or unmasked in self-refresh mode. It has no effect in auto-refresh mode because LPDDR2 1Gb device does not support per-bank refresh in auto-refresh mode.

OP	Bank Mask	4-Bank S4 SDRAM
0	XXXXXXX1	Bank 0
1	XXXXXX1X	Bank 1
2	XXXXX1XX	Bank 2
3	XXXX1XXX	Bank 3
4	XXX1XXXX	Bank4
5	XX1XXXXX	Bank5
6	X1XXXXXX	Bank6
7	1XXXXXXX	Bank7

8.3.14 MR32_DQ Calibration Pattern A (MA[7:0] = 20H)

Reads to MR32 return DQ Calibration Pattern “A”. See section 8.4.20.2 “DQ Calibration”.

8.3.15 MR40_DQ Calibration Pattern B (MA[7:0] = 28H)

Reads to MR40 return DQ Calibration Pattern “B”. See section 8.4.20.2 “DQ Calibration”.

8.3.16 MR63_Reset (MA[7:0] = 3FH): MRW only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
X							

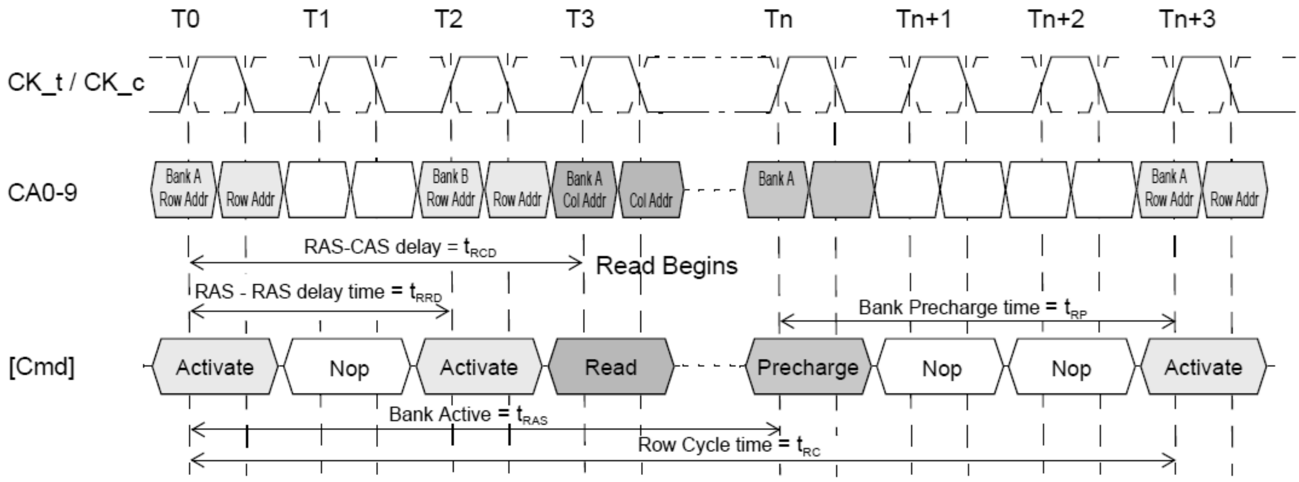
For additonal information on MRW RESET see section 8.4.21 “Mode Register Write Command”.

8.4 Command Definitions and Timing Diagrams

8.4.1 Activate Command

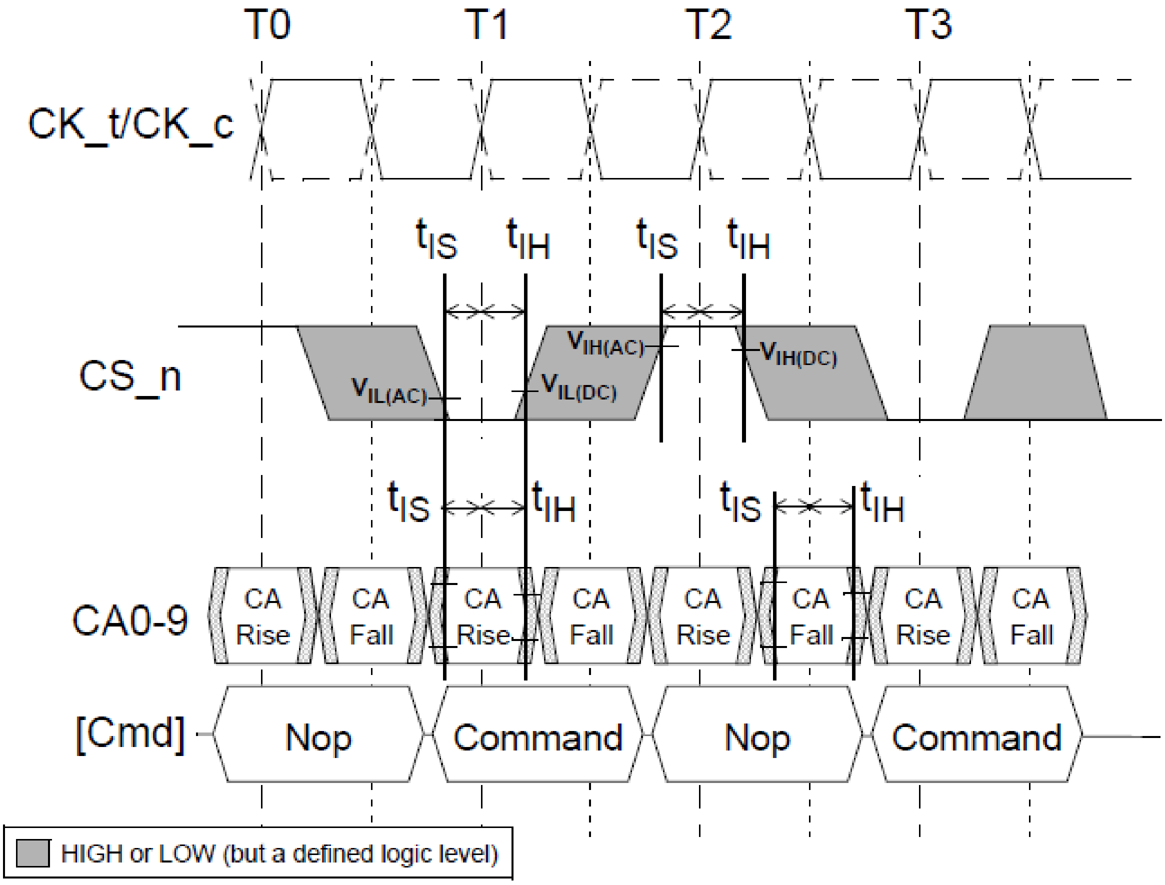
The SDRAM Activate command is issued by holding CS_n LOW, CA0 LOW, and CA1 HIGH at the rising edge of the clock. The bank addresses are used to select the desired bank. The row addresses are used to determine which row to activate in the selected bank. The Activate command must be applied before any Read or Write operation can be executed. The LPDDR2 SDRAM can accept a read or write command at time tRCD after the activate command is sent. Once a bank has been activated it must be precharged before another Activate command can be applied to the same bank. The bank active and precharge times are defined as tRAS and tRP, respectively. The minimum time interval between successive Activate commands to the same bank is determined by the RAS cycle time of the device (tRC). The minimum time interval between Activate commands to different banks is tRRD.

8.4.1.1 Activate Command Cycle: tRCD = 3, tRP = 3, tRRD = 2



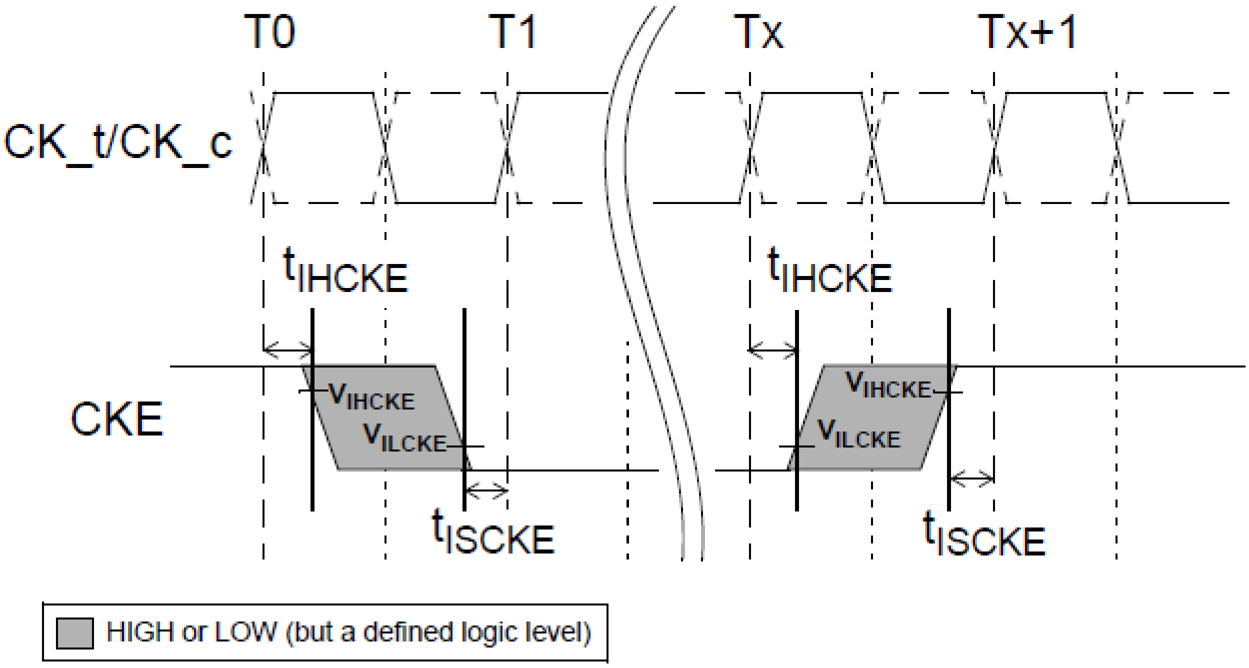
Note:
A Precharge-All command uses tRPab timing, while a Single Bank Precharge command uses tRPpb timing. In this figure, tRP is used to denote either an All-bank Precharge or a Single Bank Precharge

8.4.1.2 Command Input Setup and Hold Timing



Note: Setup and hold conditions also apply to the CKE pad. See section related to power down for timing diagrams related to the CKE pad.

8.4.1.3 CKE Input Setup and Hold Timing



Notes:
1. After CKE is registered LOW, CKE signal level shall be maintained below VILCKE for tCKE specification (LOW pulse width).
2. After CKE is registered HIGH, CKE signal level shall be maintained above VIHCKE for tCKE specification (HIGH pulse width).

8.4.2 Read and Write Access Modes

After a bank has been activated, a read or write cycle can be executed. This is accomplished by setting CS_n LOW, CA0 HIGH, and CA1 LOW at the rising edge of the clock. CA2 must also be defined at this time to determine whether the access cycle is a READ operation (CA2 HIGH) or a WRITE operation (CA2 LOW).

The LPDDR2 SDRAM provides a fast column access operation. A single Read or Write Command will initiate a burst read or write operation on successive clock cycles.

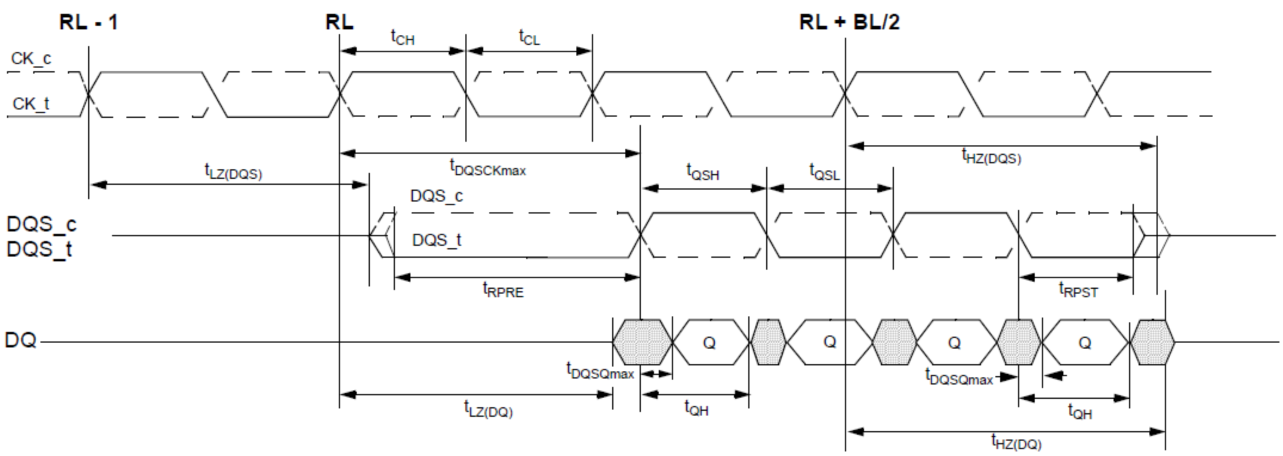
A new burst access must not interrupt the previous 4-bit burst operation in case of BL = 4 setting. In case of BL = 8 and BL = 16 settings, Reads may be interrupted by Reads and Writes may be interrupted by Writes provided that this occurs on even clock cycles after the Read or Write command and tCCD is met.

8.4.3 Burst Read Command

The Burst Read command is initiated by having CS_n LOW, CA0 HIGH, CA1 LOW and CA2 HIGH at the rising edge of the clock. The command address bus inputs, CA5r-CA6r and CA1f-CA9f, determine the starting column address for the burst. The Read Latency (RL) is defined from the rising edge of the clock on which the Read Command is issued to the rising edge of the clock from which the tDQSCK delay is measured. The first valid datum is available RL * tCK + tDQSCK + tDQSQ after the rising edge of the clock where the Read Command is issued. The data strobe output is driven LOW tRPRE before the first rising valid strobe edge. The first bit of the burst is synchronized with the first rising edge of the data strobe. Each subsequent data-out appears on each DQ pad edge aligned with the data strobe. The RL is programmed in the mode registers.

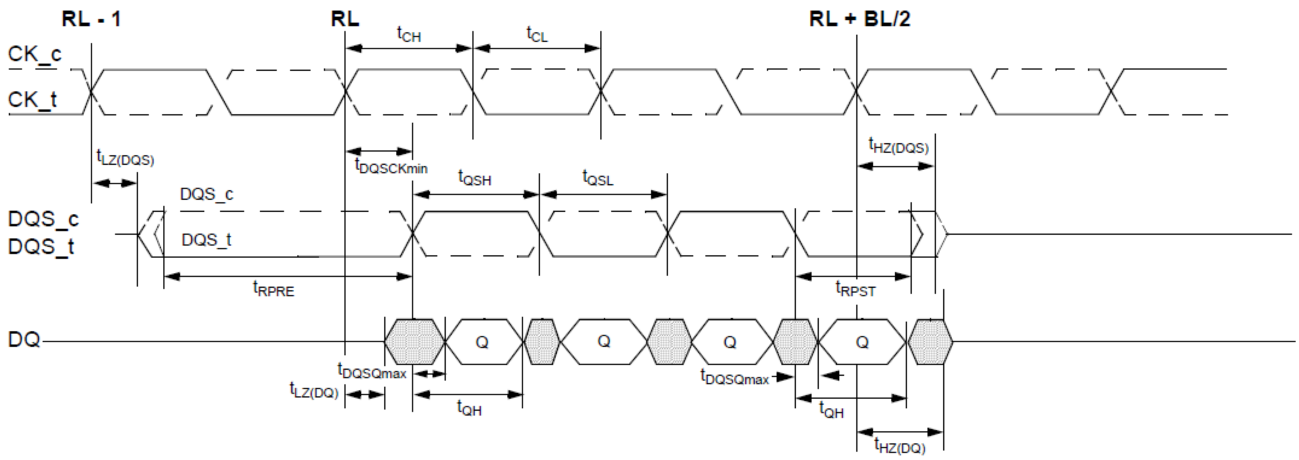
Timings for the data strobe are measured relative to the crosspoint of DQS_t and its complement, DQS_c.

8.4.3.1 Data Output (Read) Timing (tDQSCKmax)



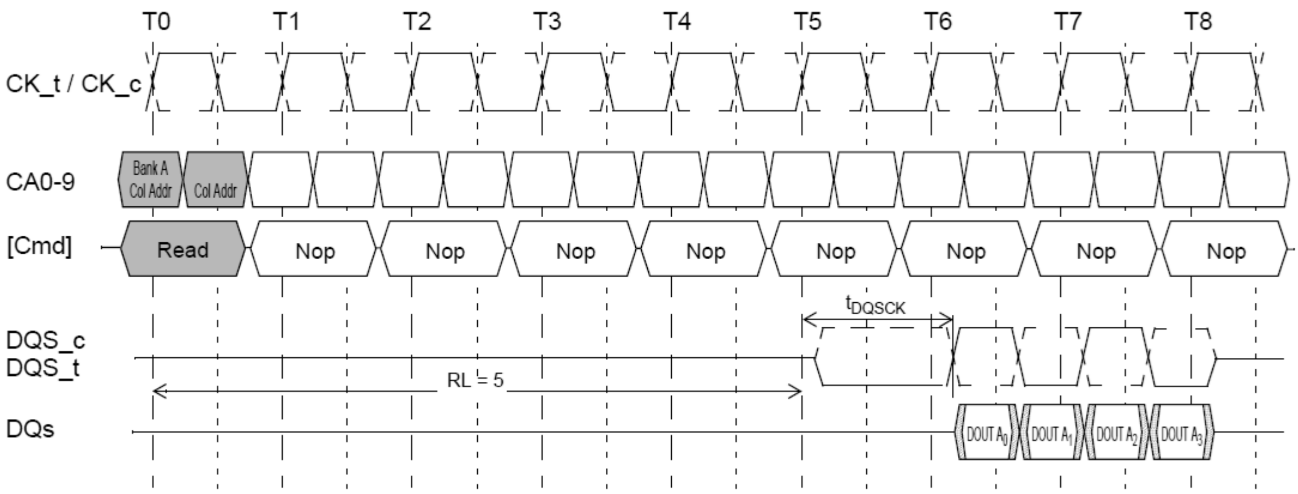
Notes:
1. tDQSCK may span multiple clock periods.
2. An effective Burst Length of 4 is shown.

8.4.3.2 Data Output (Read) Timing (tDQSCKmin)

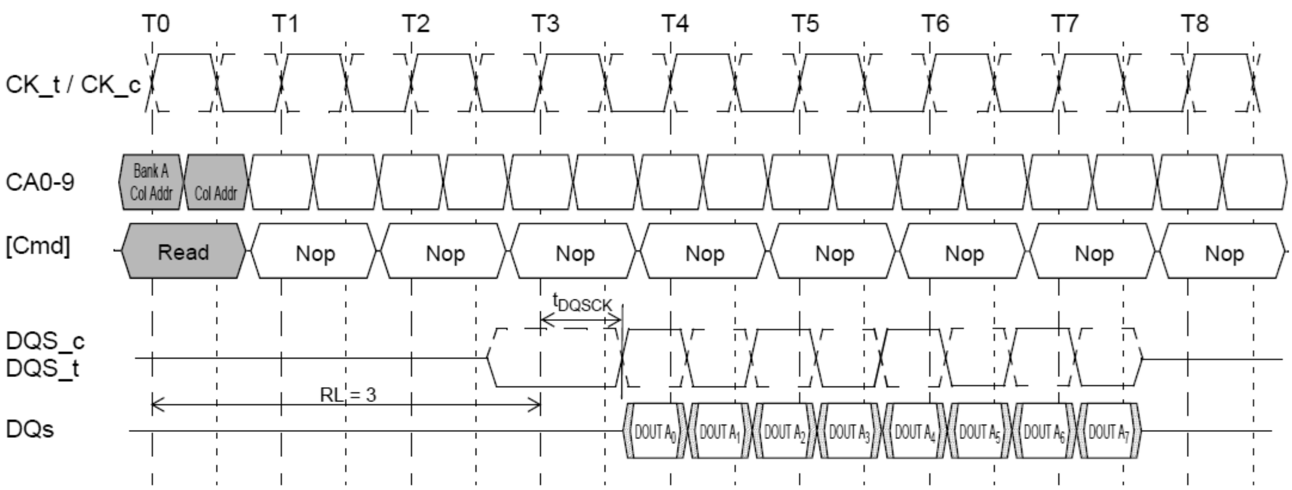


Note: An effective Burst Length of 4 is shown.

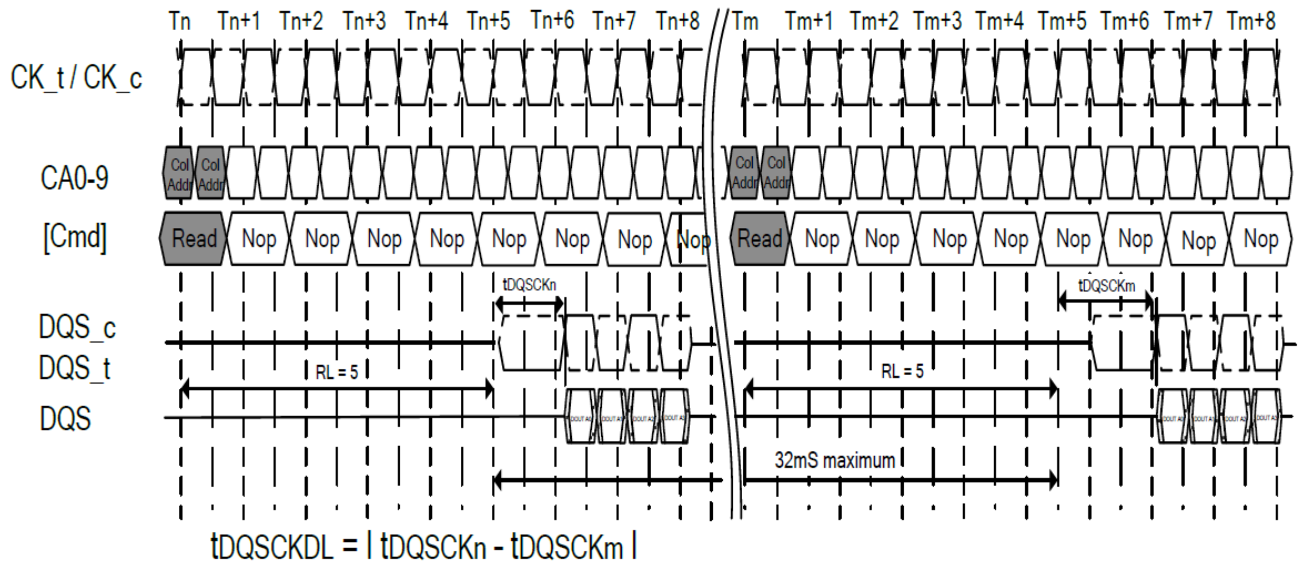
8.4.3.3 Burst Read: RL = 5, BL = 4, tDQSCK > tCK



8.4.3.4 Burst Read: RL = 3, BL = 8, tDQSCK < tCK

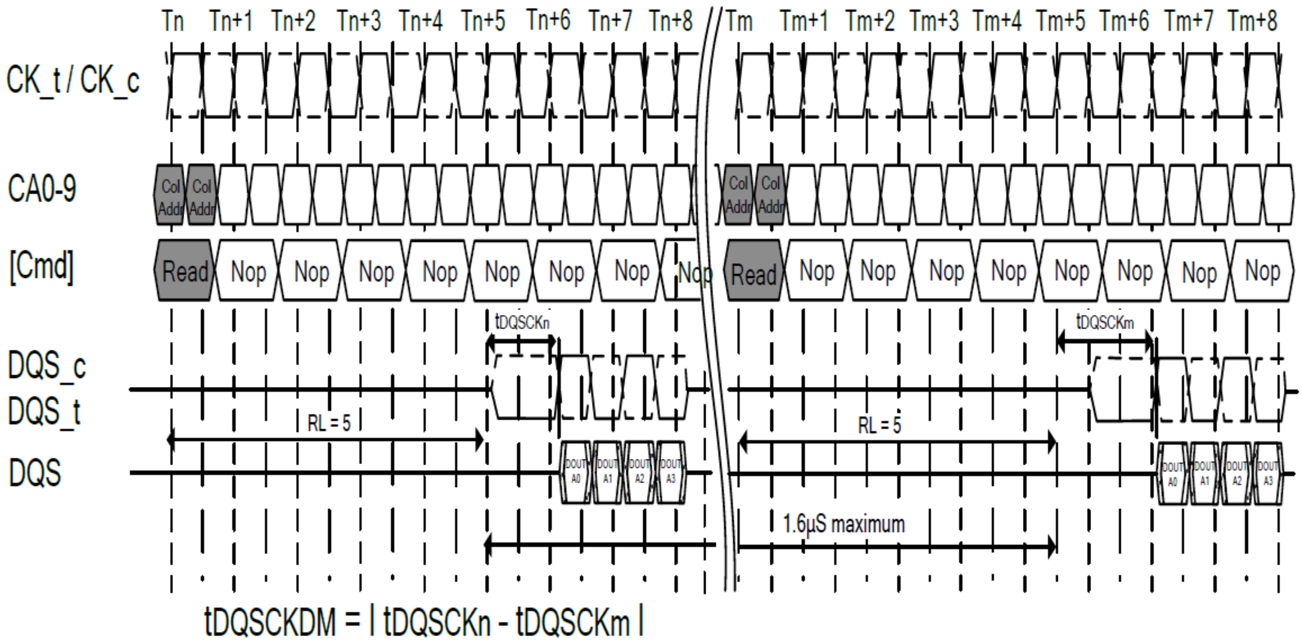


8.4.3.5 LPDDR2: tDQSCKDL Timing



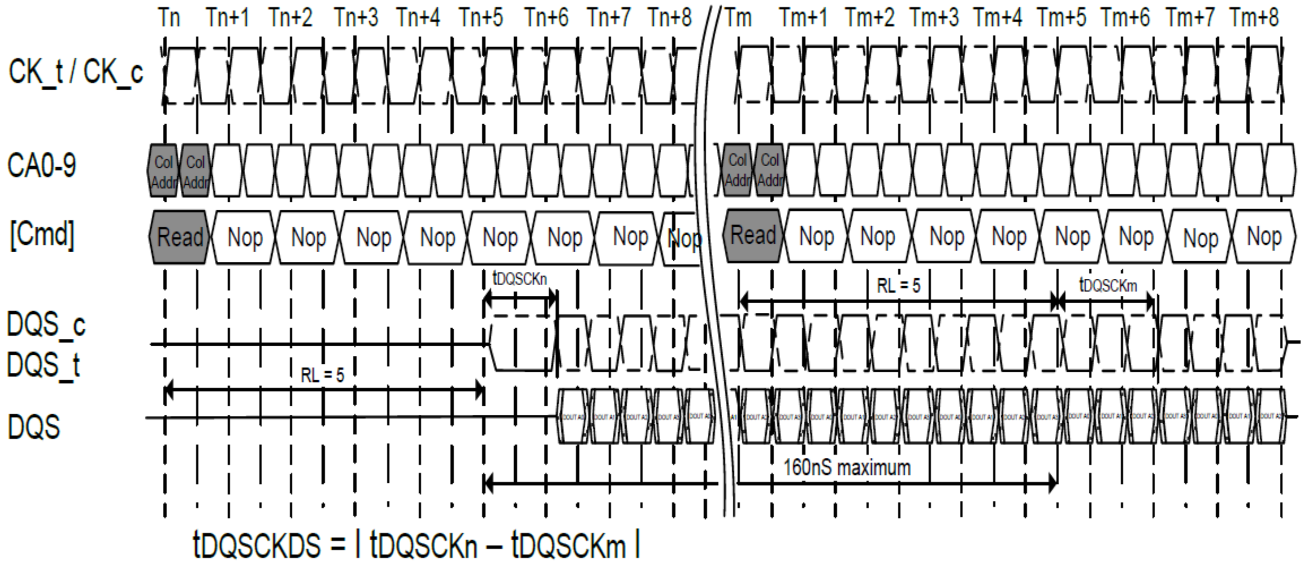
Note: tDQSCKDLmax is defined as the maximum of ABS(tDQSCKn - tDQSCKm) for any {tDQSCKn ,tDQSCKm} pair within any 32mS rolling window.

8.4.3.6 LPDDR2: tDQSCKDM Timing



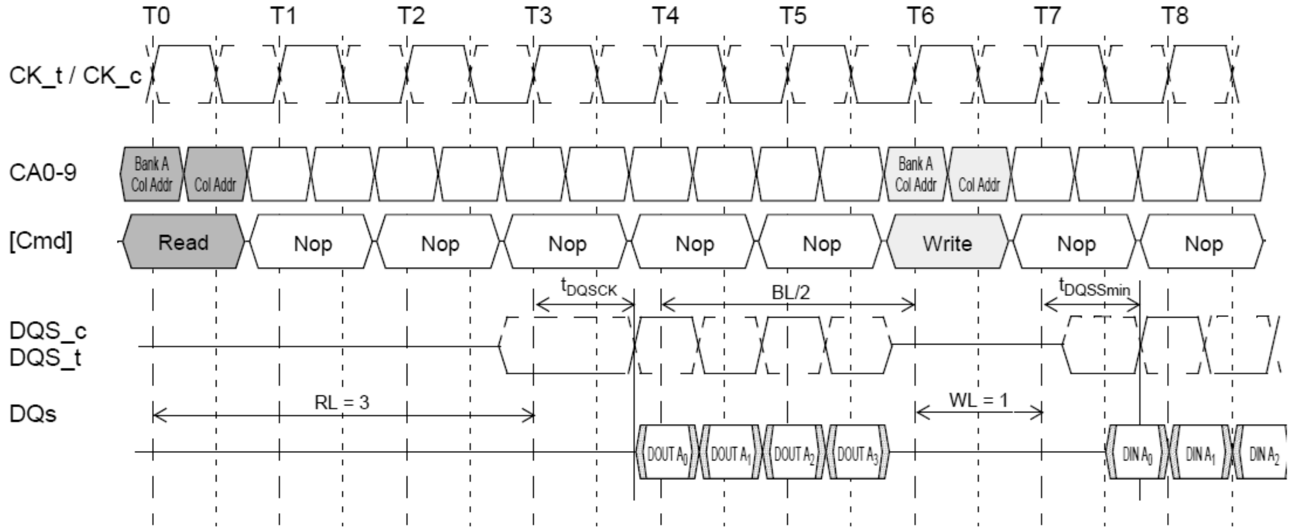
Note: tDQSCKDMmax is defined as the maximum of ABS(tDQSCKn - tDQSCKm) for any {tDQSCKn,tDQSCKm} pair within any 1.6µS rolling window.

8.4.3.7 LPDDR2: tDQSCKDS Timing



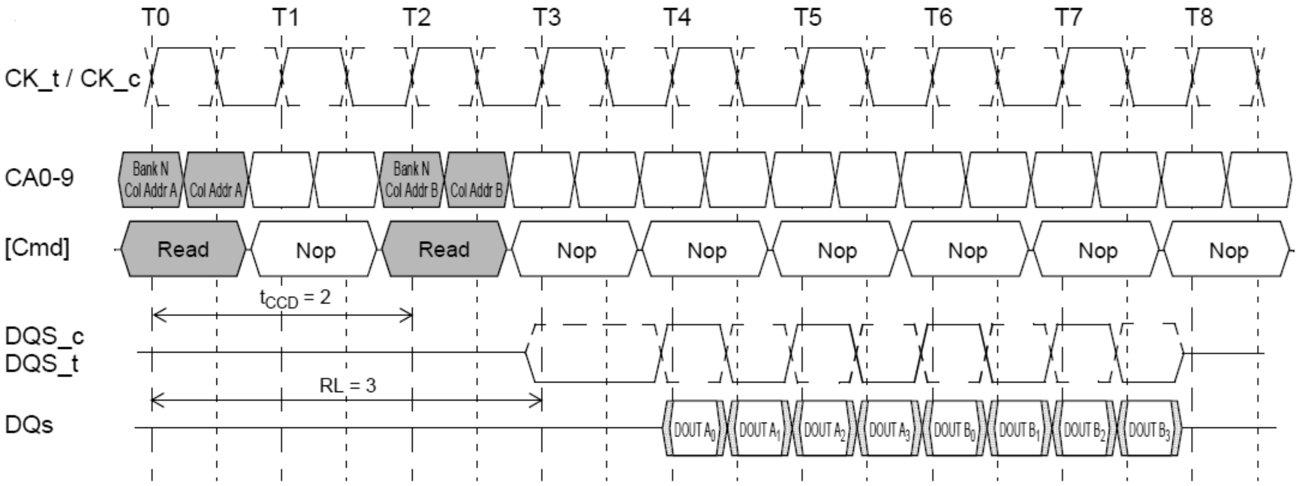
Note:
tDQSCKDSmax is defined as the maximum of ABS(tDQSCKn - tDQSCKm) for any {tDQSCKn ,tDQSCKm} pair for reads within a consecutive burst within any 160nS rolling window

8.4.3.8 Burst Read Followed by Burst Write: RL = 3, WL = 1, BL = 4



The minimum time from the burst read command to the burst write command is defined by the Read Latency (RL) and the Burst Length (BL). Minimum read to write latency is RL + RU(tDQSCKmax/tCK) + BL/2 + 1 - WL clock cycles. Note that if a read burst is truncated with a Burst Terminate (BST) command, the effective burst length of the truncated read burst should be used as “BL” to calculate the minimum read to write delay.

8.4.3.9 Seamless Burst Read: RL = 3, BL= 4, tCCD = 2



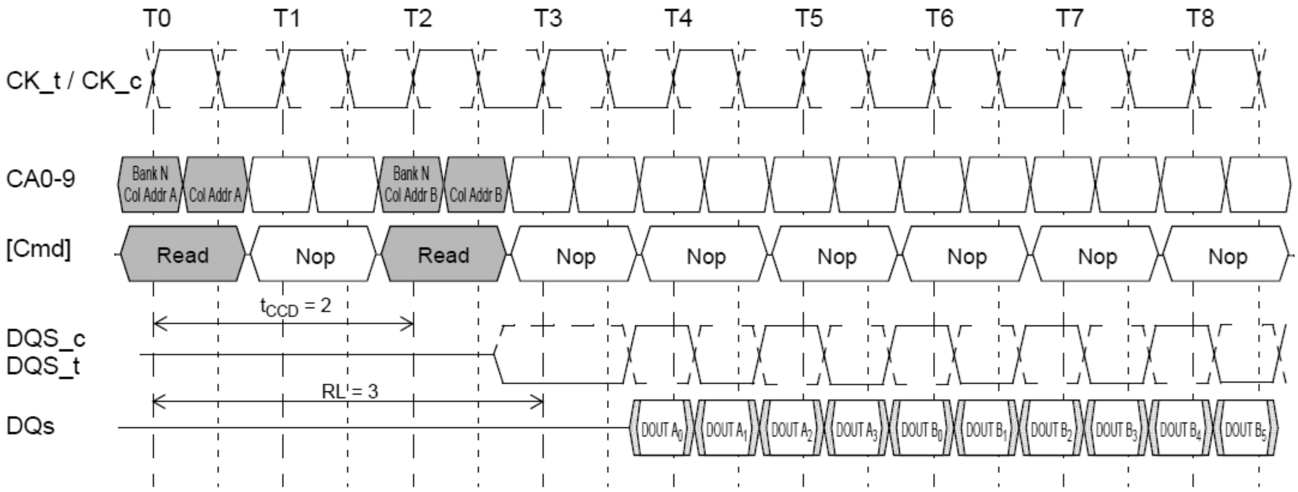
The seamless burst read operation is supported by enabling a read command at every other clock for BL = 4 operation, every 4 clocks for BL = 8 operation, and every 8 clocks for BL=16 operation.

For LPDDR2-SDRAM, this operation is allowed regardless of whether the accesses read the same or different banks as long as the banks are activated.

8.4.4 Reads Interrupted by a Read

For LPDDR2-S4 device, burst read can be interrupted by another read on even clock cycles after the Read command, provided that tCCD is met.

8.4.4.1 Read Burst Interrupt Example: RL = 3, BL= 8, tCCD = 2



Notes:
1. For LPDDR2-S4 devices, read burst interrupt function is only allowed on burst of 8 and burst of 16.
2. For LPDDR2-S4 devices, read burst interrupt may occur on any clock cycle after the initial read command, provided that tCCD is met.
3. Reads can only be interrupted by other reads or the BST command.
4. Read burst interruption is allowed to any bank inside DRAM.
5. Read burst with Auto-Precharge is not allowed to be interrupted.
6. The effective burst length of the first read equals two times the number of clock cycles between the first read and the interrupting read.

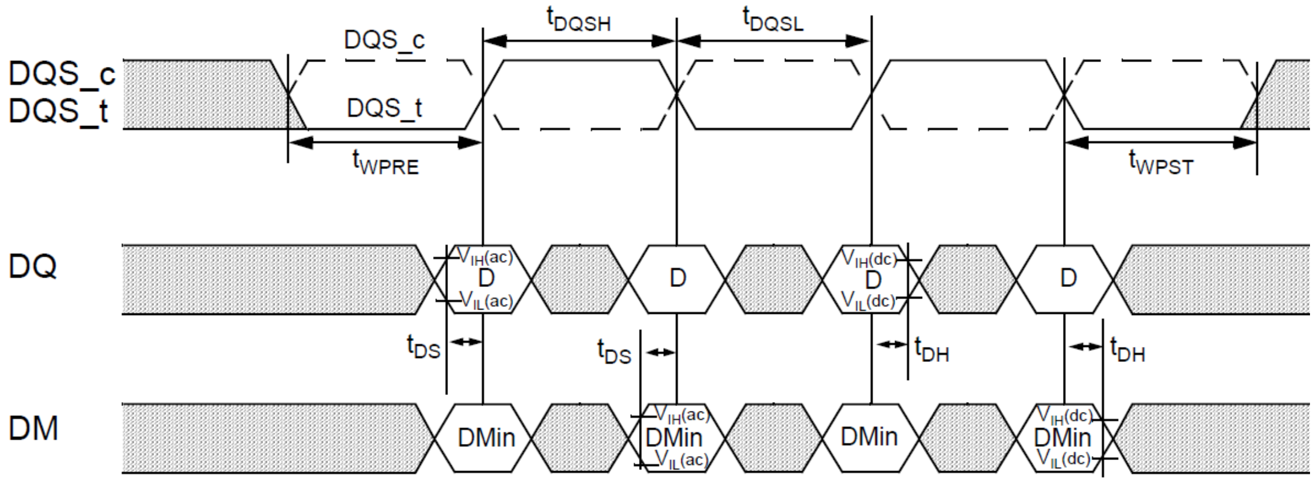
8.4.5 Burst Write Operation

The Burst Write command is initiated by having CS_n LOW, CA0 HIGH, CA1 LOW and CA2 LOW at the rising edge of the clock. The command address bus inputs, CA5r-CA6r and CA1f-CA9f, determine the starting column address for the burst. The Write Latency (WL) is defined from the rising edge of the clock on which the Write Command is issued to the rising edge of the clock from which the tDQSS delay is measured. The first valid data must be driven WL * tCK + tDQSS from the rising edge of the clock from which the Write command is issued. The data strobe signal (DQS) should be driven LOW tWPRE prior to the data input. The data bits of the burst cycle must be applied to the DQ pads tDS prior to the respective edge of the DQS_t, DQS_c and held valid until tDH after that edge. The burst data are sampled on successive edges of the DQS_t, DQS_c until the burst length is completed, which is 4, 8, or 16 bit burst.

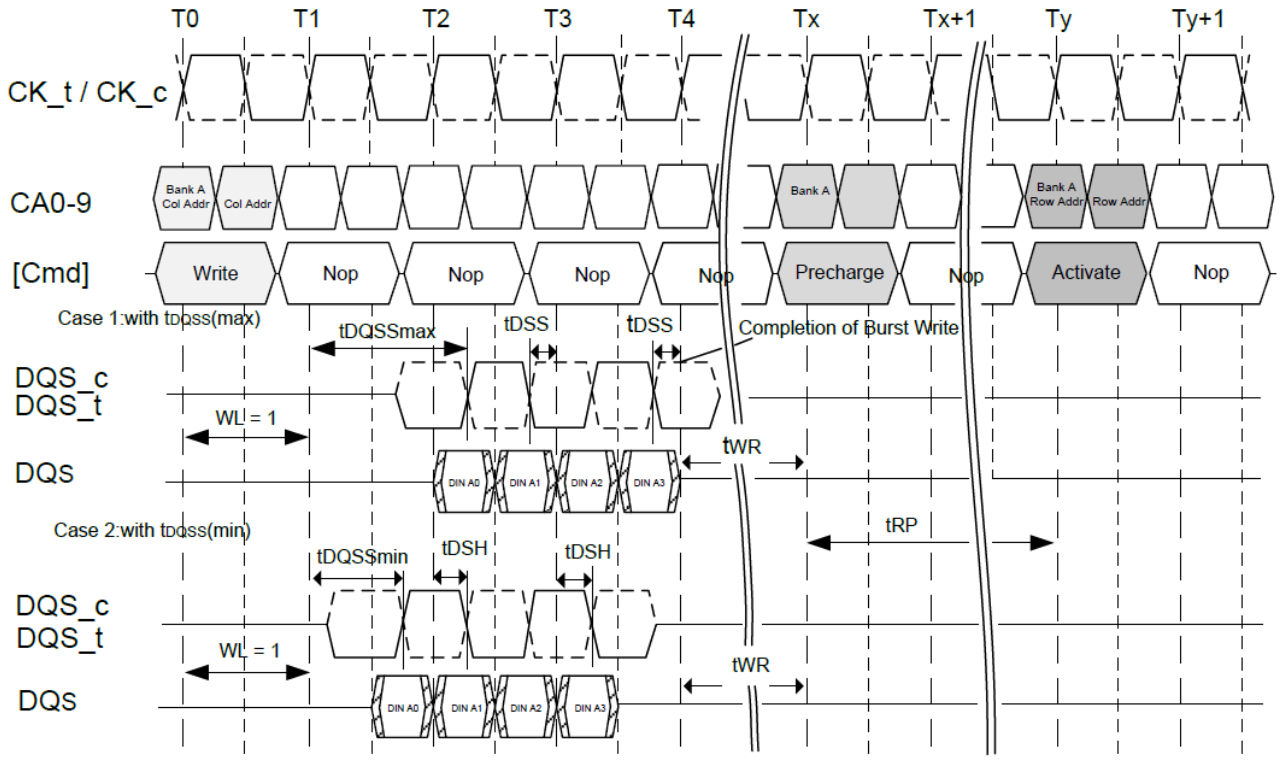
For LPDDR2-SDRAM devices, tWR must be satisfied before a precharge command to the same bank may be issued after a burst write operation.

Input timings are measured relative to the cross point of DQS_t and its complement, DQS_c.

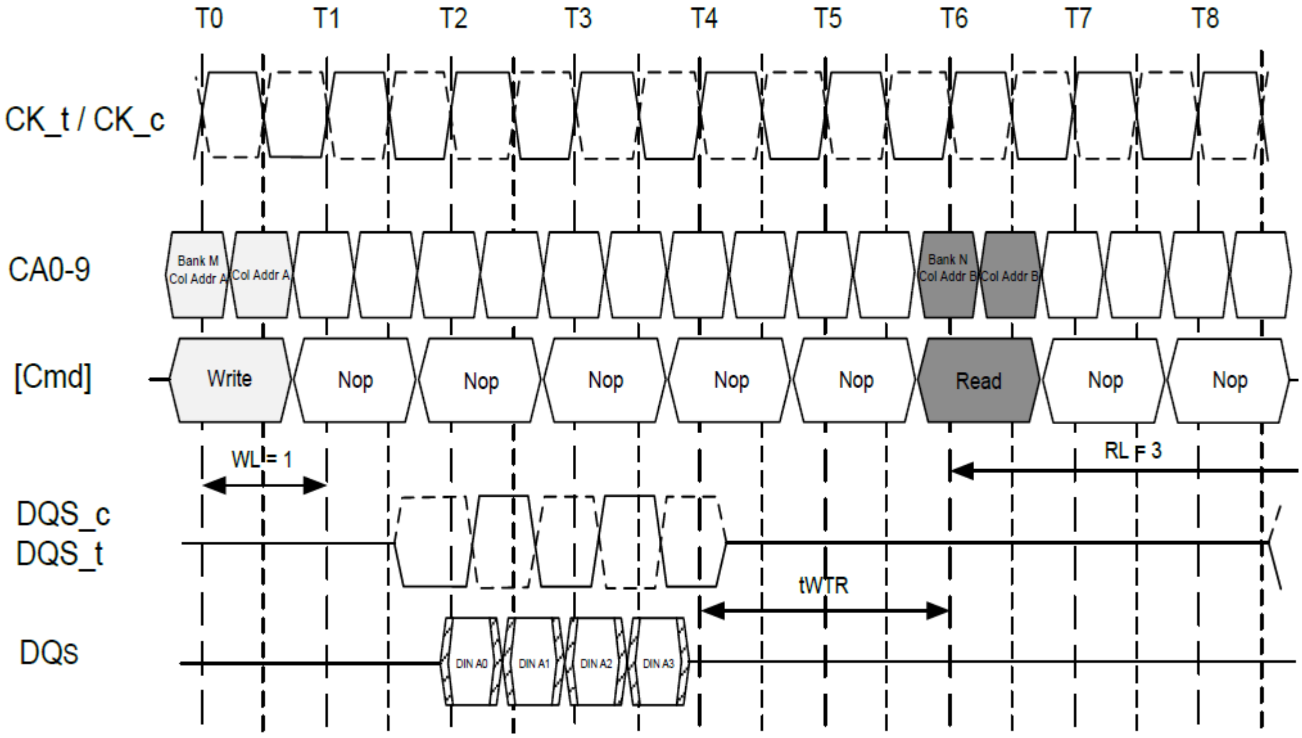
8.4.5.1 Data Input (Write) Timing



8.4.5.2 Burst Write: WL = 1, BL= 4

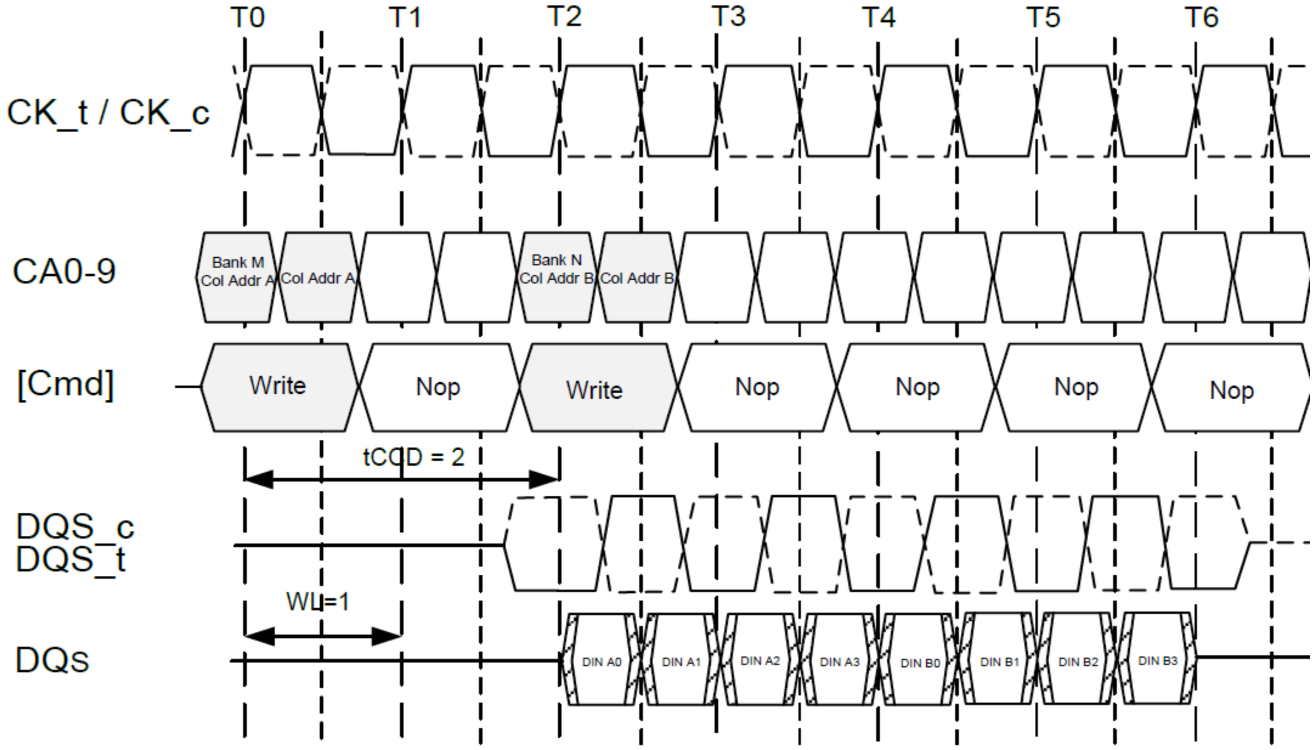


8.4.5.3 Burst Write Followed by Burst Read: RL = 3, WL= 1, BL= 4



Notes:
1. The minimum number of clock cycles from the burst write command to the burst read command for any bank is [WL + 1 + BL/2 + RU(tWTR/tCK)].
2. tWTR starts at the rising edge of the clock after the last valid input datum.
3. If a write burst is truncated with a Burst Terminate (BST) command, the effective burst length of the truncated write burst should be used as “BL” to calculate the minimum write to read delay.

8.4.5.4 Seamless Burst Write: WL= 1, BL = 4, tCCD = 2



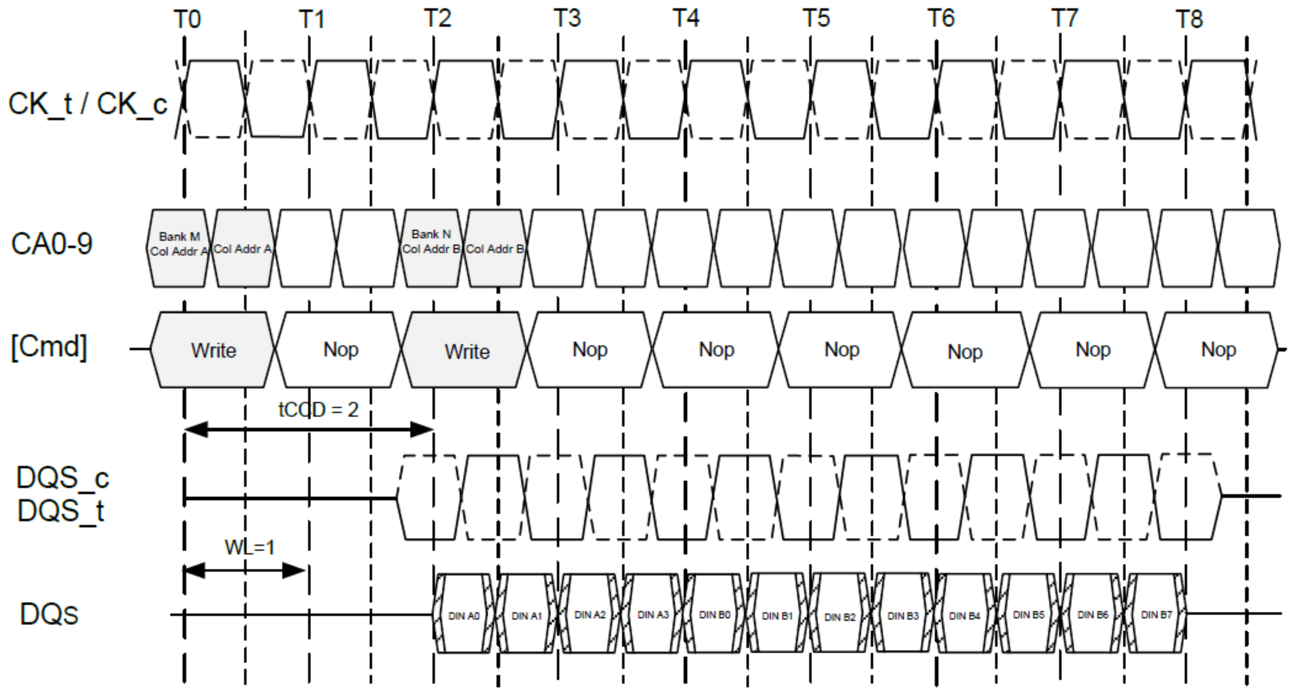
Note:

The seamless burst write operation is supported by enabling a write command every other clock for BL = 4 operation, every four clocks for BL = 8 operation, or every eight clocks for BL = 16 operation. This operation is allowed regardless of same or different banks as long as the banks are activated

8.4.5.5 Writes Interrupted by a Write

For LPDDR2-S4 devices, burst writes can only be interrupted by another write on even clock cycles after the write command, provided that tCCD(min) is met.

8.4.5.6 Write Burst Interrupt Timing: WL = 1, BL = 8, tCCD = 2



Notes:
1. For LPDDR2-S4 devices, write burst interrupt function is only allowed on burst of 8 and burst of 16.
2. For LPDDR2-S4 devices, write burst interrupt may only occur on even clock cycles after the previous write commands, provided that tCCD(min) is met.
3. Writes can only be interrupted by other writes or the BST command.
4. Write burst interruption is allowed to any bank inside DRAM.
5. Write burst with Auto-Precharge is not allowed to be interrupted.
6. The effective burst length of the first write equals two times the number of clock cycles between the first write and the interrupting write.

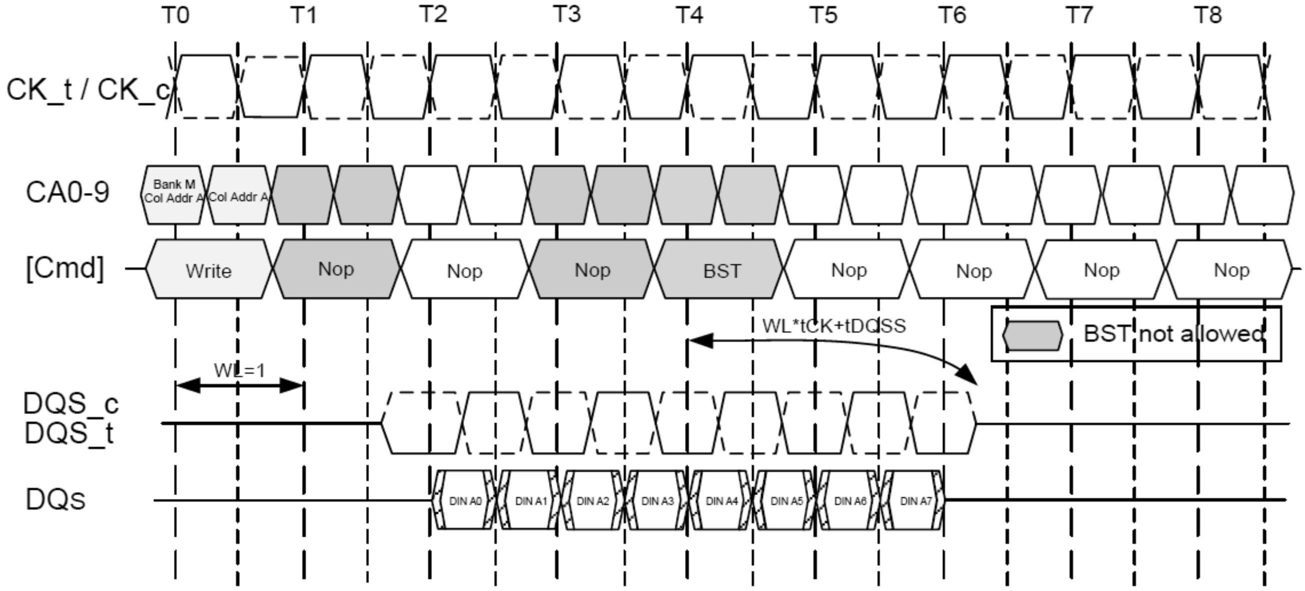
8.4.6 Burst Terminate

The Burst Terminate (BST) command is initiated by having CS_n LOW, CA0 HIGH, CA1 HIGH, CA2 LOW, and CA3 LOW at the rising edge of clock. A Burst Terminate command may only be issued to terminate an active Read or Write burst. Therefore, a Burst Terminate command may only be issued up to and including BL/2 - 1 clock cycles after a Read or Write command. The effective burst length of a Read or Write command truncated by a BST command is as follows:
Effective burst length = 2 x {Number of clock cycles from the Read or Write Command to the BST command}
Note that if a read or write burst is truncated with a Burst Terminate (BST) command, the effective burst length of the truncated burst should be used as “BL” to calculate the minimum read to write or write to read delay.

The BST command only affects the most recent read or write command. The BST command truncates an ongoing read burst RL * tCK + tDQSCK + tDQSQ after the rising edge of the clock where the Burst Terminate command is issued. The BST command truncates an ongoing write burst WL * tCK + tDQSS after the rising edge of the clock where the Burst Terminate command is issued.

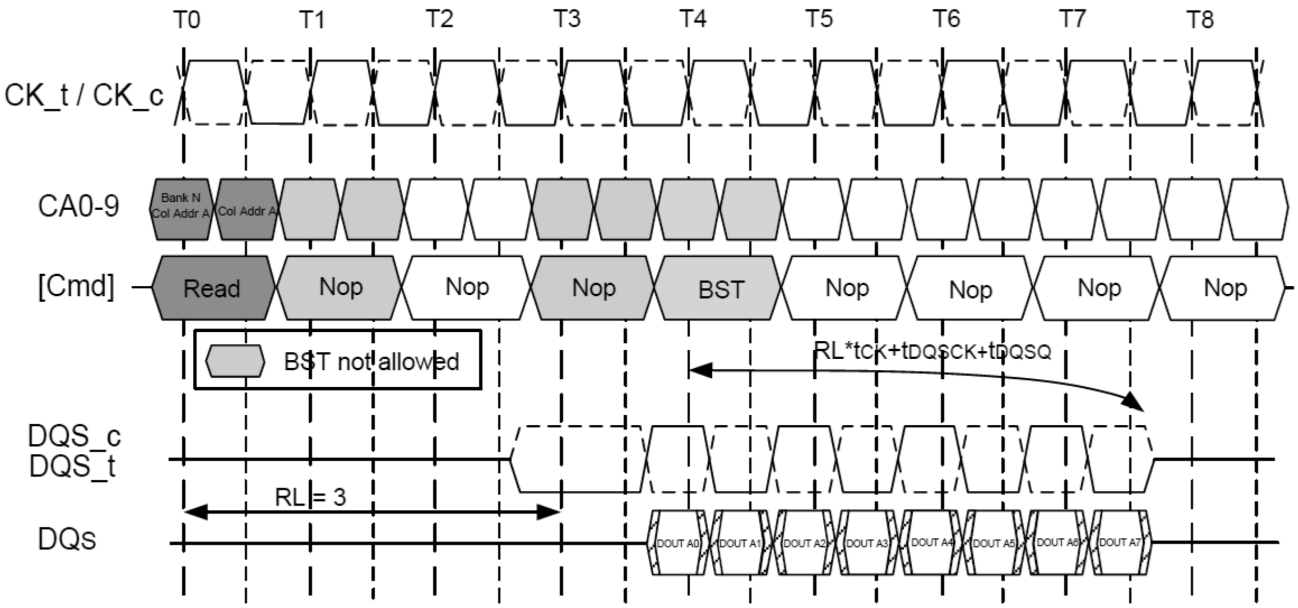
For LPDDR2-S4 devices, the 4-bit prefetch architecture allows the BST command to be issued on an even number of clock cycles after a Write or Read command. Therefore, the effective burst length of a Read or Write command truncated by a BST command is an integer multiple of 4.

8.4.6.1 Burst Write Truncated by BST: WL = 1, BL = 16



Notes:
1. The BST command truncates an ongoing write burst WL * tCK + tDQSS after the rising edge of the clock where the Burst Terminate command is issued.
2. For LPDDR2-S4 devices, BST can only be issued at even number of clock cycles after the Write command.
3. Additional BST commands are not allowed after T4 and may not be issued until after the next Read or Write command.

8.4.6.2 Burst Read Truncated by BST: RL = 3, BL = 16



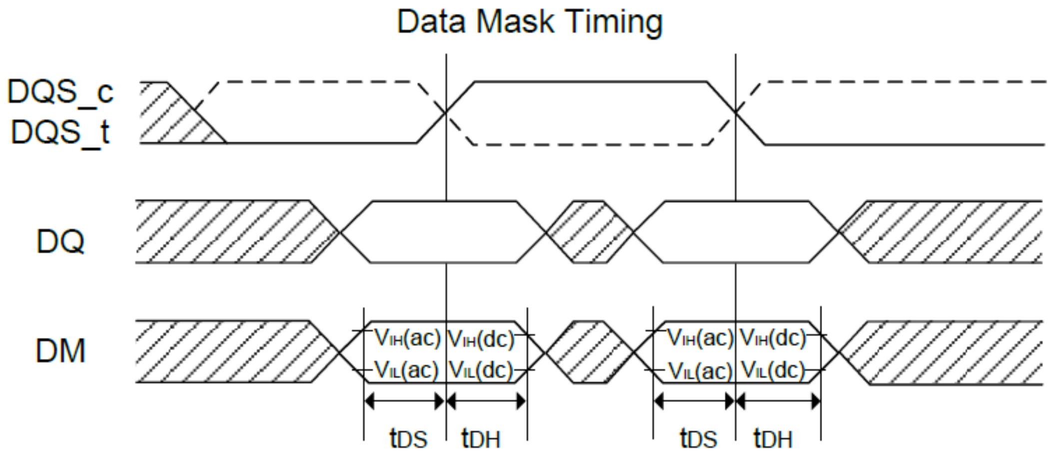
Notes:
1. The BST command truncates an ongoing read burst RL * tCK + tDQSCK + tDQSQ after the rising edge of the clock where the Burst Terminate command is issued.
2. For LPDDR2-S4 devices, BST can only be issued at even number of clock cycles after the Read command.
3. Additional BST commands are not allowed after T4 and may not be issued until after the next Read or Write command.

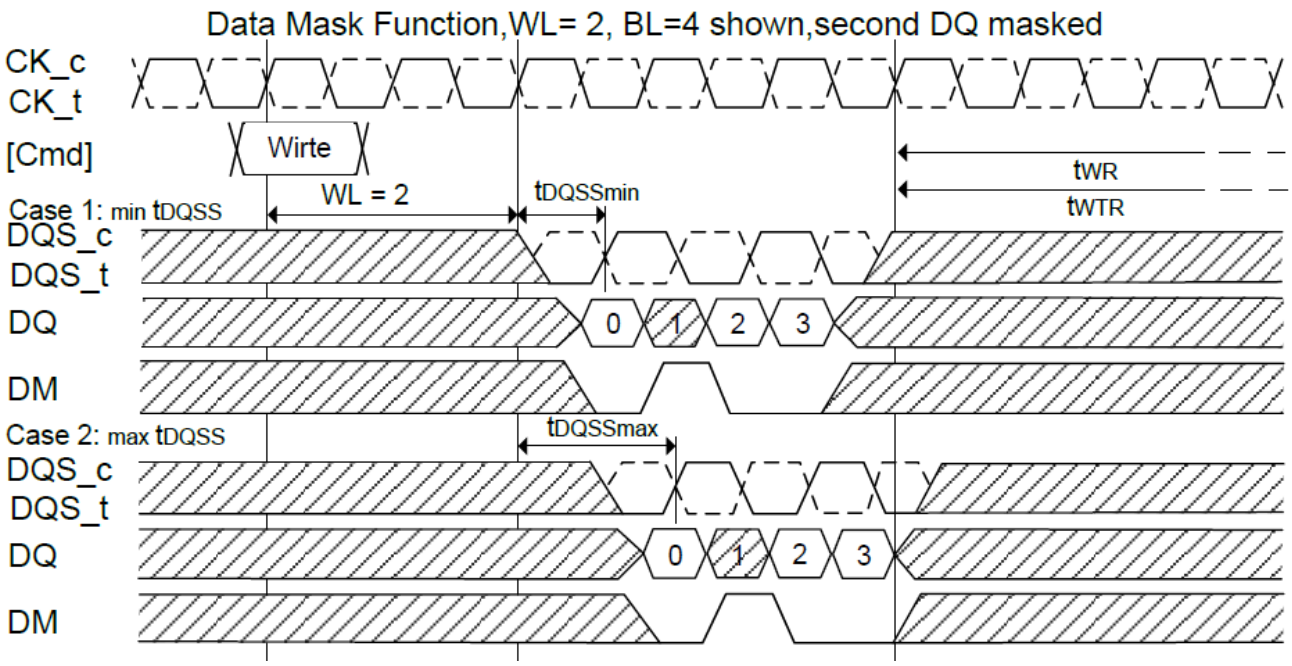
8.4.7 Write Data Mask

One write data mask (DM) pad for each data byte (DQ) will be supported on LPDDR2 devices, consistent with the implementation on LPDDR SDRAMs. Each data mask (DM) may mask its respective data byte (DQ) for any given cycle of the burst. Data mask has identical timings on write operations as the data bits, though used as input only, is internally loaded identically to data bits to insure matched system timing.

See 8.4.14.2 “Precharge & Auto Precharge Clarification” table for Write to Precharge timings.

8.4.7.1 Write Data Mask Timing





8.4.8 Precharge Operation

The Precharge command is used to precharge or close a bank that has been activated. The Precharge command is initiated by having CS_n LOW, CA0 HIGH, CA1 HIGH, CA2 LOW, and CA3 HIGH at the rising edge of the clock. The Precharge Command can be used to precharge each bank independently or all banks simultaneously. For 4-bank devices, the AB flag, and the bank address bits, BA0 and BA1 are used to determine which bank(s) to precharge. The bank(s) will be available for a subsequent row access tRPab after an All-Bank Precharge command is issued and tRPpb after a Single-Bank Precharge command is issued.

For 4-bank devices, the Row Precharge time (tRP) for an All-Bank Precharge (tRPab) is equal to the Row Precharge time for a Single-Bank Precharge (tRPpb).

8.4.8.1 Bank Selection for Precharge by Address Bits

AB(CA4r)	BA2(CA9r)	BA1(CA8r)	BA0(CA7r)	Precharged Banks
0	0	0	0	Bank0 only
0	0	0	1	Bank1 only
0	0	1	0	Bank2 only
0	0	1	1	Bank3 only
0	1	0	0	Bank4 only
0	1	0	1	Bank5 only
0	1	1	0	Bank6 only
0	1	1	1	Bank7 only
1	DON'T CARE	DON'T CARE	DON'T CARE	All Banks

8.4.9 Burst Read Operation Followed by Precharge

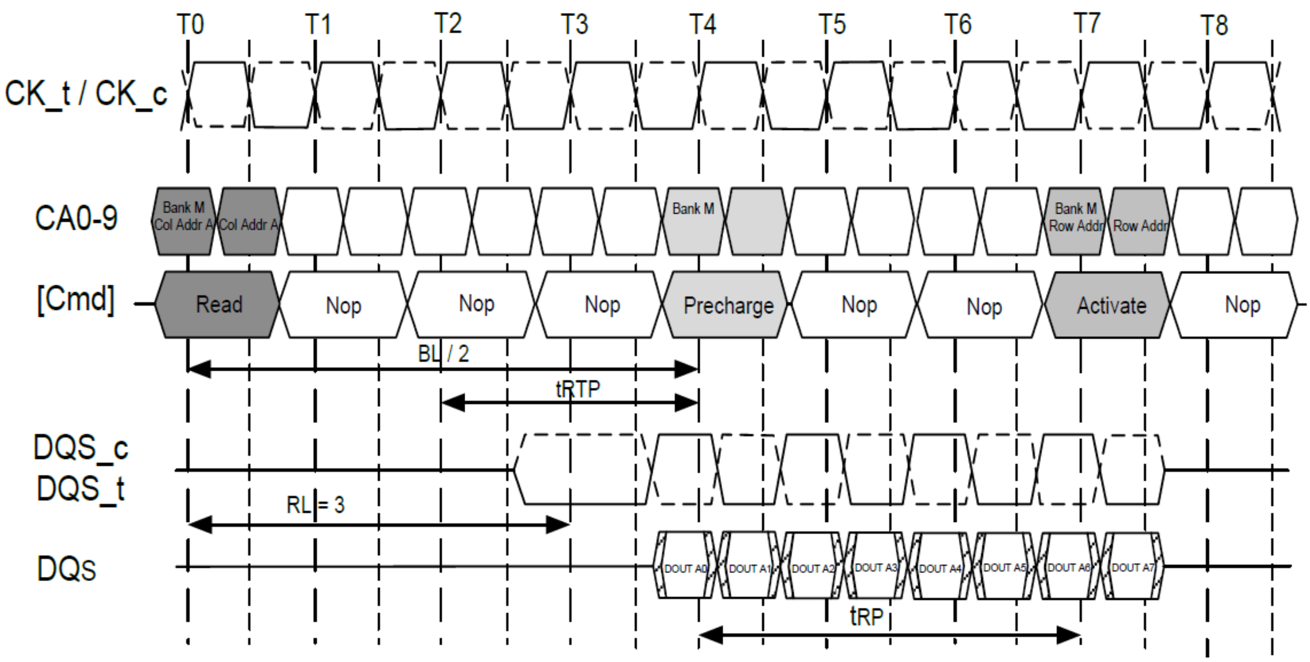
For the earliest possible precharge, the precharge command may be issued BL/2 clock cycles after a Read command. For an untruncated burst, BL is the value from the Mode Register. For a truncated burst, BL is the effective burst length. A new bank active (command) may be issued to the same bank after the Row Precharge time (tRP). A precharge command cannot be issued until after tRAS is satisfied.

For LPDDR2-S4 devices, the minimum Read to Precharge spacing has also to satisfy a minimum analog time from the rising clock edge that initiates the last 4-bit prefetch of a Read command. This time is called tRTP (Read to Precharge).

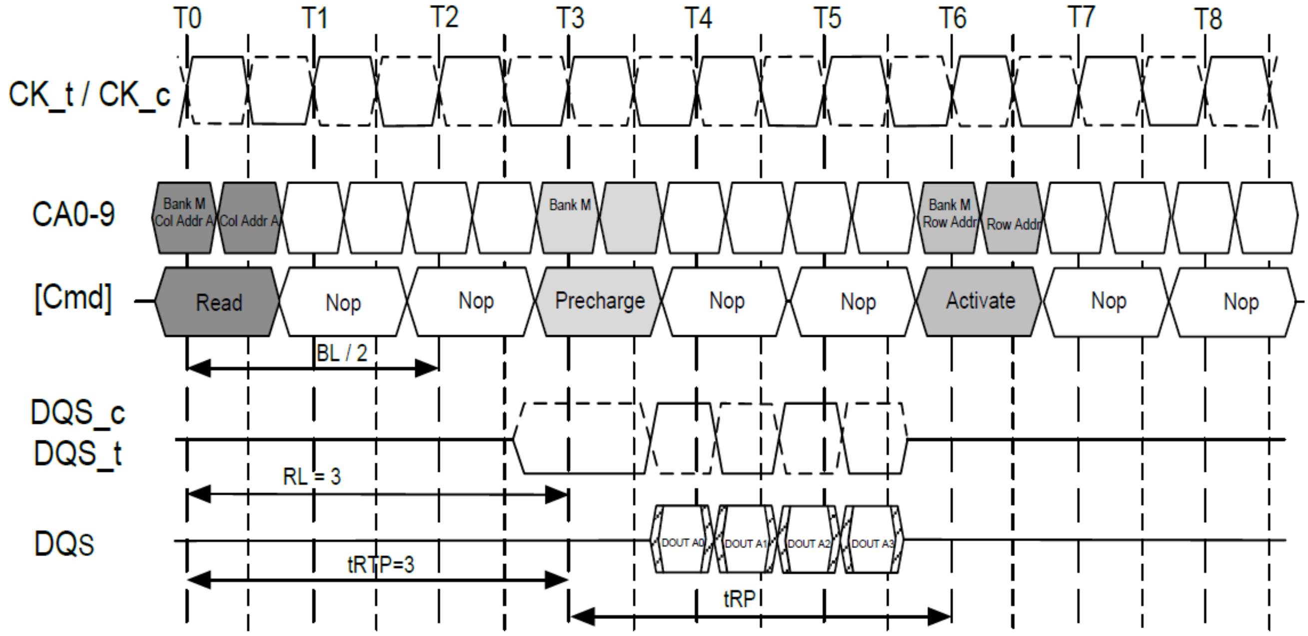
For LPDDR2-S4 devices, tRTP begins BL/2 - 2 clock cycles after the Read command. If the burst is truncated by a BST command or a Read command to a different bank, the effective "BL" shall be used to calculate when tRTP begins.

See 8.4.14.2 "Precharge & Auto Precharge Clarification" table for Read to Precharge timings.

8.4.9.1 Burst Read Followed by Precharge: RL = 3, BL = 8, RU(tRTP(min)/tCK) = 2



8.4.9.2 Burst Read Followed by Precharge: RL = 3, BL = 4, RU(tRTP(min)/tCK) = 3



8.4.10 Burst Write Followed by Precharge

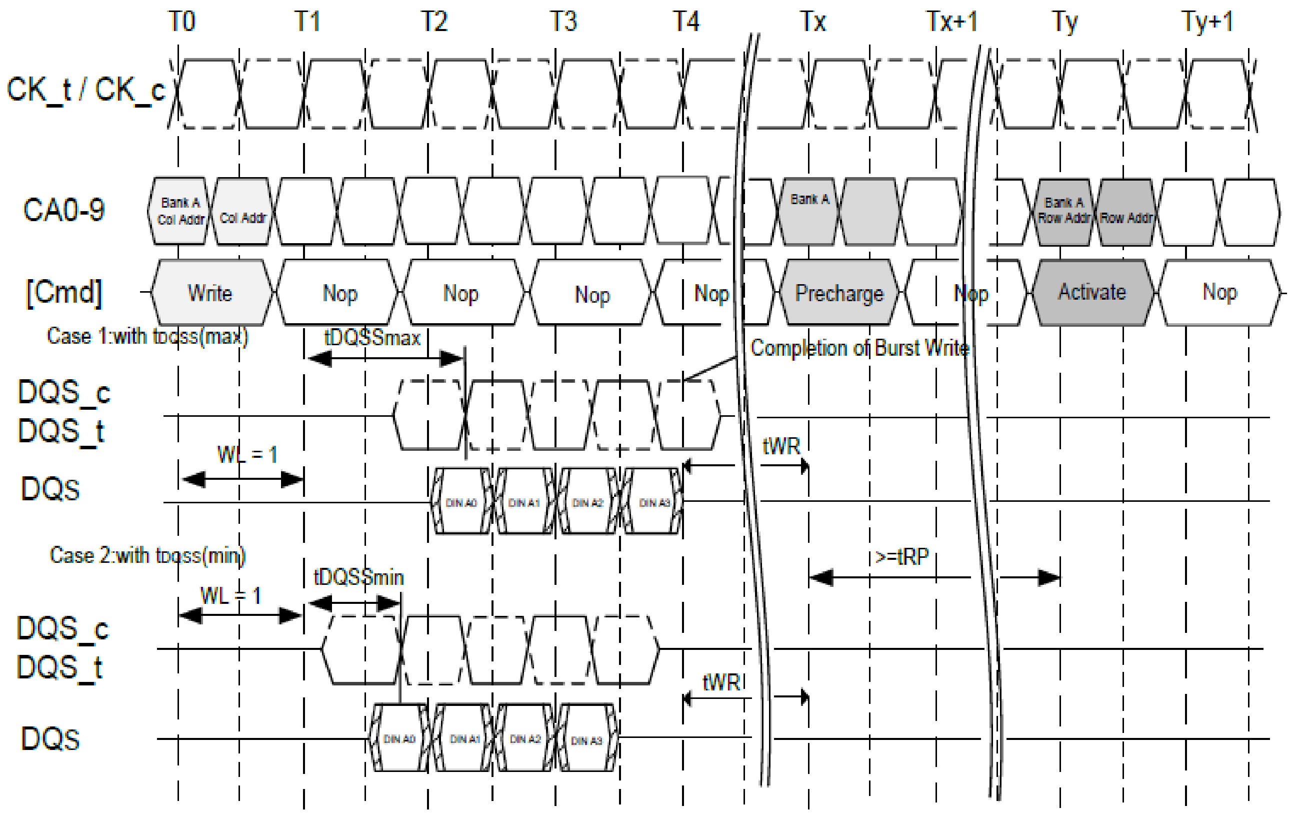
For write cycles, a delay must be satisfied from the time of the last valid burst input data until the Precharge command may be issued. This delay is known as the write recovery time (tWR) referenced from the completion of the burst write to the precharge command. No Precharge command to the same bank should be issued prior to the tWR delay.

LPDDR2-S4 devices write data to the array in prefetch quadruples (prefetch = 4). The beginning of an internal write operation may only begin after a prefetch group has been latched completely. Therefore, the write recovery time (tWR) starts at different boundaries.

The minimum Write to Precharge command spacing to the same bank is WL + BL/2 + 1 + RU(tWR/tCK) clock cycles. For an untruncated burst, BL is the value from the Mode Register. For a truncated burst, BL is the effective burst length.

See 8.4.14.2 “Precharge & Auto Precharge Clarification” table for Write to Precharge timings.

8.4.10.1 Burst Write Followed by Precharge: WL = 1, BL = 4



8.4.11 Auto Precharge Operation

Before a new row in an active bank can be opened, the active bank must be precharged using either the Precharge command or the auto-precharge function. When a Read or a Write command is given to the LPDDR2 SDRAM, the AP bit (CA0f) may be set to allow the active bank to automatically begin precharge at the earliest possible moment during the burst read or write cycle.

If AP is LOW when the Read or Write command is issued, then normal Read or Write burst operation is executed and the bank remains active at the completion of the burst.

If AP is HIGH when the Read or Write command is issued, then the auto-precharge function is engaged. This feature allows the precharge operation to be partially or completely hidden during burst read cycles (dependent upon Read or Write latency) thus improving system performance for random data access.

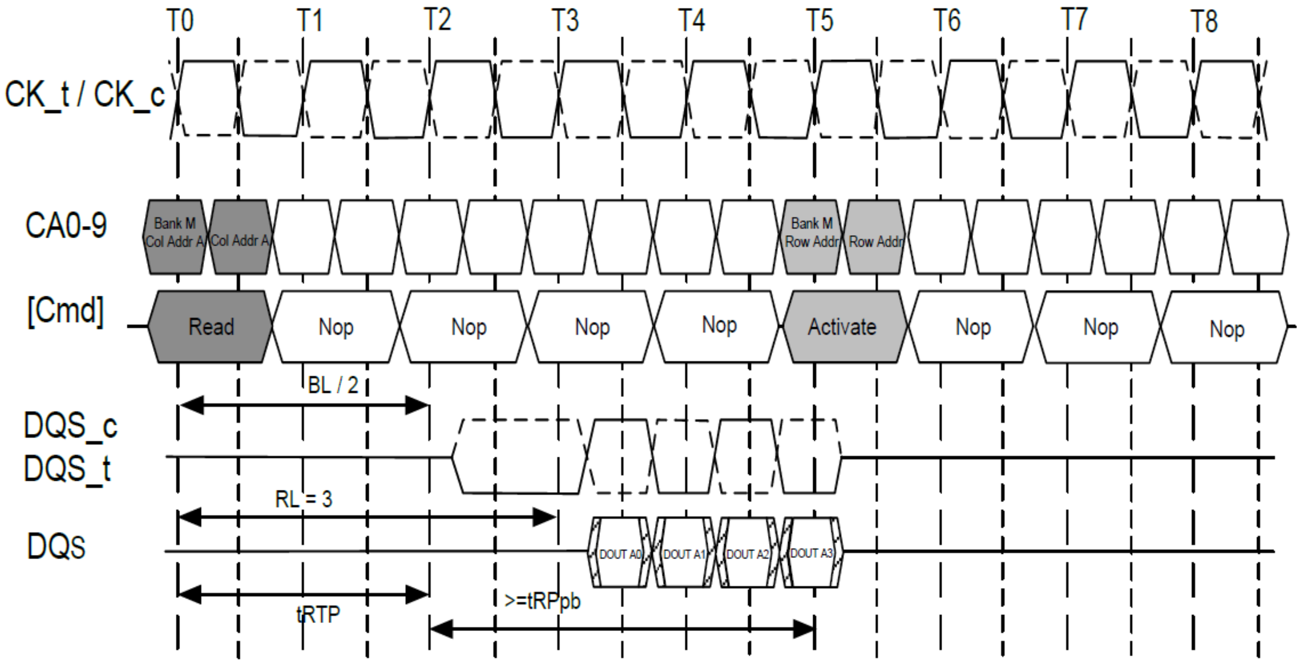
8.4.12 Burst Read with Auto-Precharge

If AP (CA0f) is HIGH when a Read Command is issued, the Read with Auto-Precharge function is engaged. LPDDR2-S4 devices start an Auto-Precharge operation on the rising edge of the clock BL/2 or BL/2 - 2 + RU(tRTP/tCK) clock cycles later than the Read with AP command, whichever is greater. Refer to section 8.4.14.2 “Precharge & Auto Precharge Clarification” table for equations related to Auto-Precharge for LPDDR2-S4.

A new bank Activate command may be issued to the same bank if both of the following two conditions are satisfied simultaneously.

- The RAS precharge time (tRP) has been satisfied from the clock at which the auto precharge begins.
- The RAS cycle time (tRC) from the previous bank activation has been satisfied.

8.4.12.1 Burst Read with Auto-Precharge: RL = 3, BL = 4, RU(tRTP(min)/tCK) = 2



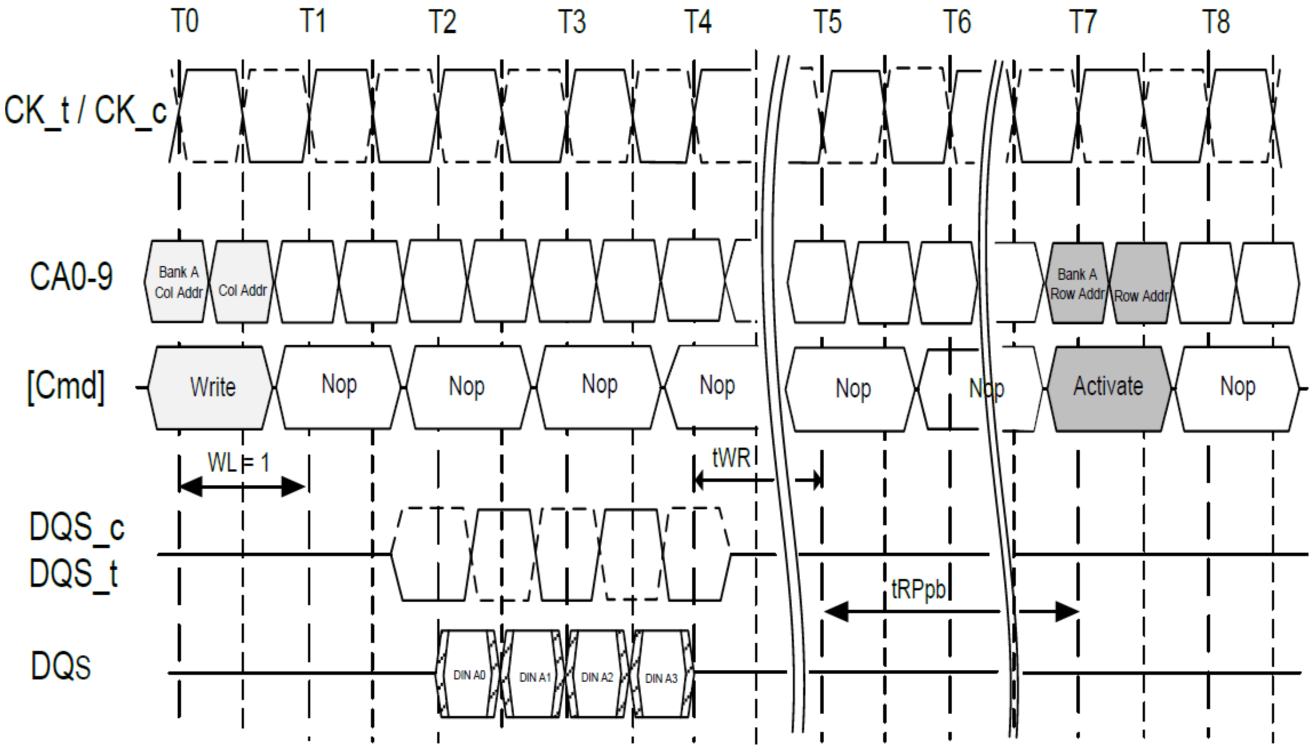
8.4.13 Burst Write with Auto-Precharge

If AP (CA0f) is HIGH when a Write Command is issued, the Write with Auto-Precharge function is engaged. The LPDDR2 SDRAM starts an Auto Precharge operation on the rising edge which is tWR cycles after the completion of the burst write.

A new bank activate (command) may be issued to the same bank if both of the following two conditions are satisfied.

- The RAS precharge time (tRP) has been satisfied from the clock at which the auto precharge begins.
- The RAS cycle time (tRC) from the previous bank activation has been satisfied.

8.4.13.1 Burst Write with Auto Precharge: WL = 1, BL = 4



8.4.13.2 Precharge & Auto Precharge Clarification

From Command	To Command	Minimum Delay between "From Command" to "To Command"	Unit	Notes
Read	Precharge (to same Bank as Read)	BL/2 + max(2, RU(tRTP/tCK)) - 2	CLK	1
	Precharge All	BL/2 + max(2, RU(tRTP/tCK)) - 2	CLK	1
BST (for Reads)	Precharge (to same Bank as Read)	1	CLK	1
	Precharge All	1	CLK	1
Read w/AP	Precharge (to same Bank as Read w/AP)	BL/2 + max(2, RU(tRTP/tCK)) - 2	CLK	1,2
	Precharge All	BL/2 + max(2, RU(tRTP/tCK)) - 2	CLK	1
	Activate (to same Bank as Read w/AP)	BL/2 + max(2, RU(tRTP/tCK)) - 2 + RU(tRPpb/tCK)	CLK	1
	Write or Write w/AP (same bank)	illegal	CLK	3
	Write or Write w/AP (different bank)	RL + BL/2 + RU(tDQSCKmax/tCK) - WL + 1	CLK	3
	Read or Read w/AP (same bank)	illegal	CLK	3
	Read or Read w/AP (different bank)	BL/2	CLK	3
Write	Precharge (to same Bank as Write)	WL + BL/2 + RU(tWR/tCK) + 1	CLK	1
	Precharge All	WL + BL/2 + RU(tWR/tCK) + 1	CLK	1
BST (for Writes)	Precharge (to same Bank as Write)	WL + RU(tWR/tCK) + 1	CLK	1
	Precharge All	WL + RU(tWR/tCK) + 1	CLK	1
Write w/AP	Precharge (to same Bank as Write w/AP)	WL + BL/2+ RU(tWR/tCK) + 1	CLK	1
	Precharge All	WL + BL/2+ RU(tWR/tCK) + 1	CLK	1
	Activate (to same Bank as Write w/AP)	WL + BL/2 + RU(tWR/tCK) + 1 + RU(tRPpb/tCK)	CLK	1
	Write or Write w/AP (same bank)	illegal	CLK	3
	Write or Write w/AP (different bank)	BL/2	CLK	3
	Read or Read w/AP (same bank)	illegal	CLK	3
	Read or Read w/AP (different bank)	WL + BL/2 + RU(tWTR/tCK) + 1	CLK	3
Precharge	Precharge (to same Bank as Precharge)	1	CLK	1
	Precharge All	1	CLK	1
Precharge All	Precharge	1	CLK	1
	Precharge All	1	CLK	1

Notes:
1. For a given bank, the precharge period should be counted from the latest precharge command, either one bank precharge or precharge all, issued to that bank. The precharge period is satisfied after tRP depending on the latest precharge command issued to that bank.
2. Any command issued during the specified minimum delay time is illegal.
3. After Read with AP, seamless read operations to different banks are supported. After Write with AP, seamless write operations to different banks are supported. Read w/AP and Write w/AP may not be interrupted or truncated.

8.4.14 Refresh Command

The Refresh command is initiated by having CS_n LOW, CA0 LOW, CA1 LOW, and CA2 HIGH at the rising edge of clock. All Bank Refresh is initiated by having CA3 HIGH at the rising edge of clock.

An All Bank Refresh command, REFab performs a refresh operation to all banks. All banks have to be in Idle state when REFab is issued (for instance, by Precharge all-bank command). REFab also synchronizes the bank count between the controller and the SDRAM to zero.

As shown in 8.4.15.1 "Command Scheduling Separations Related to Refresh" table, the REFab command may not be issued to the memory until the following conditions have been met:
a) The tRFCab has been satisfied after the prior REFab command
b) The tRP has been satisfied after prior Precharge commands

When the All Bank refresh cycle has completed, all banks will be in the Idle state.

As shown in 8.4.15.1 "Command Scheduling Separations Related to Refresh" table, after issuing REFab:
a) The tRFCab latency must be satisfied before issuing an ACTIVATE command
b) The tRFCab latency must be satisfied before issuing a REFab command

8.4.14.1 Command Scheduling Separations Related to Refresh

Symbol	minimum delay from	to
tRFCab	REFab	REFab
		Activate cmd to any bank
tRRD	Activate	Activate cmd to different bank than prior Activate
Note: A bank must be in the Idle state before it is refreshed.		

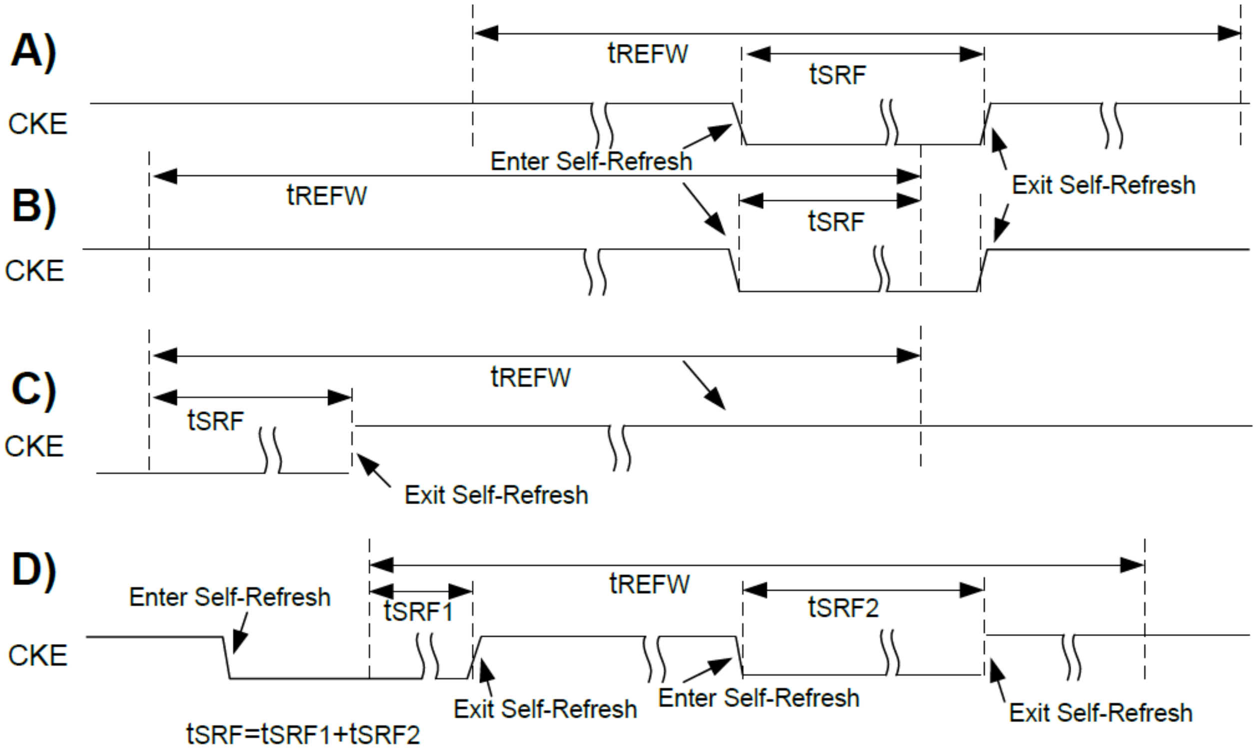
8.4.15 LPDDR2 SDRAM Refresh Requirements

(1) Minimum number of Refresh commands:
The LPDDR2 SDRAM requires a minimum number of R Refresh (REFab) commands within any rolling Refresh Window (tREFW = 32 mS @ MR4[2:0] = "011" or Tj ≤ 85°C). The required minimum number of Refresh commands and resulting average refresh interval (tREFI) are given in 9.6.1 "Refresh Requirement Parameters" table. See Mode Register 4 for tREFW and tREFI refresh multipliers at different MR4 settings.

(2) Burst Refresh limitation:
To limit maximum current consumption, a maximum of 8 REFab commands may be issued in any rolling tREFBW (tREFBW = 4 x 8 x tRFCab).

(3) Refresh Requirements and Self-Refresh:
If any time within a refresh window is spent in Self-Refresh Mode, the number of required Refresh commands in this particular window is reduced to:
R* = R - RU{tSRF / tREFI} = R - RU{R * tSRF / tREFW}; where RU stands for the round-up function.

8.4.15.1 Definition of tSRF



Several examples on how tSRF is calculated:
A: with the time spent in Self-Refresh Mode fully enclosed in the Refresh Window (tREFW).
B: at Self-Refresh entry.
C: at Self-Refresh exit.
D: with several different intervals spent in Self Refresh during one tREFW interval.

In contrast to JESD79 and JESD79-2 and JESD79-3 compliant SDRAM devices, LPDDR2-S4 devices allow significant flexibility in scheduling REFRESH commands, as long as the boundary conditions above are met. In the most straight forward case a REFRESH command should be scheduled every tREFI. In this case Self-Refresh may be entered at any time.

The users may choose to deviate from this regular refresh pattern e.g., to enable a period where no refreshes are required. As an example, using a 1Gb LPDDR2-S4 device, the user can choose to issue a refresh burst of 4096 REFRESH commands with the maximum allowable rate (limited by tREFBW) followed by a long time without any REFRESH commands, until the refresh window is complete, then repeating this sequence. The achievable time without REFRESH commands is given by tREFW - (R / 8) * tREFBW = tREFW - R * 4 * tRFCab.@ Tj ≤ 85°C this can be up to 32 mS - 4096 * 4 * 130 nS ≈ 30 mS.

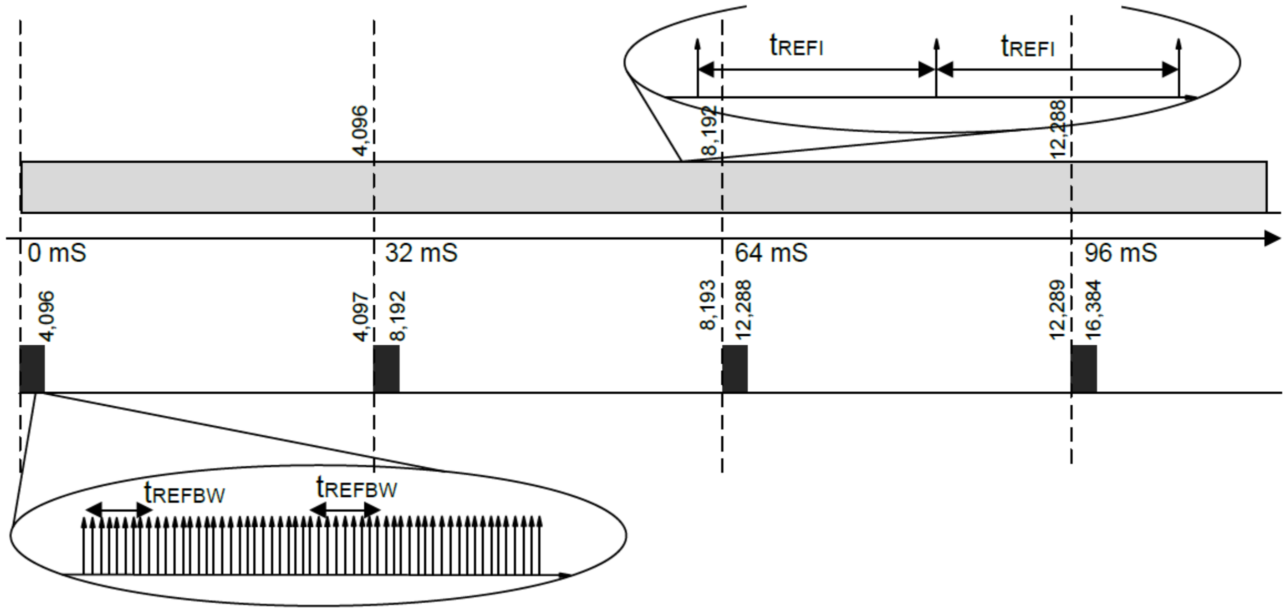
While both - the regular and the burst/pause - patterns can satisfy the refresh requirements per rolling refresh interval, if they are repeated in every subsequent 32 mS window, extreme care must be taken when transitioning from one pattern to another to satisfy the refresh requirement in every rolling refresh window during the transition.

Figure of 8.4.16.3 shows an example of an allowable transition from a burst pattern to a regular, distributed pattern. If this transition happens directly after the burst refresh phase, all rolling tREFW interval will have at least the required number of refreshes.

Figure of 8.4.16.4 shows an example of a non-allowable transition. In this case the regular refresh pattern starts after the completion of the pause-phase of the burst/pause refresh pattern. For several rolling tREFW intervals the minimum number of REFRESH commands is not satisfied.

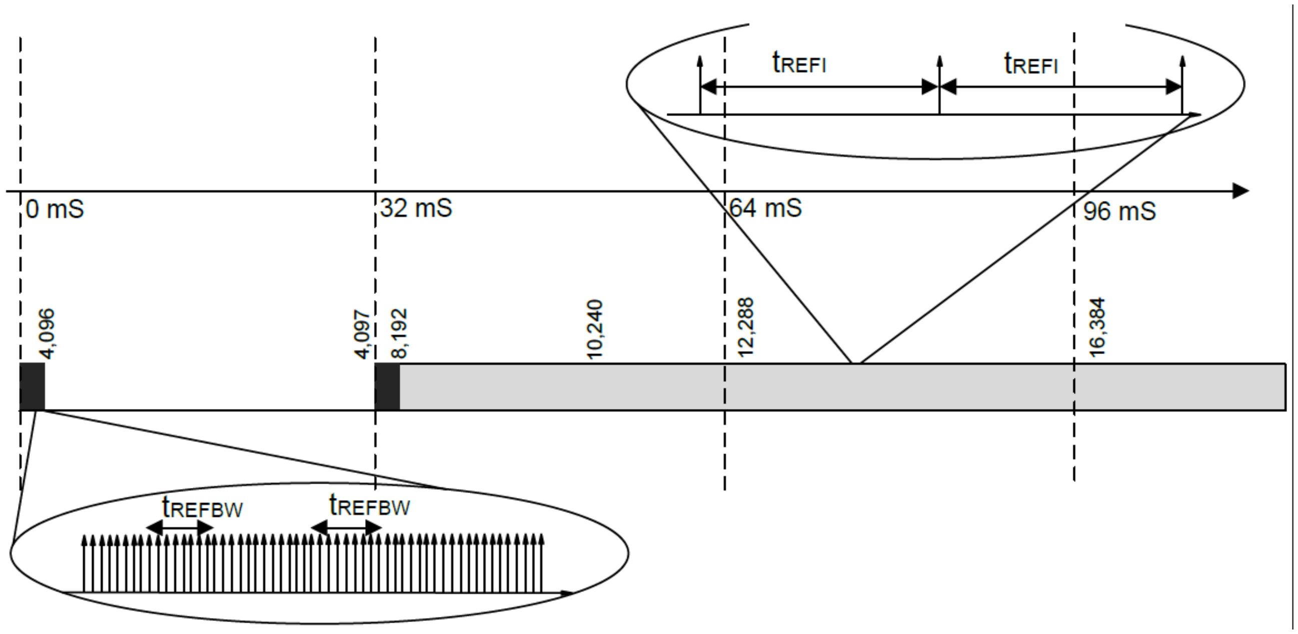
The understanding of the pattern transition is extremely relevant (even if in normal operation only one pattern is employed), as in Self-Refresh-Mode a regular, distributed refresh pattern has to be assumed, which is reflected in the equation for R* above. Therefore it is recommended to enter Self-Refresh-Mode ONLY directly after the burst-phase of a burst/pause refresh pattern as indicated in figure of 8.4.16.5 and begin with the burst phase upon exit from Self-Refresh.

8.4.15.2 Regular, Distributed Refresh Pattern



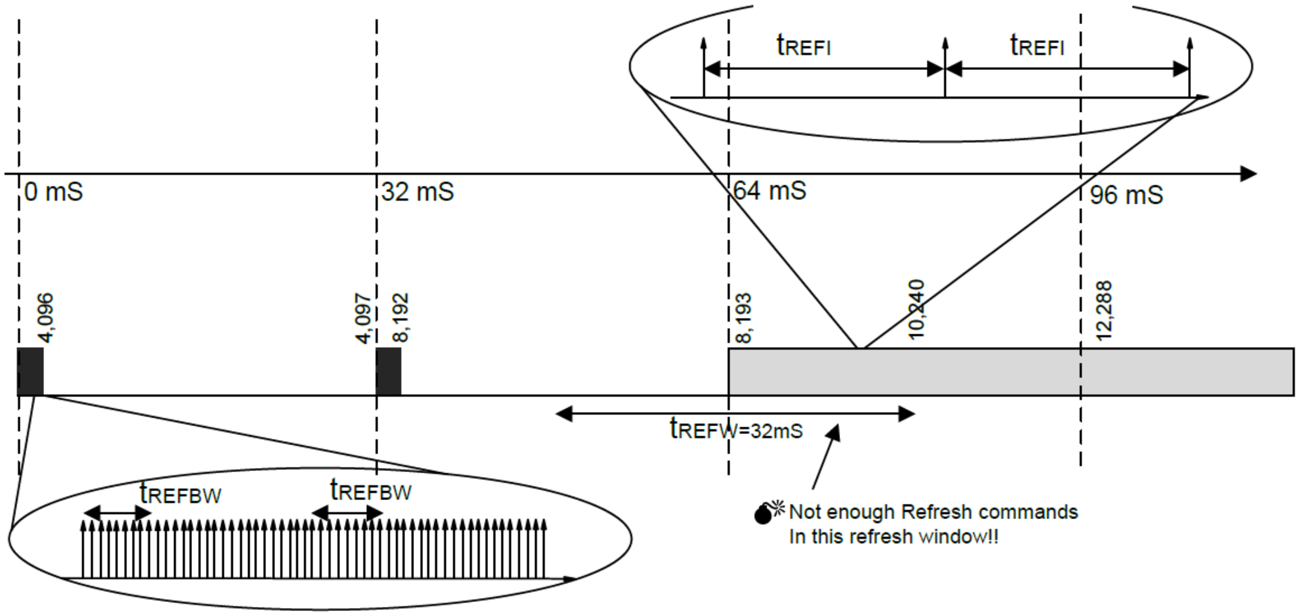
Notes:
1. Compared to repetitive burst Refresh with subsequent Refresh pause.
2. For an example, in a 1Gb LPDDR2 device at Tj ≤ 85°C, the distributed refresh pattern would have one REFRESH command per 7.8 µS; the burst refresh pattern would have an average of one refresh command per 0.52 µS followed by ≈30 mS without any REFRESH command.

8.4.15.3 Allowable Transition from Repetitive Burst Refresh



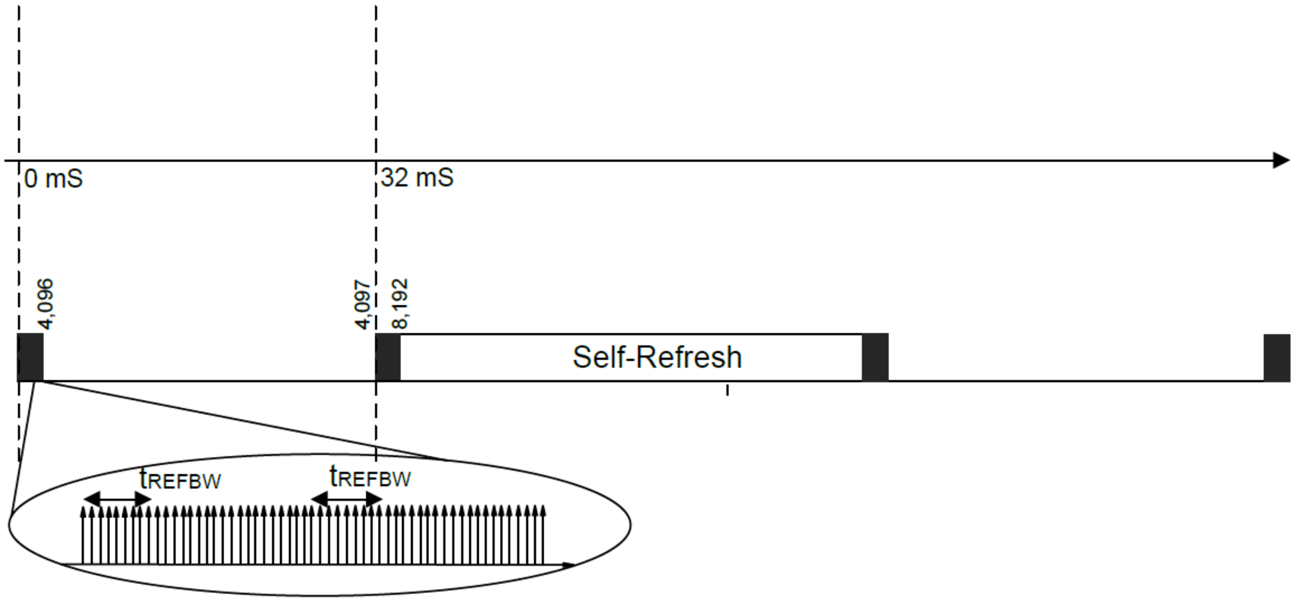
Notes:
1. Shown with subsequent Refresh pause to regular distributed Refresh pattern.
2. For an example, in a 1Gb LPDDR2 device at Tj ≤ 85°C, the distributed refresh pattern would have one REFRESH command per 7.8 µS; the burst refresh pattern would have an average of one refresh command per 0.52 µS followed by ≈30 mS without any REFRESH command.

8.4.15.4 NOT-Allowable Transition from Repetitive Burst Refresh



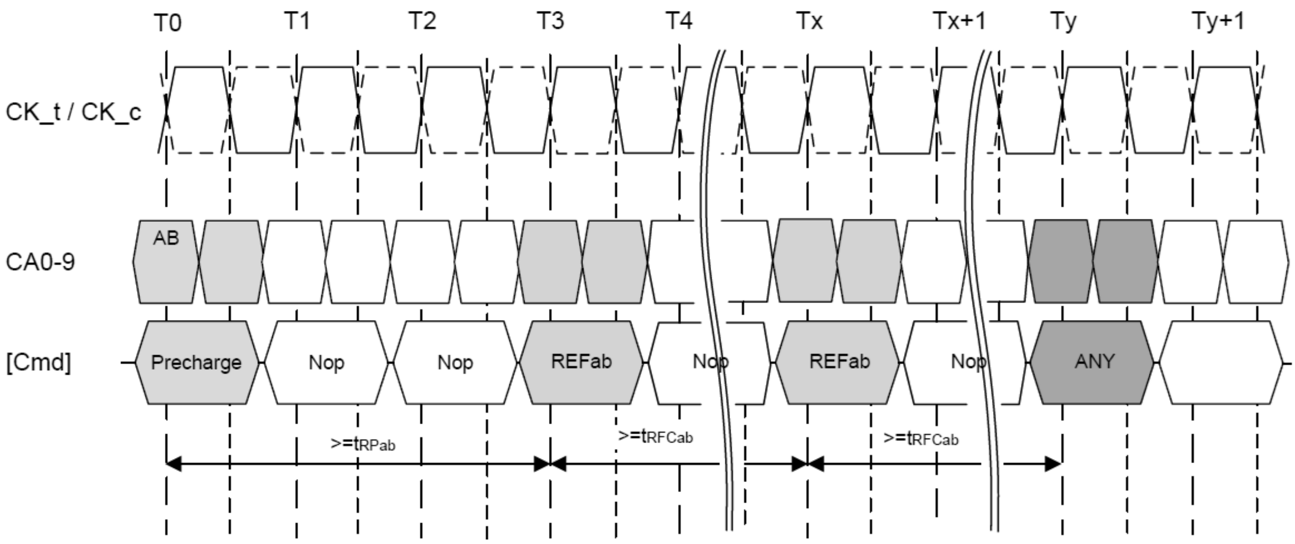
Notes:
1. Shown with subsequent Refresh pause to regular distributed Refresh pattern.
2. Only ≈2048 REFRESH commands (< R which is 4096) in the indicated tREFW window.

8.4.15.5 Recommended Self-Refresh Entry and Exit



Note:
1. In conjunction with a Burst/Pause Refresh patterns.

8.4.15.6 All Bank Refresh Operation



8.4.16 Self Refresh Operation

The Self Refresh command can be used to retain data in the LPDDR2 SDRAM, even if the rest of the system is powered down. When in the Self Refresh mode, the LPDDR2 SDRAM retains data without external clocking. The LPDDR2 SDRAM device has a built-in timer to accommodate Self Refresh operation. The Self Refresh Command is defined by having CKE LOW, CS_n LOW, CA0 LOW, CA1 LOW, and CA2 HIGH at the rising edge of the clock. CKE must be HIGH during the previous clock cycle. A NOP command must be driven in the clock cycle following the power-down command. Once the command is registered, CKE must be held LOW to keep the device in Self Refresh mode.

LPDDR2-S4 devices can operate in Self Refresh in both the Standard or Extended Temperature Ranges. LPDDR2-S4 devices will also manage Self Refresh power consumption when the operating temperature changes, lower at low temperatures and higher temperatures.

Once the LPDDR2 SDRAM has entered Self Refresh mode, all of the external signals except CKE, are “don’t care”. For proper self refresh operation, power supply pads (VDD1, VDD2, and VDD2) must be at valid levels. VDDQ may be turned off during Self-Refresh. Prior to exiting Self-Refresh, VDDQ must be within specified limits. VrefDQ and VrefCA may be at any level within minimum and maximum levels (see section 9.1 “Absolute Maximum DC Ratings” table). However prior to exit Self-Refresh, VrefDQ and VrefCA must be within specified limits (see section 9.2.1.1 “Recommended DC Operating Conditions” table). The SDRAM initiates a minimum of one all-bank refresh command internally within tCKESR period once it enters Self Refresh mode. The clock is internally disabled during Self Refresh Operation to save power. The minimum time that the LPDDR2 SDRAM must remain in Self Refresh mode is tCKESR. The user may change the external clock frequency or halt the external clock one clock after Self Refresh entry is registered; however, the clock must be restarted and stable before the device can exit Self Refresh operation.

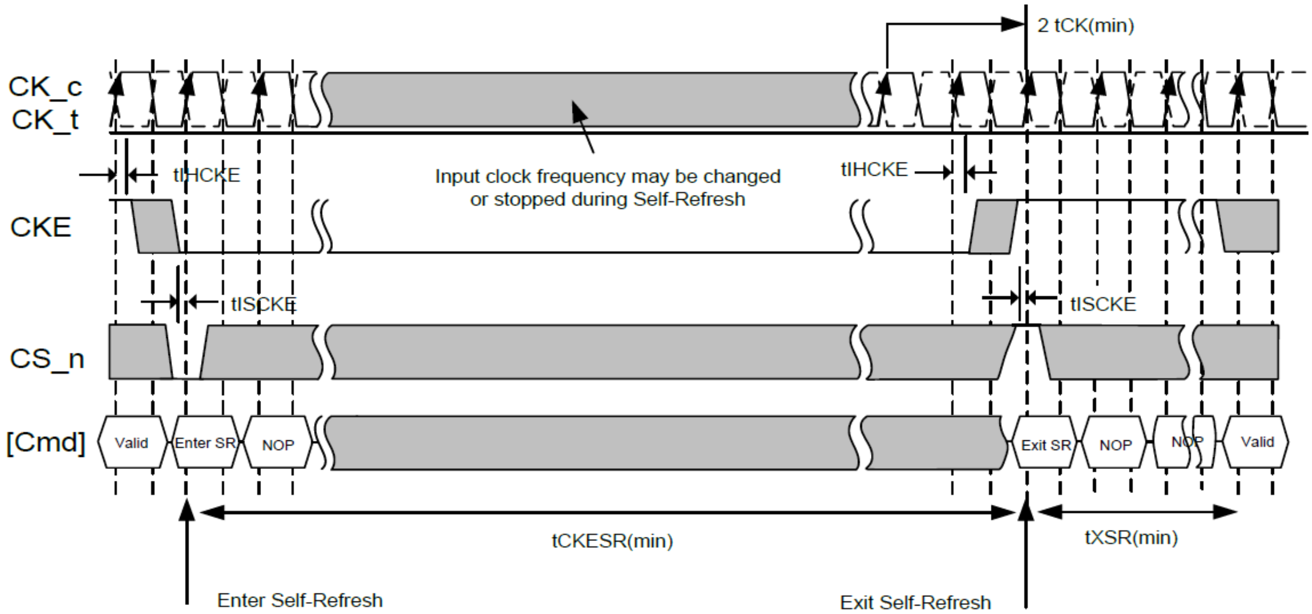
The procedure for exiting Self Refresh requires a sequence of commands. First, the clock shall be stable and within specified limits for a minimum of 2 clock cycles prior to CKE going back HIGH. Once Self Refresh Exit is registered, a delay of at least tXSR must be satisfied before a valid command can be issued to the device to allow for any internal refresh in progress. CKE must remain HIGH for the entire Self Refresh exit period tXSR for proper operation except for self refresh re-entry. NOP commands must be registered on each positive clock edge during the Self Refresh exit interval tXSR.

The use of Self Refresh mode introduces the possibility that an internally timed refresh event can be missed when

CKE is raised for exit from Self Refresh mode. Upon exit from Self Refresh, it is required that at least one Refresh command (one all-bank) is issued before entry into a subsequent Self Refresh.

For LPDDR2 SDRAM, the maximum duration in power-down mode is only limited by the refresh requirements outlined in section 8.4.16 “LPDDR2 SDRAM Refresh Requirements”, since no refresh operations are performed in power-down mode.

8.4.16.1 Figure of Self Refresh Operation



Notes:
1. Input clock frequency may be changed or stopped during self-refresh, provided that upon exiting self-refresh, a minimum of 2 clocks of stable clock are provided and the clock frequency is between the minimum and maximum frequency for the particular speed grad
2. Device must be in the “All banks idle” state prior to entering Self Refresh mode.
3. tXSR begins at the rising edge of the clock after CKE is driven HIGH.
4. A valid command may be issued only after tXSR is satisfied. NOPs shall be issued during tXSR.

8.4.17 Partial Array Self-Refresh: Bank Masking

Each bank of LPDDR2 SDRAM can be independently configured whether a self refresh operation is taking place. One mode register unit of 4 bits accessible via MRW command is assigned to program the bank masking status of each bank up to 4 banks. For bank masking bit assignments, see section 8.3.13 Mode Register 16 “MR16_PASR_Bank Mask (MA[7:0] = 10H)”.

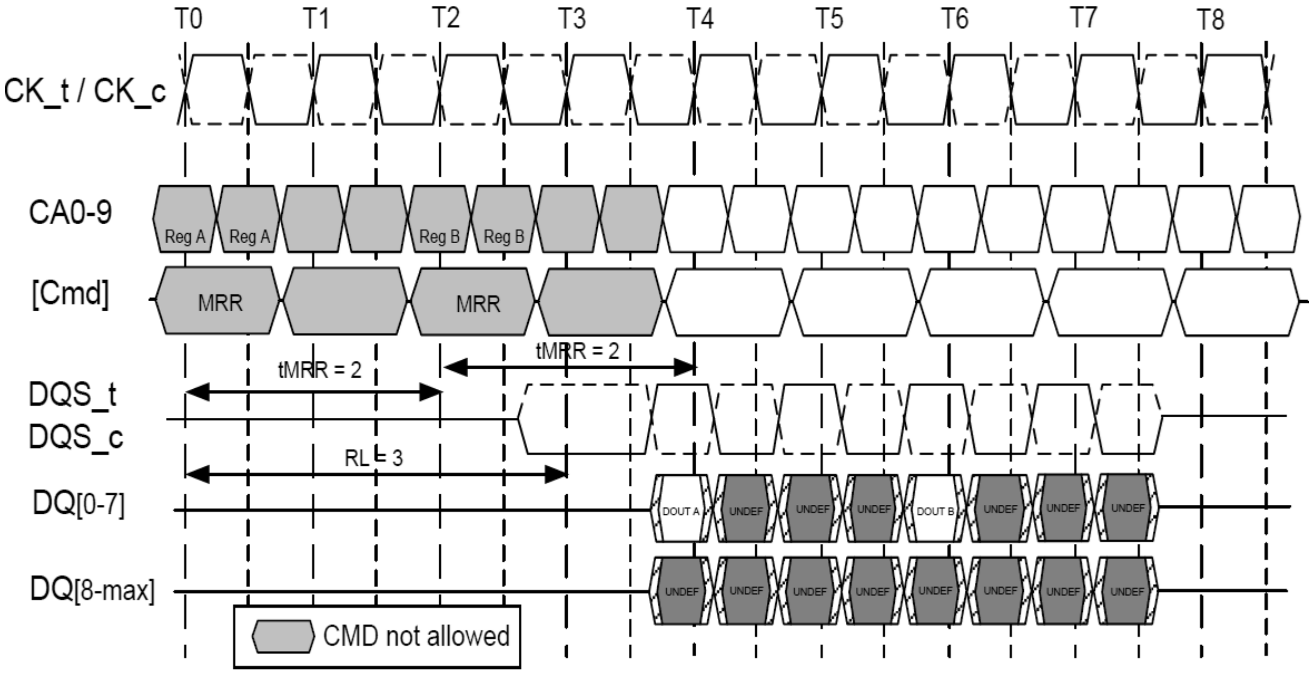
The mask bit to the bank controls a refresh operation of entire memory within the bank. If a bank is masked via MRW, a refresh operation to the entire bank is blocked and data retention by a bank is not guaranteed in self refresh mode. To enable a refresh operation to a bank, a coupled mask bit has to be programmed, “unmasked”. When a bank mask bit is unmasked, a refresh to a bank is determined by the programmed status of segment mask bits.

8.4.18 Mode Register Read Command

The Mode Register Read command is used to read configuration and status data from mode registers. The Mode Register Read (MRR) command is initiated by having CS_n LOW, CA0 LOW, CA1 LOW, CA2 LOW, and CA3 HIGH at the rising edge of the clock. The mode register is selected by {CA1f-CA0f, CA9r- CA4r}. The mode register contents are available on the first data beat of DQ[0:7], RL * tCK + tDQSCK + tDQSQ after the rising edge of the clock where the Mode Register Read Command is issued. Subsequent data beats contain valid, but undefined content, except in the case of the DQ Calibration function DQC, where subsequent data beats contain valid content as described in section 8.4.20.2 “DQ Calibration”. All DQS_t, DQS_c shall be toggled for the duration of the Mode Register Read burst.

The MRR command has a burst length of four. The Mode Register Read operation (consisting of the MRR command and the corresponding data traffic) shall not be interrupted. The MRR command period (tMRR) is 2 clock cycles. Mode Register Reads to reserved and write-only registers shall return valid, but undefined content on all data beats and DQS_t, DQS_c shall be toggled.

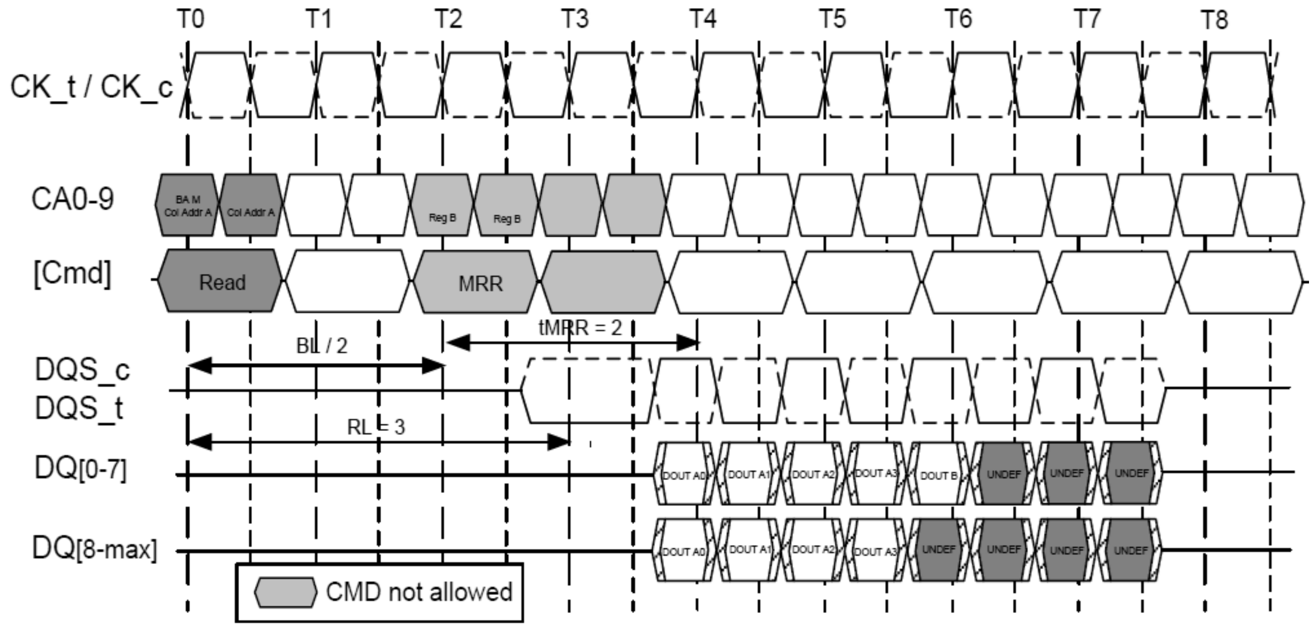
8.4.18.1 Mode Register Read Timing Example: RL = 3, tMRR = 2



Notes:
1. Mode Register Read has a burst length of four.
2. Mode Register Read operation shall not be interrupted.
3. Mode Register data is valid only on DQ[0-7] on the first beat. Subsequent beats contain valid, but undefined data. DQ[8-max] contain valid, but undefined data for the duration of the MRR burst.
4. The Mode Register Command period is tMRR. No command (other than Nop) is allowed during this period.
5. Mode Register Reads to DQ Calibration registers MR32 and MR40 are described in the section on DQ Calibration.
6. Minimum Mode Register Read to write latency is RL + RU(tDQSCKmax/tCK) + 4/2 + 1 - WL clock cycles.
7. Minimum Mode Register Read to Mode Register Write latency is RL + RU(tDQSCKmax/tCK) + 4/2 + 1 clock cycles.

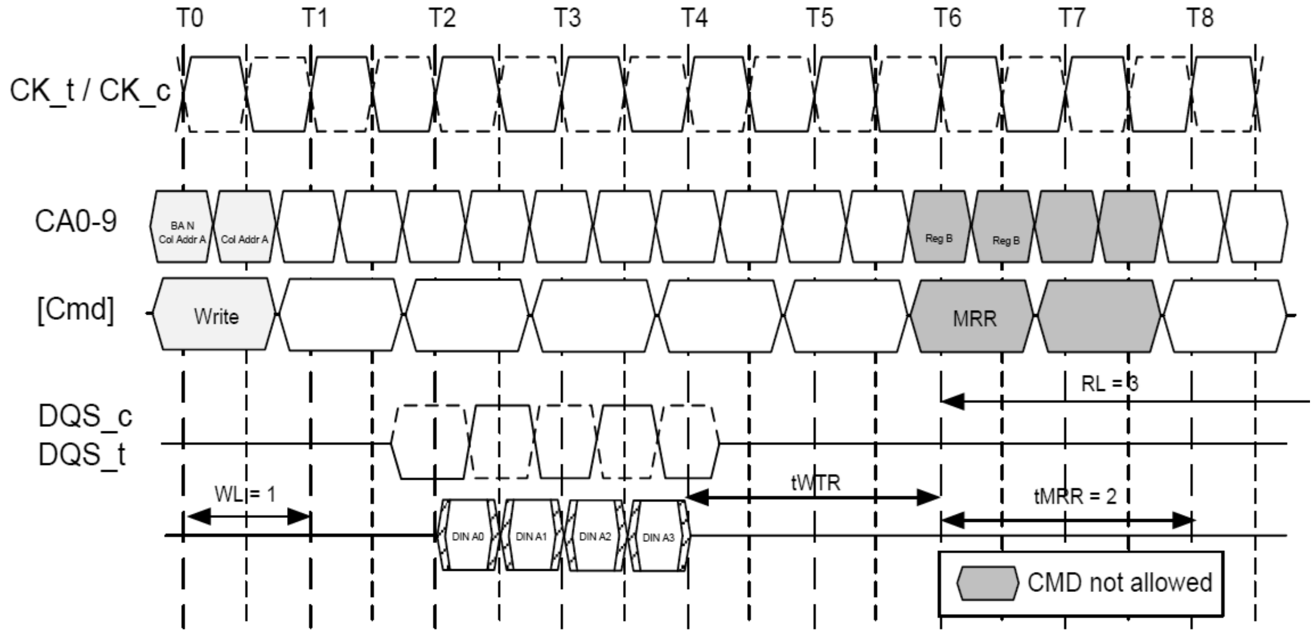
The MRR command shall not be issued earlier than BL/2 clock cycles after a prior Read command and WL + 1 + BL/2 + RU(tWTR/tCK) clock cycles after a prior Write command, because read-bursts and write-bursts shall not be truncated by MRR. Note that if a read or write burst is truncated with a Burst Terminate (BST) command, the effective burst length of the truncated burst should be used as “BL”.

8.4.18.2 Read to MRR Timing Example: RL = 3, tMRR = 2



Notes:
1. The minimum number of clocks from the burst read command to the Mode Register Read command is BL/2.
2. The Mode Register Read Command period is tMRR. No command (other than Nop) is allowed during this period.

8.4.18.3 Burst Write Followed by MRR: RL = 3, WL = 1, BL = 4



Notes:
1. The minimum number of clock cycles from the burst write command to the Mode Register Read command is [WL + 1 + BL/2 + RU(tWTR/tCK)].
2. The Mode Register Read Command period is tMRR. No command (other than Nop) is allowed during this period.

8.4.19 Temperature Sensor

LPDDR2 SDRAM features a temperature sensor whose status can be read from MR4. This sensor can be used to determine an appropriate refresh rate, determine whether AC timing derating is required in the Extended Temperature Range and/or monitor the operating temperature. Either the temperature sensor or the device operating temperature (See 9.2.3 “Operating Temperature Conditions” table) may be used to determine whether operating temperature requirements are being met.

LPDDR2 devices shall monitor device temperature and update MR4 according to tTSI. Upon exiting self-refresh or power-down, the device temperature status bits shall be no older than tTSI.

When using the temperature sensor, the actual device junction temperature may be higher than the operating temperature specification (See 9.2.3 “Operating Temperature Conditions” table) that applies for the Standard or Extended Temperature Ranges. For example, Tj may be above 85°C when MR4[2:0] equals 011b.

To assure proper operation using the temperature sensor, applications should consider the following factors:
TempGradient is the maximum temperature gradient experienced by the memory device at the temperature of interest over a range of 2°C.

ReadInterval is the time period between MR4 reads from the system.

TempSensorInterval (tTSI) is maximum delay between internal updates of MR4.

SysRespDelay is the maximum time between a read of MR4 and the response by the system.

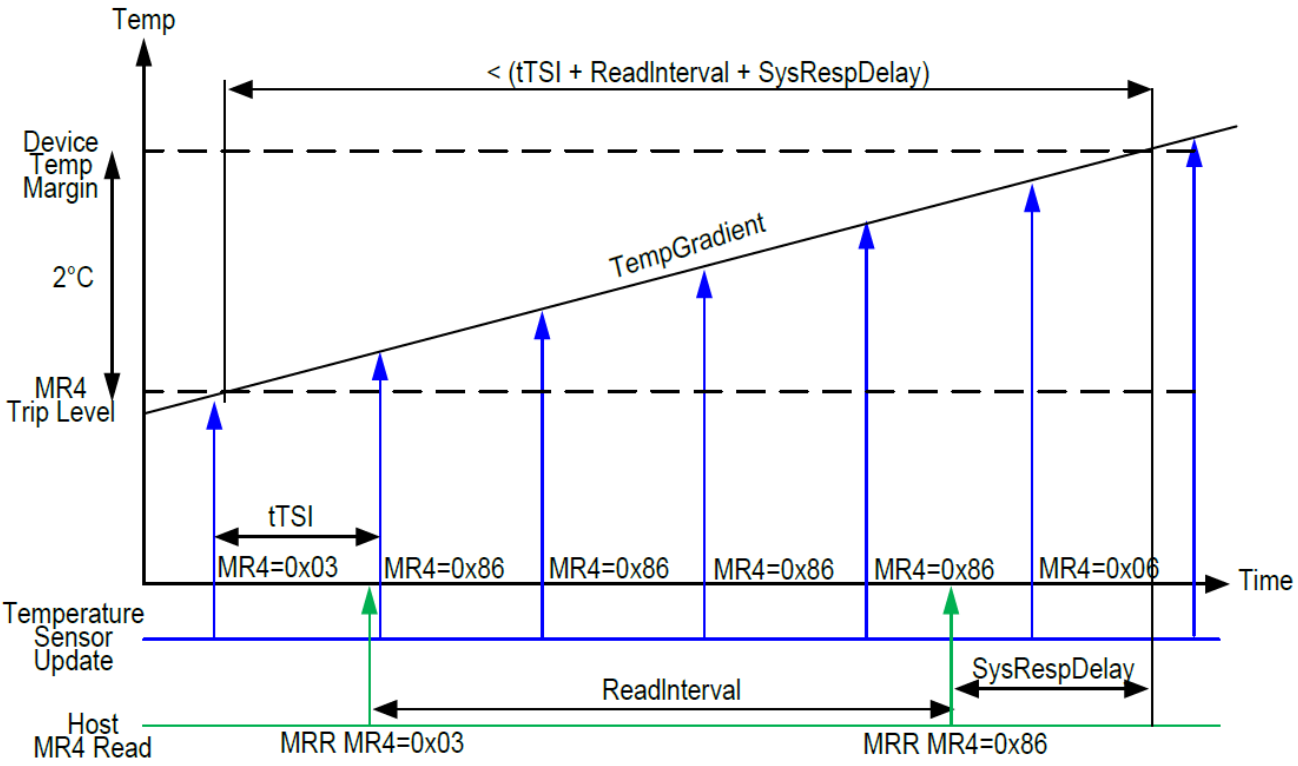
LPDDR2 devices shall allow for a 2°C temperature margin between the point at which the device temperature enters the Extended Temperature Range and point at which the controller re-configures the system accordingly.

In order to determine the required frequency of polling MR4, the system shall use the maximum TempGradient and the maximum response time of the system using the following equation:

$$\text{TempGradient} \times (\text{ReadInterval} + \text{tTSI} + \text{SysRespDelay}) \leq 2°\text{C}$$

In this case, ReadInterval shall be no greater than 167 mS.

8.4.19.1 Temperature Sensor Timing



8.4.19.2 DQ Calibration

LPDDR2 device features a DQ Calibration function that outputs one of two predefined system timing calibration patterns. A Mode Register Read to MR32 (Pattern “A”) or MR40 (Pattern “B”) will return the specified pattern on DQ[0] and DQ[8] for x16 devices, and DQ[0] , DQ[8] , DQ[16] , and DQ[24] for x32 devices.

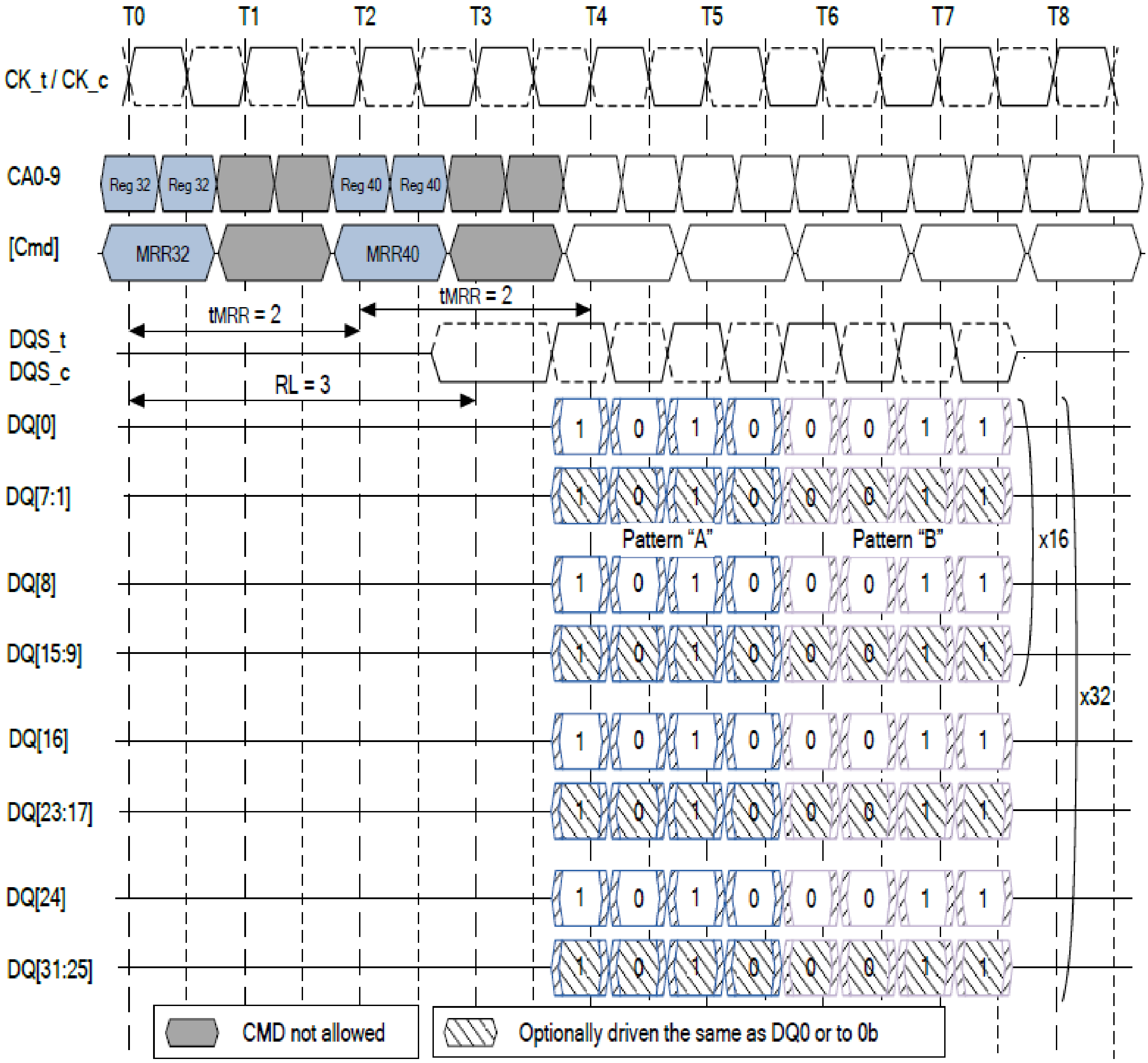
For x16 devices, DQ[7:1] and DQ[15:9] may optionally drive the same information as DQ[0] or may drive 0b during the MRR burst. For x32 devices, DQ[7:1], DQ[15:9], DQ[23:17], and DQ[31:25] may optionally drive the same information as DQ[0] or may drive 0b during the MRR burst.

For LPDDR2-S4 devices, MRR DQ Calibration commands may only occur in the Idle state.

Table 5: Data Calibration Pattern Description

Pattern	MR#	Bit Time 0	Bit Time 1	Bit Time 2	Bit Time 3	Description
Pattern A	MR32	1	0	1	0	Read to MR32 return DQ calibration pattern A
Pattern B	MR40	0	0	1	1	Read to MR40 return DQ calibration pattern B

8.4.19.3 MR32 and MR40 DQ Calibration Timing Example: RL = 3, tMRR = 2



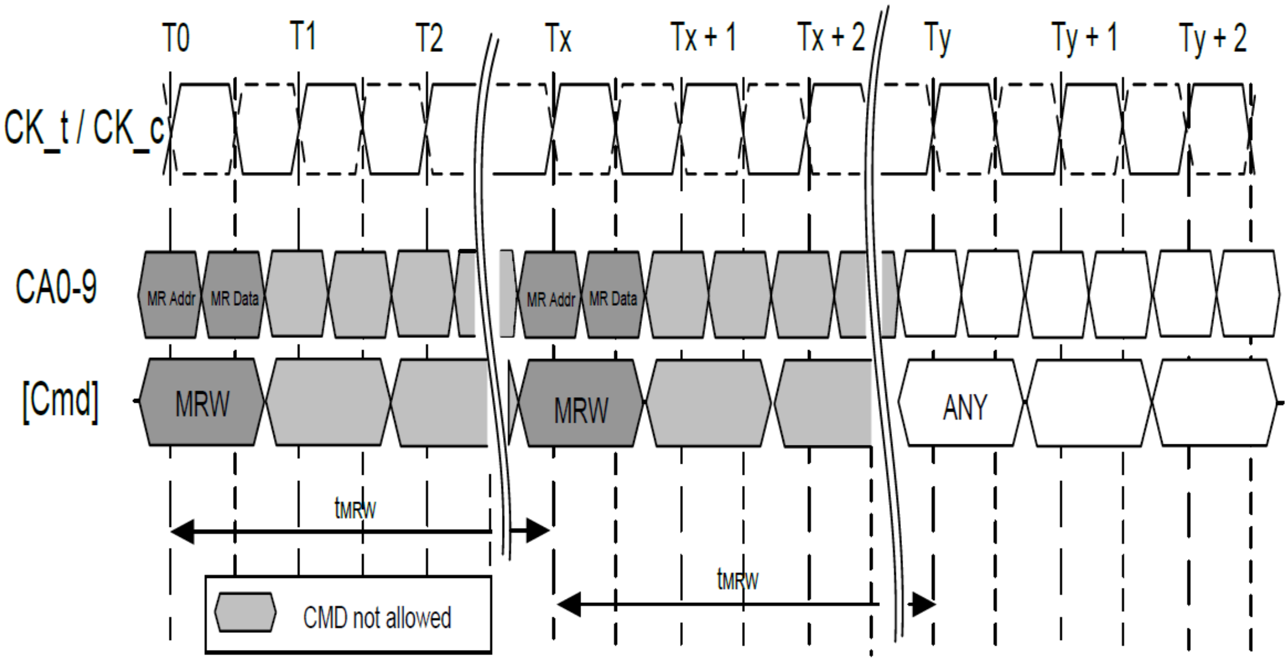
Notes:
1. Mode Register Read has a burst length of four.
2. Mode Register Read operation shall not be interrupted.
3. Mode Register Reads to MR32 and MR40 drive valid data on DQ[0] during the entire burst. For x16 devices, DQ[8] shall drive the same information as DQ[0] during the burst. For x32 devices, DQ[8], DQ[16], and DQ[24] shall drive the same information as DQ[0] during the burst.
4.For x32 devices, DQ[7:1], DQ[15:9], DQ[23:17], and DQ[31:25] may optionally drive the same information as DQ[0] or they may drive 0b during the burst.
5. The Mode Register Command period is tMRR. No command (other than Nop) is allowed during this period.

8.4.20 Mode Register Write Command

The Mode Register Write command is used to write configuration data to mode registers. The Mode Register Write (MRW) command is initiated by having CS_n LOW, CA0 LOW, CA1 LOW, CA2 LOW, and CA3 LOW at the rising edge of the clock. The mode register is selected by {CA1f-CA0f, CA9r-CA4r}. The data to be written to the mode register is contained in CA9f-CA2f. The MRW command period is defined by tMRW. Mode Register Writes to read-only registers shall have no impact on the functionality of the device.

For LPDDR2-S4 devices, the MRW may only be issued when all banks are in the idle precharge state. One method of ensuring that the banks are in the idle precharge state is to issue a Precharge-All command.

8.4.20.1 Mode Register Write Timing Example: RL = 3, tMRW = 5



Notes:
1. The Mode Register Write Command period is tMRW. No command (other than Nop) is allowed during this period.
2. At time Ty, the device is in the idle state.

8.4.20.2 Truth Table for Mode Register Read (MRR) and Mode Register Write (MRW)

Current State	Command	Intermediate State	Next State
All Banks Idle	MRR	Mode Register Reading (All Banks Idle)	All Banks Idle
	MRW	Mode Register Writing (All Banks Idle)	All Banks Idle
	MRW (RESET)	Resetting (Device Auto-Initialization)	All Banks Idle
Bank(s) Active	MRR	Mode Register Reading (Bank(s) Active)	Bank(s) Active
	MRW	Not Allowed	Not Allowed
	MRW (RESET)	Not Allowed	Not Allowed

8.4.21 Mode Register Write Reset (MRW Reset)

Any MRW command issued to MRW63 initiates an MRW Reset. The MRW Reset command brings the device to the Device Auto-Initialization (Resetting) State in the Power-On Initialization sequence (see step 3 in sections 8.2.1 “Power Ramp and Device Initialization”). The MRW Reset command may be issued from the Idle state for LPDDR2-S4 devices. This command resets all Mode Registers to their default values. No commands other than NOP may be issued to the LPDDR2 device during the MRW Reset period (tINIT4). After MRW Reset, boot timings must be observed until the device initialization sequence is complete and the device is in the Idle state. Array data for LPDDR2-S4 devices are undefined after the MRW Reset command.

For the timing diagram related to MRW Reset, refer to 8.2.3 “Power Ramp and Initialization Sequence” figure.

8.4.22 Mode Register Write ZQ Calibration Command

The MRW command is also used to initiate the ZQ Calibration command. The ZQ Calibration command is used to calibrate the LPDDR2 output drivers (RON) over process, temperature, and voltage. LPDDR2-S4 devices support ZQ Calibration.

There are four ZQ Calibration commands and related timings times, tZQINIT, tZQRESET, tZQCL, and tZQCS. tZQINIT corresponds to the initialization calibration, tZQRESET for resetting ZQ setting to default, tZQCL is for long calibration, and tZQCS is for short calibration. See Mode Register 10 (MR10) for description on the command codes for the different ZQ Calibration commands.

The Initialization ZQ Calibration (ZQINIT) shall be performed for LPDDR2-S4 devices. This Initialization Calibration achieves a RON accuracy of ±15%. After initialization, the ZQ Long Calibration may be used to re-calibrate the system to a RON accuracy of ±15%. A ZQ Short Calibration may be used periodically to compensate for temperature and voltage drift in the system.

The ZQ Reset Command resets the RON calibration to a default accuracy of ±30% across process, voltage, and temperature. This command is used to ensure RON accuracy to ±30% when ZQCS and ZQCL are not used.

One ZQCS command can effectively correct a minimum of 1.5% (ZQ Correction) of RON impedance error within tZQCS for all speed bins assuming the maximum sensitivities specified in the 'Output Driver Voltage and Temperature Sensitivity'. The appropriate interval between ZQCS commands can be determined from these tables and other application-specific parameters.

One method for calculating the interval between ZQCS commands, given the temperature (Tdriftrate) and voltage (Vdriftrate) drift rates that the LPDDR2 is subject to in the application, is illustrated. The interval could be defined by the following formula:

$$\frac{ZQCorrection}{(TSens \times Tdriftrate) + (VSens \times Vdriftrate)}$$

where TSens = max(dRONdT) and VSens = max(dRONdV) define the LPDDR2 temperature and voltage sensitivities.

For example, if TSens = 0.75% / C, VSens = 0.20% / mV, Tdriftrate = 1 C / sec and Vdriftrate = 15 mV / sec, then the interval between ZQCS commands is calculated as:

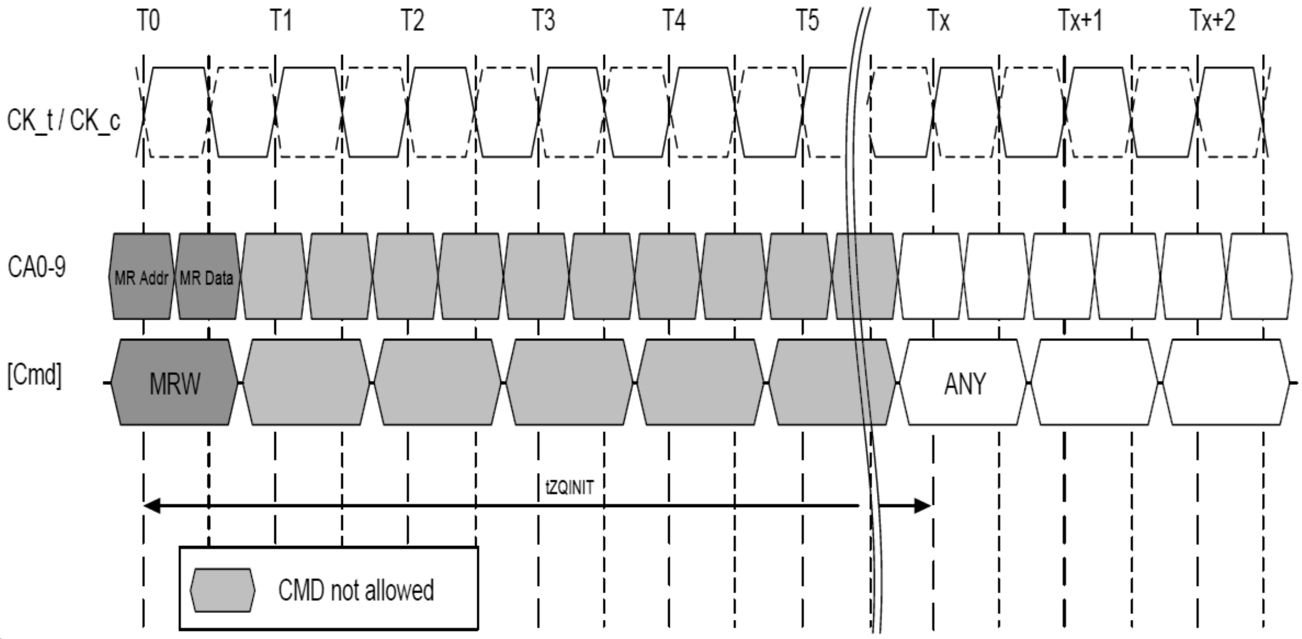
$$\frac{1.5}{(0.75 \times 1) + (0.20 \times 15)} = 0.4s$$

For LPDDR2-S4 devices, a ZQ Calibration command may only be issued when the device is in Idle state with all banks precharged.

No other activities can be performed on the LPDDR2 data bus during the calibration period (tZQINIT, tZQCL, tZQCS). The quiet time on the LPDDR2 data bus helps to accurately calibrate RON. There is no required quiet time after the ZQ Reset command. If multiple devices share a single ZQ Resistor, only one device may be calibrating at any given time. After calibration is achieved, the LPDDR2 device shall disable the ZQ pad's current consumption path to reduce power.

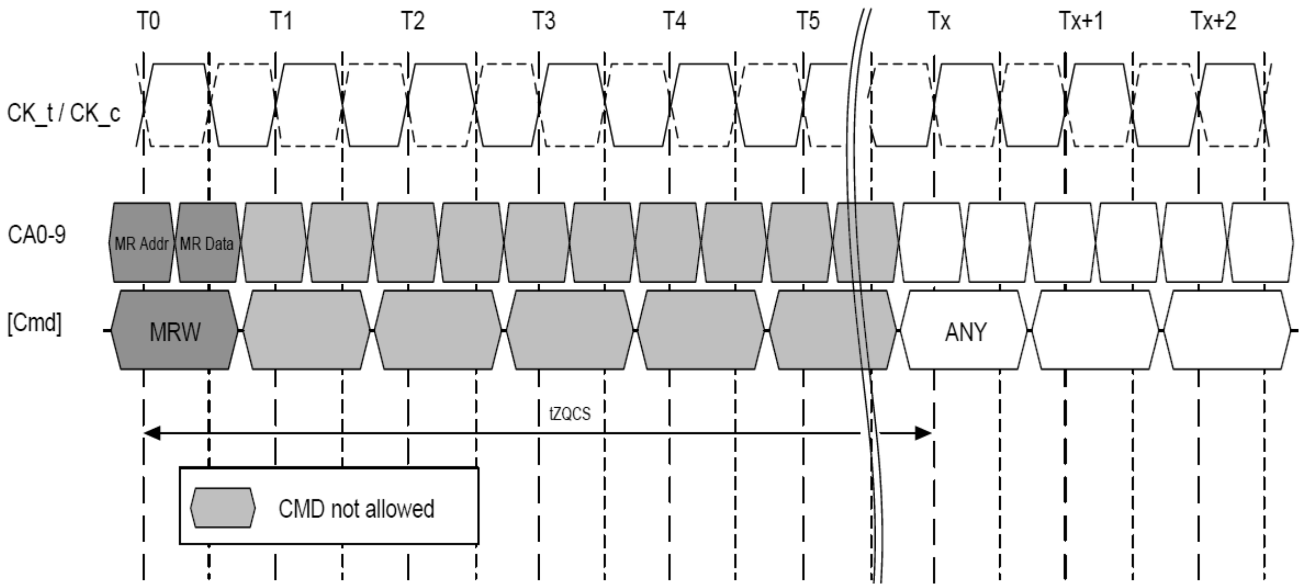
In systems that share the ZQ resistor between devices, the controller must not allow overlap of tZQINIT, tZQCS, or tZQCL between the devices. ZQ Reset overlap is allowed. If the ZQ resistor is absent from the system, ZQ shall be connected to VDD2. In this case, the LPDDR2 device shall ignore ZQ calibration commands and the device will use the default calibration settings (See section 9.2.6.5 "RONPU and RONPD Characteristics without ZQ Calibration" Output Driver DC Electrical Characteristics without ZQ Calibration table).

8.4.22.1 ZQ Calibration Initialization Timing Example



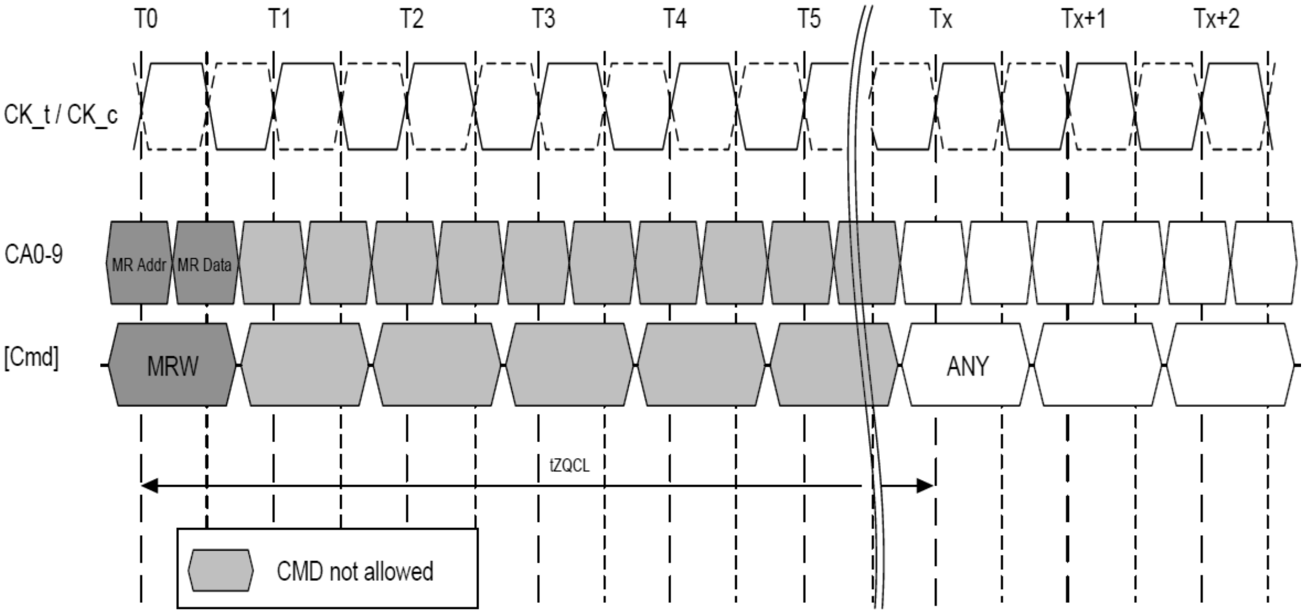
Notes:
1. The ZQ Calibration Initialization period is tZQINIT. No command (other than Nop) is allowed during this period.
2. CKE must be continuously registered HIGH during the calibration period.
3. All devices connected to the DQ bus should be high impedance during the calibration process.

8.4.22.2 ZQ Calibration Short Timing Example



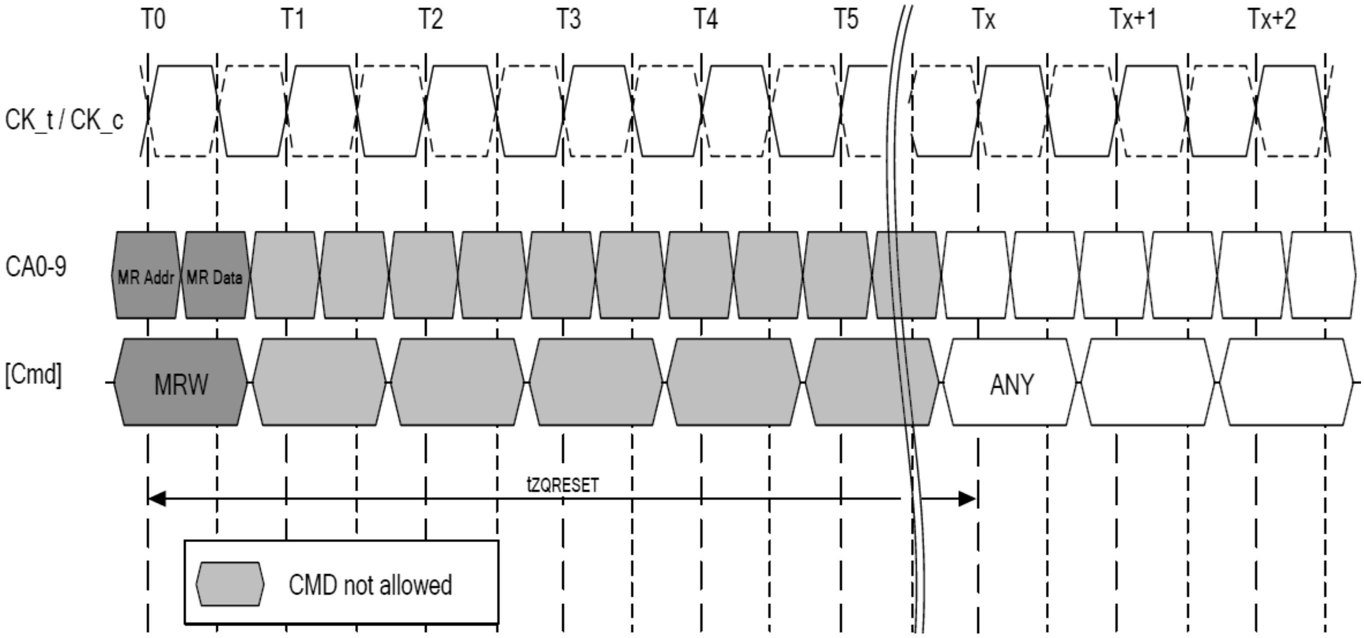
Notes:
1. The ZQ Calibration Short period is tZQCS. No command (other than Nop) is allowed during this period.
2. CKE must be continuously registered HIGH during the calibration period.
3. All devices connected to the DQ bus should be high impedance during the calibration process.

8.4.22.3 ZQ Calibration Long Timing Example



Notes:
1. The ZQ Calibration Long period is tZQCL. No command (other than Nop) is allowed during this period.
2. CKE must be continuously registered HIGH during the calibration period.
3. All devices connected to the DQ bus should be high impedance during the calibration process.

8.4.22.4 ZQ Calibration Reset Timing Example



Notes:
1. The ZQ Calibration Reset period is tZQRESET. No command (other than Nop) is allowed during this period.
2. CKE must be continuously registered HIGH during the calibration period.
3. All devices connected to the DQ bus should be high impedance during the calibration process.

8.4.22.5 ZQ External Resistor Value, Tolerance, and Capacitive Loading

To use the ZQ Calibration function, a 240 Ohm ± 1% tolerance external resistor must be connected between the ZQ pad and ground. A single resistor can be used for each LPDDR2 device or one resistor can be shared between multiple LPDDR2 devices if the ZQ calibration timings for each LPDDR2 device do not overlap. The total capacitive loading on the ZQ pad must be limited (See section 9.2.6.7 "Input/Output Capacitance" table).

8.4.23 Power-Down

For LPDDR2 SDRAM, power-down is synchronously entered when CKE is registered LOW and CS_n HIGH at the rising edge of clock. CKE must be registered HIGH in the previous clock cycle. A NOP command must be driven in the clock cycle following the power-down command. CKE is not allowed to go LOW while mode register, read, or write operations are in progress. CKE is allowed to go LOW while any of other operations such as row activation, precharge, autoprecharge, or refresh is in progress, but power-down IDD spec will not be applied until finishing those operations. Timing diagrams are shown in the following pages with details for entry into power down.

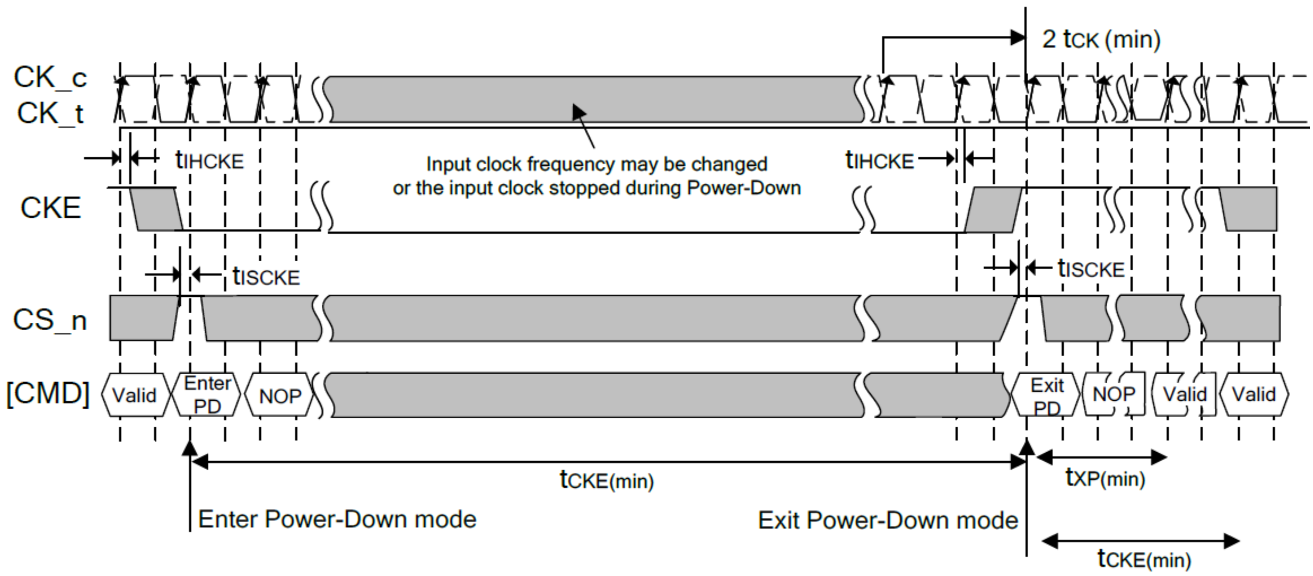
For LPDDR2 SDRAM, if power-down occurs when all banks are idle, this mode is referred to as idle power- down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down.

Entering power-down deactivates the input and output buffers, excluding CK_t, CK_c, and CKE. In power-down mode, CKE must be maintained LOW while all other input signals are "Don't Care". CKE LOW must be maintained until tCKE has been satisfied. VREF must be maintained at a valid level during power down.
VDDQ may be turned off during power down. If VDDQ is turned off, then VREFDQ must also be turned off. Prior to exiting power down, both VDDQ and VREFDQ must be within their respective min/max operating ranges (See 9.2.1.1 "Recommended DC Operating Conditions" table).

For LPDDR2 SDRAM, the maximum duration in power-down mode is only limited by the refresh requirements outlined in section 8.4.16 "LPDDR2 SDRAM Refresh Requirements", as no refresh operations are performed in power-down mode.

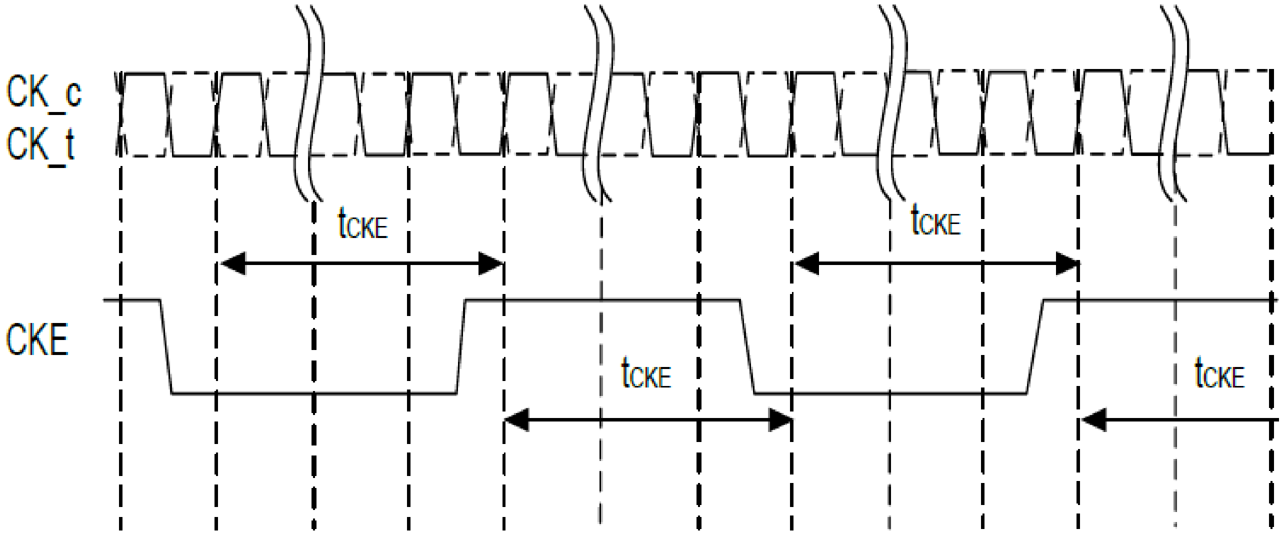
The power-down state is exited when CKE is registered HIGH. The controller shall drive CS_n HIGH in conjunction with CKE HIGH when exiting the power-down state. CKE HIGH must be maintained until tCKE has been satisfied. A valid, executable command can be applied with power-down exit latency, tXP after CKE goes HIGH. Power-down exit latency is defined in section 9.7.1 "LPDDR2 AC Timing" table.

8.4.23.1 Basic Power Down Entry and Exit Timing

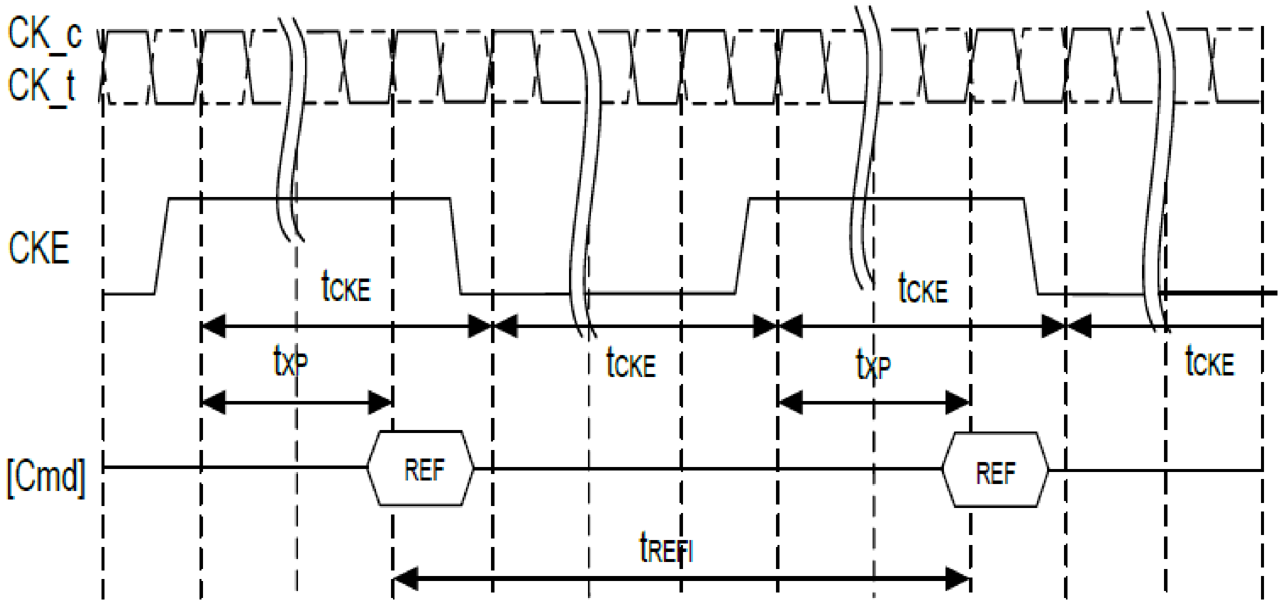


Note:
Input clock frequency may be changed or the input clock stopped during power-down, provided that upon exiting power-down, the clock is stable and within specified limits for a minimum of 2 clock cycles prior to power-down exit and the clock frequency is between the minimum and maximum frequency for the particular speed grade.

8.4.23.2 Example of CKE Intensive Environment

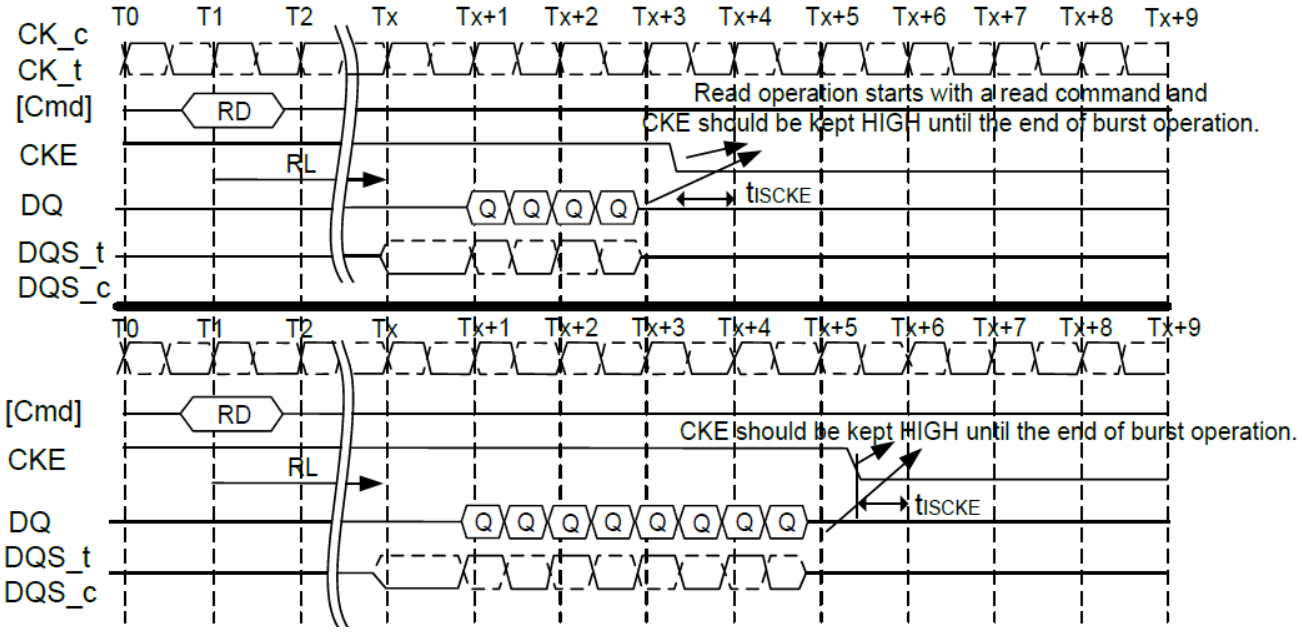


8.4.23.3 Refresh to Refresh Timing with CKE Intensive Environment



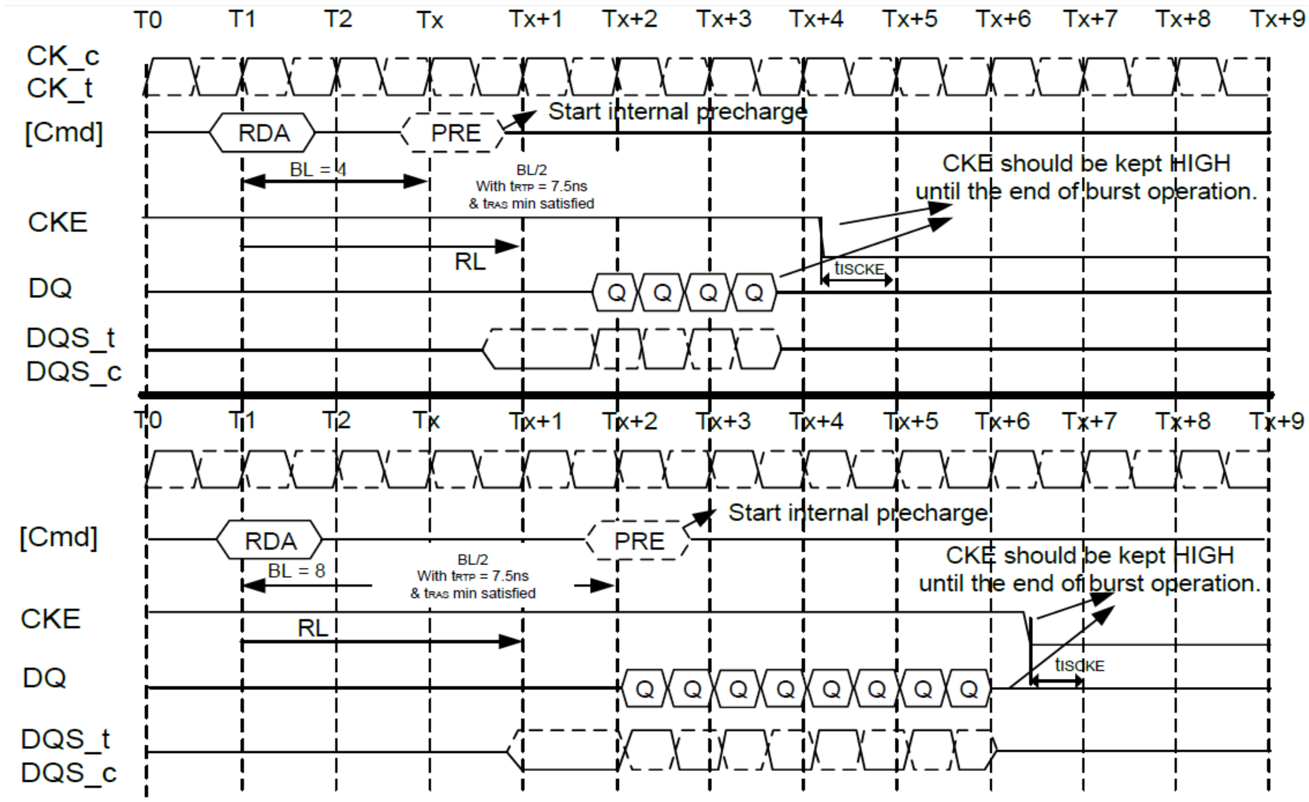
Note:
The pattern shown above can repeat over a long period of time. With this pattern, LPDDR2 SDRAM guarantees all AC and DC timing & voltage specifications with temperature and voltage drift.

8.4.23.4 Read to Power-Down Entry



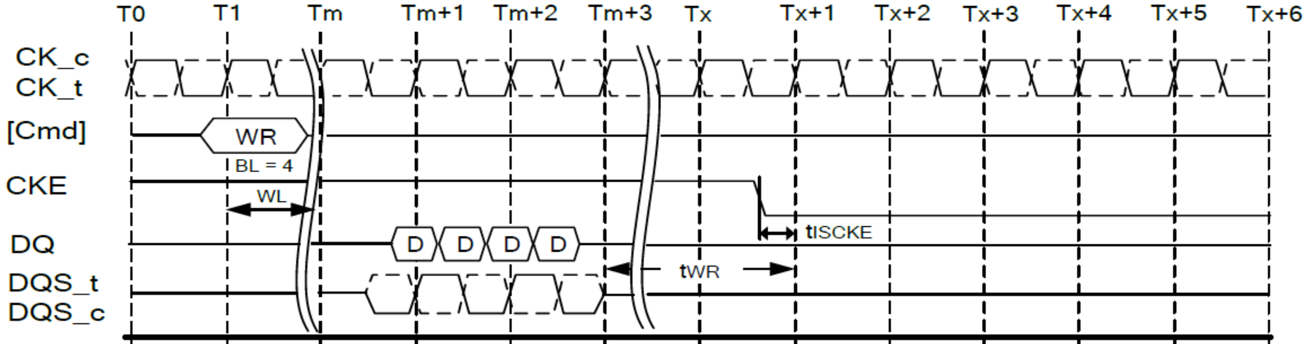
Note:
CKE may be registered LOW RL + RU(tDQSCK(MAX)/tCK)+ BL/2 + 1 clock cycles after the clock on which the Read command is Registered.

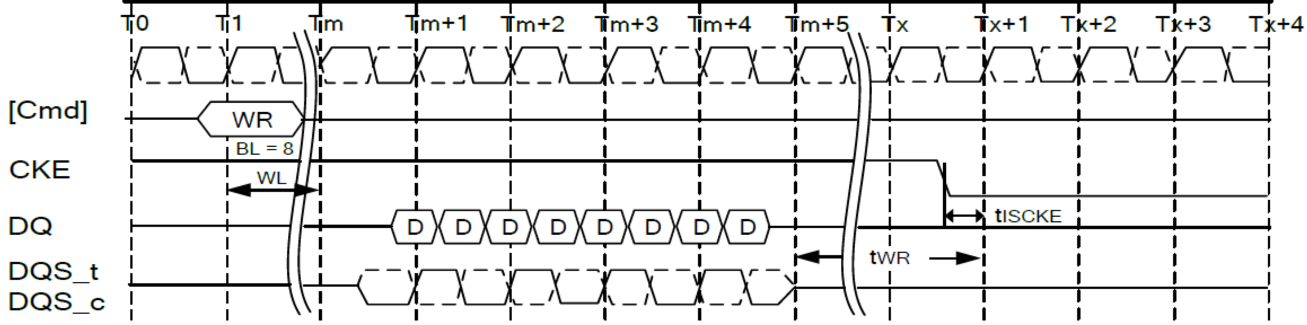
8.4.23.5 Read with Auto precharge to Power-Down Entry



Note:
CKE may be registered LOW RL + RU(tDQSCK(MAX)/tCK)+ BL/2 + 1 clock cycles after the clock on which the Read command is registered.

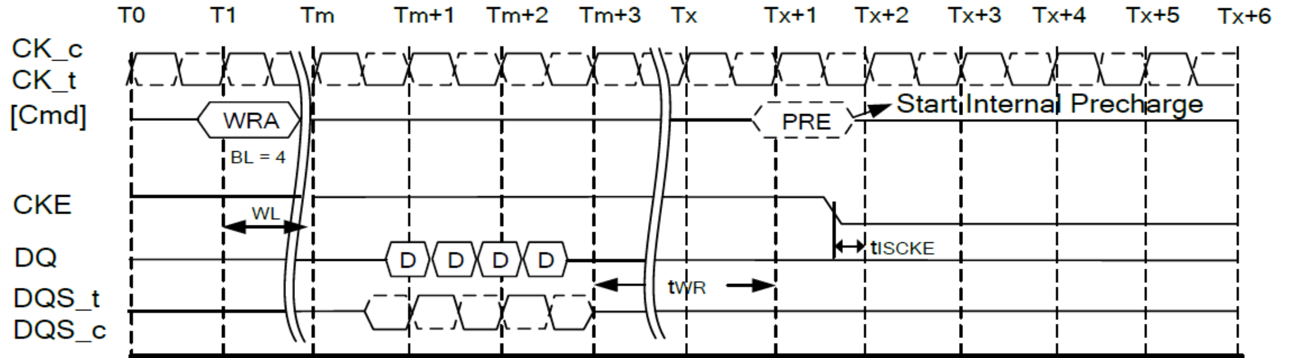
8.4.23.6 Write to Power-Down Entry

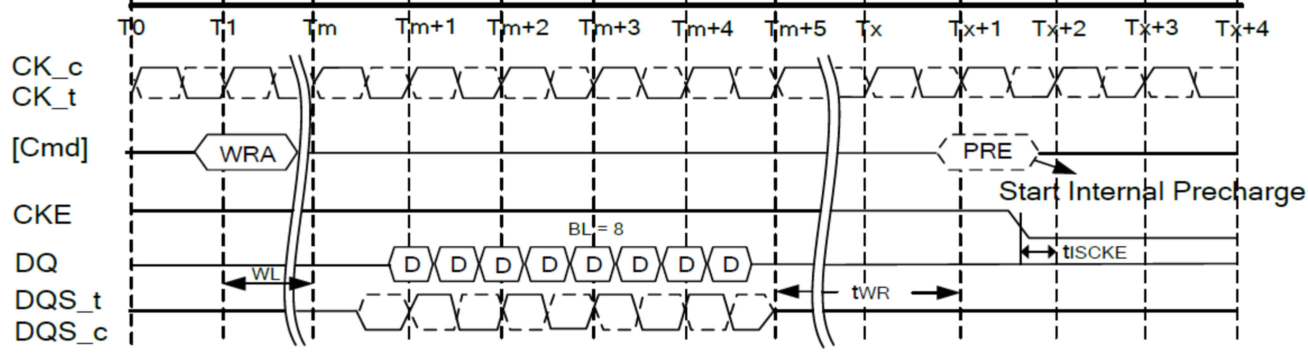




Note:
CKE may be registered LOW WL + 1 + BL/2 + RU(tWR/tCK) clock cycles after the clock on which the Write command is registered.

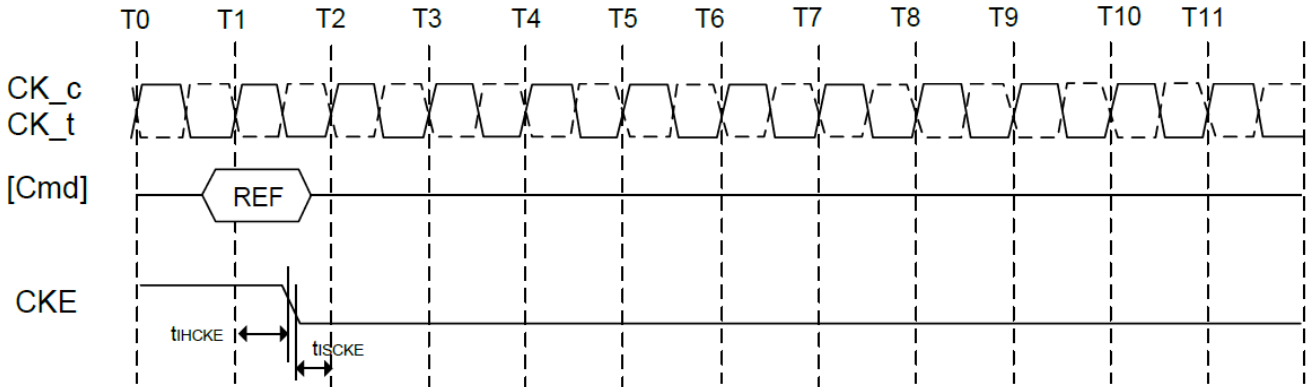
8.4.23.7 Write with Auto Precharge to Power-Down Entry





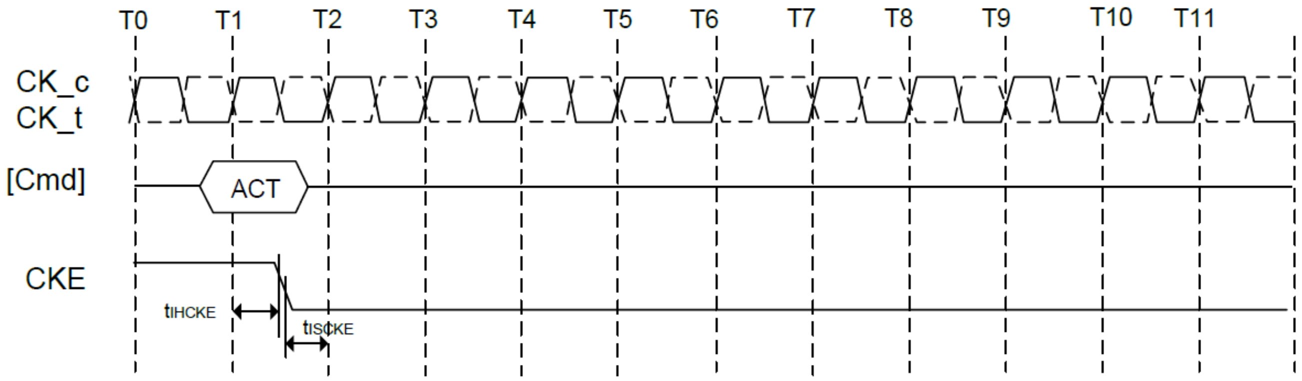
Note:
CKE may be registered LOW WL + 1 + BL/2 + RU(tWR/tCK) + 1 clock cycles after the Write command is registered.

8.4.23.8 Refresh Command to Power-Down Entry

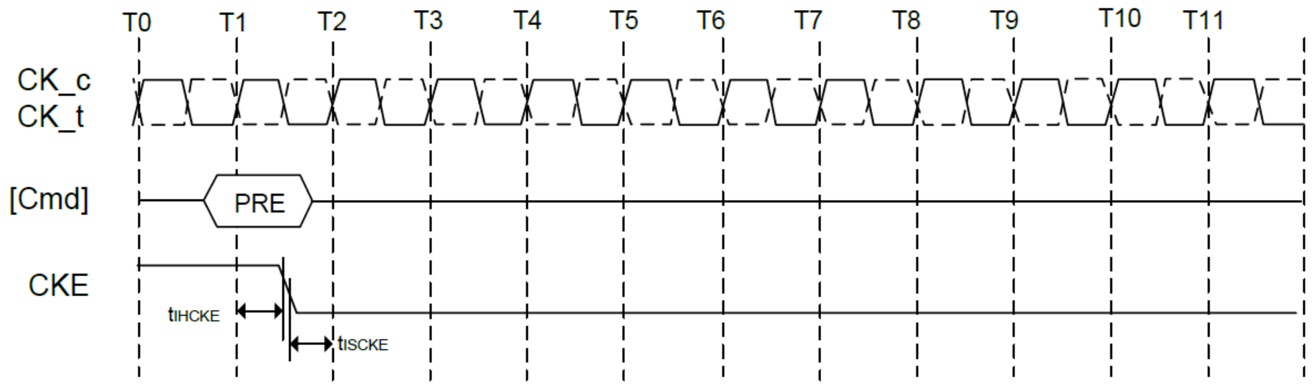


Note:
CKE may go LOW tIHCKE after the clock on which the Refresh command is registered.

8.4.23.9 Activate Command to Power-Down Entry

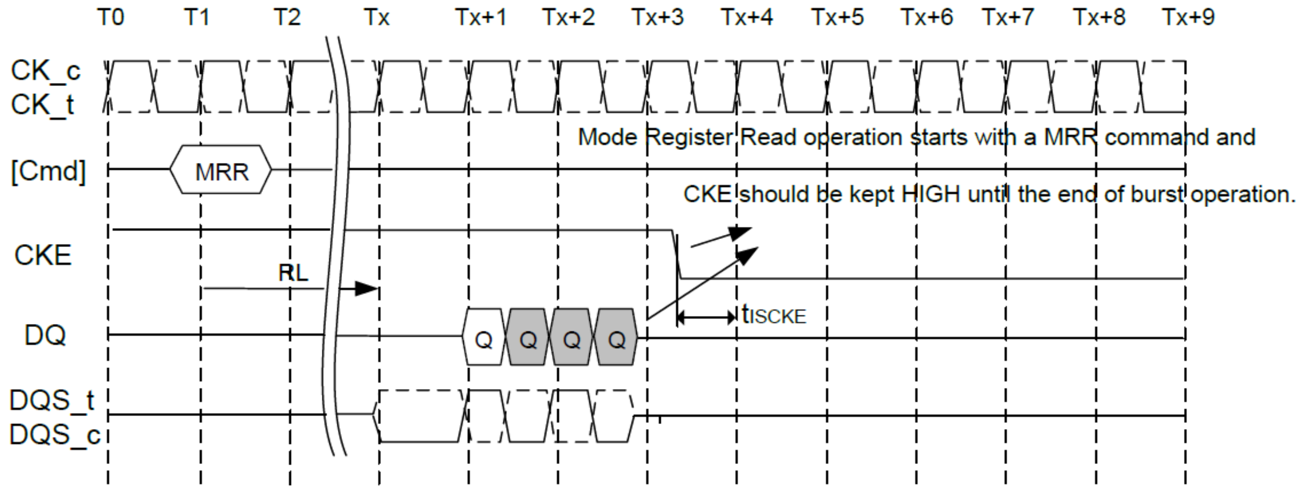


8.4.23.10 Precharge/Precharge-all Command to Power-Down Entry



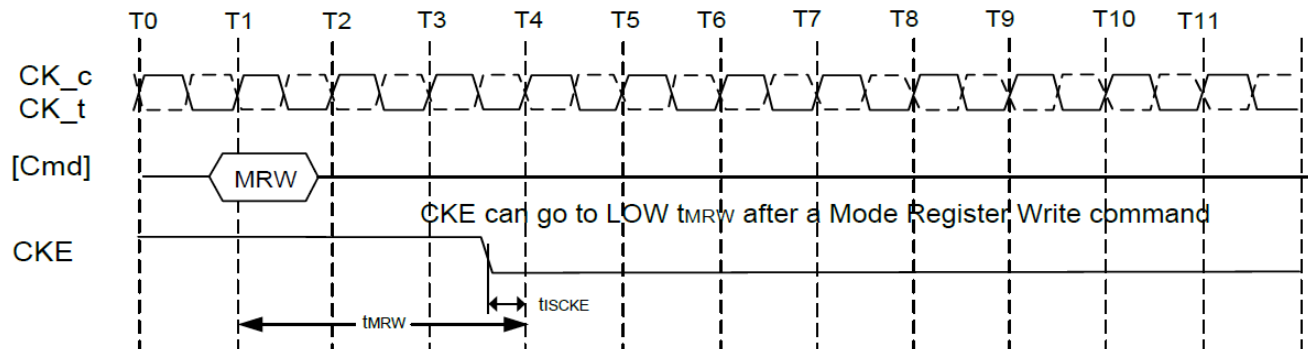
Note:
CKE may go LOW tIHCKE after the clock on which the Precharge/Precharge-All command is registered.

8.4.23.11 Mode Register Read to Power-Down Entry



Note:
CKE may be registered LOW RL + RU(tDQSCK(MAX)/tCK)+ BL/2 + 1 clock cycles after the clock on which the Mode Register Read command is registered.

8.4.23.12 MRW Command to Power-Down Entry



Note:
CKE may be registered LOW tMRW after the clock on which the Mode Register Write command is registered.

8.4.24 Deep Power-Down

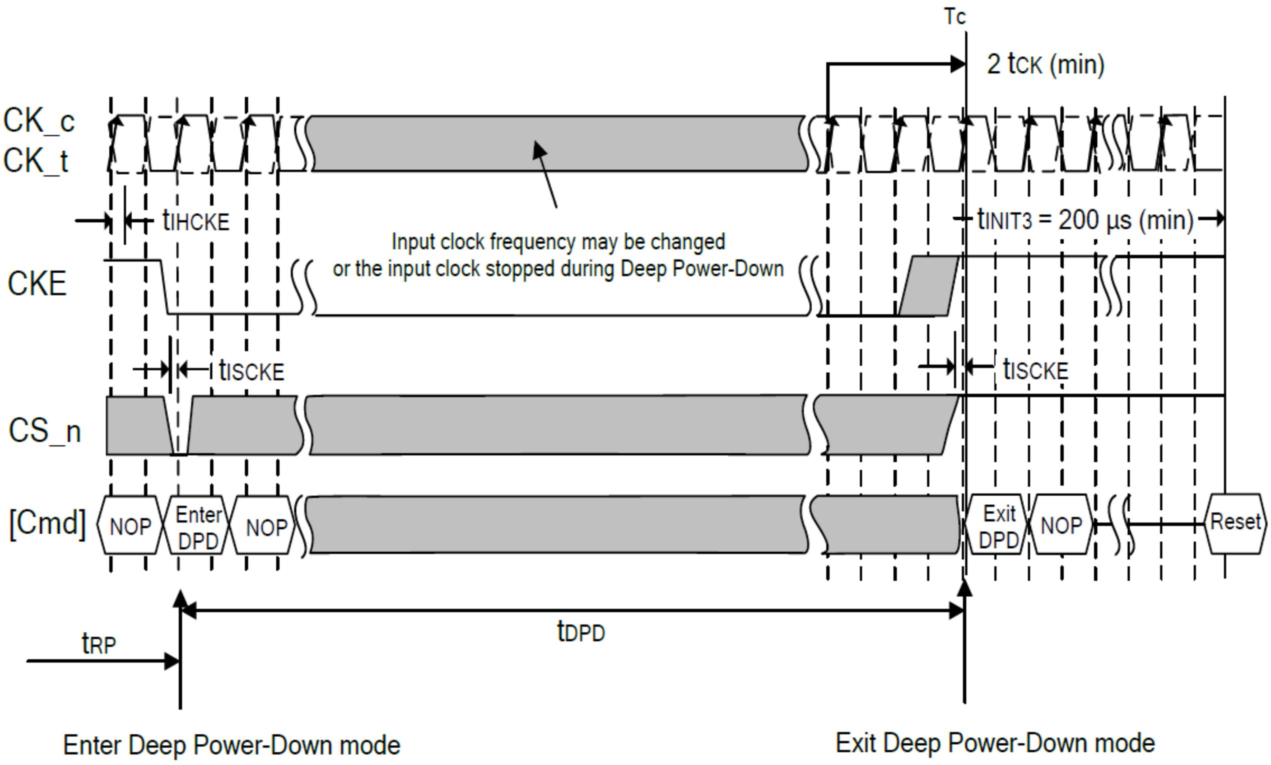
Deep Power-Down is entered when CKE is registered LOW with CS_n LOW, CA0 HIGH, CA1 HIGH, and CA2 LOW at the rising edge of clock. A NOP command must be driven in the clock cycle following the power-down command. CKE is not allowed to go LOW while mode register, read, or write operations are in progress. All banks must be in idle state with no activity on the data bus prior to entering the Deep Power Down mode. During Deep Power-Down, CKE must be held LOW.

In Deep Power-Down mode, all input buffers except CKE, all output buffers, and the power supply to internal circuitry may be disabled within the SDRAM. All power supplies must be within specified limits prior to exiting Deep Power- Down. VrefDQ and VrefCA may be at any level within minimum and maximum levels (See 9.1 “Absolute Maximum DC Ratings”). However prior to exiting Deep Power-Down, Vref must be within specified limits (See 9.2.1.1 “Recommended DC Operating Conditions”).

The contents of the SDRAM may be lost upon entry into Deep Power-Down mode.
The Deep Power-Down state is exited when CKE and CS_n are registered HIGH, while meeting tISCKE with a stable clock input. The SDRAM must be fully re-initialized by controller as described in the Power up initialization

Sequence. The SDRAM is ready for normal operation after the initialization sequence.

8.4.24.1 Deep Power Down Entry and Exit Timing



Notes:
1. Initialization sequence may start at any time after TC.
2. tINIT3 and TC refer to timings in the LPDDR2 initialization sequence. For more detail, see section 8.2 “Power-up, Initialization, and Power-Off”.
3. Input clock frequency may be changed or the input clock stopped during deep power-down, provided that upon exiting deep power-down, the clock is stable and within specified limits for a minimum of 2 clock cycles prior to deep power-down exit and the clock frequency is between the minimum and maximum frequency for the particular speed grade.

8.4.25 Input Clock Stop and Frequency Change

LPDDR2 devices support input clock frequency change during CKE LOW under the following conditions:

- tCK(abs)min is met for each clock cycle;
- Refresh Requirements apply during clock frequency change;
- During clock frequency change, only REFab commands may be executing;
- Any Activate, or Precharge commands have executed to completion prior to changing the frequency;
- The related timing conditions (tRCD, tRP) have been met prior to changing the frequency;
- The initial clock frequency shall be maintained for a minimum of 2 clock cycles after CKE goes LOW;
- The clock satisfies tCH(abs) and tCL(abs) for a minimum of 2 clock cycles prior to CKE going HIGH.

After the input clock frequency is changed and CKE is held HIGH, additional MRW commands may be required to set the WR, RL etc. These settings may need to be adjusted to meet minimum timing requirements at the target clock frequency.

LPDDR2 devices support clock stop during CKE LOW under the following conditions:

- CK_t is held LOW and CK_c is held HIGH during clock stop;
- Refresh Requirements apply during clock stop;
- During clock stop, only REFab commands may be executing;
- Any Activate, or Precharge commands have executed to completion prior to stopping the clock;
- The related timing conditions (tRCD, tRP) have been met prior to stopping the clock;

- The initial clock frequency shall be maintained for a minimum of 2 clock cycles after CKE goes LOW;
- The clock satisfies tCH(abs) and tCL(abs) for a minimum of 2 clock cycles prior to CKE going HIGH.

LPDDR2 devices support input clock frequency change during CKE HIGH under the following conditions:

- tCK(abs)min is met for each clock cycle;
- Refresh Requirements apply during clock frequency change;
- Any Activate, Read, Write, Precharge, Mode Register Write, or Mode Register Read commands must have executed to completion, including any associated data bursts prior to changing the frequency;
- The related timing conditions (tRCD, tWR, tWRA, tRP, tMRW, tMRR, etc.) have been met prior to changing the frequency;
- CS_n shall be held HIGH during clock frequency change;
- During clock frequency change, only REFab commands may be executing;
- The LPDDR2 device is ready for normal operation after the clock satisfies tCH(abs) and tCL(abs) for a minimum of 2tCK + tXP.

After the input clock frequency is changed, additional MRW commands may be required to set the WR, RL etc. These settings may need to be adjusted to meet minimum timing requirements at the target clock frequency.

LPDDR2 devices support clock stop during CKE HIGH under the following conditions:

- CK_t is held LOW and CK_c is held HIGH during clock stop;
- CS_n shall be held HIGH during clock stop;
- Refresh Requirements apply during clock stop;
- During clock stop, only REFab commands may be executing;
- Any Activate, Read, Write, Precharge, Mode Register Write, or Mode Register Read commands must have executed to completion, including any associated data bursts prior to stopping the clock;
- The related timing conditions (tRCD, tWR, tWRA, tRP, tMRW, tMRR, etc.) have been met prior to stopping the clock;
- The LPDDR2 device is ready for normal operation after the clock is restarted and satisfies tCH(abs) and tCL(abs) for a minimum of 2tCK + tXP.

8.4.26 No Operation Command

The purpose of the No Operation command (NOP) is to prevent the LPDDR2 device from registering any unwanted command between operations. Only when the CKE level is constant for clock cycle N-1 and clock cycle N, a NOP command may be issued at clock cycle N. A NOP command has two possible encodings:

1. CS_n HIGH at the clock rising edge N.
2. CS_n LOW and CA0, CA1, CA2 HIGH at the clock rising edge N.

The No Operation command will not terminate a previous operation that is still executing, such as a burst read or write cycle.

8.5 Truth Tables

The truth tables provide complementary information to the state diagram, they clarify the device behavior and the applied restrictions when considering the actual state of all the Banks.

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the LPDDR2 device must be powered down and then restarted through the specified initialization sequence before normal operation can continue.

8.5.1 Command Truth Table

Command	Command Pins			DDR CA Pins (10)										CK_t EDGE
	CKE		CS_N	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	
	CK_t(n-1)	CK_t(n)												
MRW	H	H	L	L	L	L	L	MA0	MA1	MA2	MA3	MA4	MA5	↑
			X	MA6	MA7	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	↓
MRR	H	H	L	L	L	L	H	MA0	MA1	MA2	MA3	MA4	MA5	↑
			X	MA6	MA7	X								↓
Refresh (all bank)	H	H	L	L	L	H	H	X						↑
			X	X										↓
Enter Self Refresh	H	L	L	L	L	H	X							↑
	X		X	X										↓
Activate (bank)	H	H	L	L	H	R8	R9	R10	R11	R12	BA0	BA1	X	↑
			X	R0	R1	R2	R3	R4	R5	R6	R7	X	X	↓
Write (bank)	H	H	L	H	L	L	RFU	RFU	C1	C2	BA0	BA1	X	↑
			X	AP*3,4	C3	C4	C5	C6	C7	C8	X	X	X	↓
Read (bank)	H	H	L	H	L	H	RFU	RFU	C1	C2	BA0	BA1	X	↑
			X	AP*3,4	C3	C4	C5	C6	C7	C8	X	X	X	↓
Precharge (per bank, all bank)	H	H	L	H	H	L	H	AB	X	X	BA0	BA1	X	↑
			X	X										↓
BST	H	H	L	H	H	L	L	X						↑
			X	X										↓
Enter Deep Power Down	H	L	L	H	H	L	X							↑
	X		X	X										↓
NOP	H	H	L	H	H	H	X							↑
			X	X										↓
Maintain PD,SREF,DPD (NOP)	L	L	L	H	H	H	X							↑
			X	X										↓
NOP	H	H	H	X										↑
			X	X										↓
Maintain PD,SREF,DPD (NOP)	L	L	H	X										↑
			X	X										↓
Enter Power Down	H	L	H	X										↑
	X		X	X										↓
Exit PD, SREF,DPD	L	H	H	X										↑
	X		X	X										↓

Notes:
1. All LPDDR2 commands are defined by states of CS_n, CA0, CA1, CA2, CA3, and CKE at the rising edge of the clock.
2. For LPDDR2 SDRAM, Bank addresses BA0 and BA1 (BA) determine which bank is to be operated upon.
3. AP is significant only to SDRAM.
4. AP "high" during a READ or WRITE command indicates that an auto-precharge will occur to the bank associated with the READ or WRITE command.
5. "X" means "H or L (but a defined logic level)".
6. Self refresh exit and Deep Power Down exit are asynchronous.
7. VREF must be between 0 and VDDQ during Self Refresh and Deep Power Down operation.
8. CAxr refers to command/address bit "x" on the rising edge of clock.
9. CAxf refers to command/address bit "x" on the falling edge of clock.
10. CS_n and CKE are sampled at the rising edge of clock.
11. The least-significant column address C0 is not transmitted on the CA bus, and is implied to be zero.
12. AB "high" during Precharge command indicates that all bank Precharge will occur. In this case, Bank Address is do-not-care.

8.5.2 CKE Truth Table

Device Current State*3	CKEn-1*1	CKEn*1	CS_n*2	Command n*4	Operation n*4	Device Next State	Notes
Active Power Down	L	L	X	X	Maintain Active Power Down	Active Power Down	
	L	H	H	NOP	Exit Active Power Down	Active	6, 9
Idle Power Down	L	L	X	X	Maintain Idle Power Down	Idle Power Down	
	L	H	H	NOP	Exit Idle Power Down	Idle	6, 9
Resetting Power Down	L	L	X	X	Maintain Resetting Power Down	Resetting Power Down	
	L	H	H	NOP	Exit Resetting Power Down	Idle or Resetting	6, 9, 12
Deep Power Down	L	L	X	X	Maintain Deep Power Down	Deep Power Down	
	L	H	H	NOP	Exit Deep Power Down	Power On	8
Self Refresh	L	L	X	X	Maintain Self Refresh	Self Refresh	
	L	H	H	NOP	Exit Self Refresh	Idle	7, 10
Bank(s) Active	H	L	H	NOP	Enter Active Power Down	Active Power Down	
All Banks Idle	H	L	H	NOP	Enter Idle Power Down	Idle Power Dow	
	H	L	L	Enter Self Refresh	Enter Self Refresh	Self Refresh	
	H	L	L	Deep Power Down	Enter Deep Power Down	Deep Power Down	
Resetting	H	L	H	NOP	Enter Resetting Power Down	Resetting Power Down	
Others states	H	H	Refer to the Command Truth Table				

Notes:
1. “CKEn” is the logic state of CKE at clock rising edge n; “CKEn-1” was the state of CKE at the previous clock edge.
2. “CS_n” is the logic state of CS_n at the clock rising edge n;
3. “Current state” is the state of the LPDDR2 device immediately prior to clock edge n.
4. “Command n” is the command registered at clock edge N, and “Operation n” is a result of “Command n”.
5. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
6. Power Down exit time (tXP) should elapse before a command other than NOP is issued.
7. Self-Refresh exit time (tXSR) should elapse before a command other than NOP is issued.
8. The Deep Power-Down exit procedure must be followed as discussed in the Deep Power-Down section of the Functional Description.
9. The clock must toggle at least once during the tXP period.
10. The clock must toggle at least once during the tXSR time.
11. X’ means ‘Don’t care’.
12. Upon exiting Resetting Power Down, the device will return to the Idle state if tINIT5 has expired.

8.5.3 Current State Bank n - Command to Bank n Truth Table

Current State	Command	Operation	Next State	Notes
Any	NOP	Continue previous operation	Current State	
Idle	ACTIVATE	Select and activate row	Active	
	Refresh (All Bank)	Begin to refresh	Refreshing(All Bank)	6
	MRW	Load value to Mode Register	MR Writing	6
	MRR	Read value from Mode Register	Idle MR Reading	
	Reset	Begin Device Auto-Initialization	Resetting	6, 7
	Precharge	Deactivate row in bank or banks	Precharging	8, 14
Row Active	Read	Select column, and start read burst	Reading	
	Write	Select column, and start write burst	Writing	
	MRR	Read value from Mode Register	Active MR Reading	
	Precharge	Deactivate row in bank or banks	Precharging	8
Reading	Read	Select column, and start new read burst	Reading	9, 10
	Write	Select column, and start write burst	Writing	9, 10, 11
	BST	Read burst terminate	Active	12
Writing	Write	Select column, and start new write burst	Writing	9, 10
	Read	Select column, and start read burst	Reading	9, 10, 13
	BST	Write burst terminate	Active	12
Power On	Reset	Begin Device Auto-Initialization	Resetting	6, 8
Resetting	MRR	Read value from Mode Register	Resetting MR Reading	

Notes:
1. The table applies when both CKEn-1 and CKEn are HIGH, and after tXSR or tXP has been met if the previous state was Power Down.
2. All states and sequences not shown are illegal or reserved.
3. Current State Definitions:
Idle: The bank or banks have been precharged, and tRP has been met.
Active: A row in the bank has been activated, and tRCD has been met. No data bursts / accesses and no register accesses are in progress.
Reading: A Read burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
Writing: A Write burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
4. The following states must not be interrupted by a command issued to the same bank. NOP commands or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other banks are determined by its current state and 8.5.3 “Current State Bank n - Command to Bank n Truth Table”, and according to 8.5.4 “Current State Bank n - Command to Bank m Truth Table”.
Precharging: starts with the registration of a Precharge command and ends when tRP is met. Once tRP is met, the bank will be in the idle state.
Row Activating: starts with registration of an Activate command and ends when tRCD is met. Once tRCD is met, the bank will be in the ‘Active’ state.
Read with AP Enabled: starts with the registration of the Read command with Auto Precharge enabled and ends when tRP has been met. Once tRP has been met, the bank will be in the idle state.
Write with AP Enabled: starts with registration of a Write command with Auto Precharge enabled and ends when tRP has been met. Once tRP is met, the bank will be in the idle state.
5. The following states must not be interrupted by any executable command; NOP commands must be applied to each positive clock edge during these states.
Refreshing (All Bank): starts with registration of a Refresh (All Bank) command and ends when tRFCab is met. Once tRFCab is met, the device will be in an ‘all banks idle’ state.
Idle MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Idle state.
Resetting MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Resetting state.
Active MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Active state.
MR Writing: starts with the registration of a MRW command and ends when tMRW has been met. Once tMRW has been met, the bank will be in the Idle state.
Precharging All: starts with the registration of a Precharge-All command and ends when tRP is met. Once tRP is met, the bank will be in the idle state.
6. Not bank-specific; requires that all banks are idle and no bursts are in progress.
7. Not bank-specific reset command is achieved through Mode Register Write command.
8. This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for pre- charging.
9. A command other than NOP should not be issued to the same bank while a Read or Write burst with Auto Precharge is enabled.
10. The new Read or Write command could be Auto Precharge enabled or Auto Precharge disabled.
11. A Write command may be applied after the completion of the Read burst; otherwise, a BST must be used to end the Read prior to asserting a Write command.
12. Not bank-specific. Burst Terminate (BST) command affects the most recent read/write burst started by the most recent Read/Write command, regardless of bank.

13. A Read command may be applied after the completion of the Write burst; otherwise, a BST must be used to end the Write prior to asserting a Read command.
14. If a Precharge command is issued to a bank in the Idle state, tRP shall still apply.

8.5.4 Current State Bank n - Command to Bank m Truth Table

Current State of Bank n	Command for Bank m	Operation	Next State for Bank m	Notes
Any	NOP	Continue previous operation	Current State of Bank m	
Idle	Any	Any command allowed to Bank m	-	18
Row Activating, Active, or Precharging	Activate	Select and activate row in Bank m	Active	7
	Read	Select column, and start read burst from Bank m	Reading	8
	Write	Select column, and start write burst to Bank m	Writing	8
	Precharge	Deactivate row in bank or banks	Precharging	9
	MRR	Read value from Mode Register	Idle MR Reading or Active MR Readin	10, 11, 13
	BST	Read or Write burst terminate an ongoing Read/Write from/to Bank m	Active	18
Reading (Autoprecharge disabled)	Read	Select column, and start read burst from Bank m	Reading	8
	Write	Select column, and start write burst to Bank m	Writing	8, 14
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	9
Writing (Autoprecharge disabled)	Read	Select column, and start read burst from Bank m	Reading	8, 16
	Write	Select column, and start write burst to Bank m	Writing	8
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	9
Reading with Autoprecharge	Read	Select column, and start read burst from Bank m	Reading	8, 15
	Write	Select column, and start write burst to Bank m	Writing	8, 14, 15
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	9
Writing with Autoprecharge	Read	Select column, and start read burst from Bank m	Reading	8, 15, 16
	Write	Select column, and start write burst to Bank m	Writing	8, 15
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	9
Power On	Reset	Begin Device Auto-Initialization	Resetting	12, 17
Resetting	MRR	Read value from Mode Register	Resetting MR Reading	

Notes:
1. The table applies when both CKEn-1 and CKEn are HIGH, and after tXSR or tXP has been met if the previous state was Self Refresh or Power Down.
2. All states and sequences not shown are illegal or reserved.
3. Current State Definitions:
Idle: the bank has been precharged, and tRP has been met.
Active: a row in the bank has been activated, and tRCD has been met. No data bursts/accesses and no register accesses are in progress.
Reading: a Read burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
Writing: a Write burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
4. Refresh, Self-Refresh, and Mode Register Write commands may only be issued when all bank are idle.
5. A Burst Terminate (BST) command cannot be issued to another bank; it applies to the bank represented by the current state only.
6. The following states must not be interrupted by any executable command; NOP commands must be applied during each clock cycle while in these states:
Idle MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been

met, the bank will be in the Idle state.
Resetting MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Resetting state.
Active MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Active state.
MR Writing: starts with the registration of a MRW command and ends when tMRW has been met. Once tMRW has been met, the bank will be in the Idle state.
7. tRRD must be met between Activate command to Bank n and a subsequent Activate command to Bank m.
8. Reads or Writes listed in the Command column include Reads and Writes with Auto Precharge enabled and Reads and Writes with Auto Precharge disabled.
9. This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for pre-charging.
10. MRR is allowed during the Row Activating state (Row Activating starts with registration of an Activate command and ends when tRCD is met).
11. MRR is allowed during the Precharging state. (Precharging starts with registration of a Precharge command and ends when tRP is met.
12. Not bank-specific; requires that all banks are idle and no bursts are in progress.
13. The next state for Bank m depends on the current state of Bank m (Idle, Row Activating, Precharging, or Active). The reader shall note that the state may be in transition when a MRR is issued. Therefore, if Bank m is in the Row Activating state and Precharging, the next state may be Active and Precharge dependent upon tRCD and tRP respectively.
14. A Write command may be applied after the completion of the Read burst; otherwise a BST must be issued to end the Read prior to asserting a Write command.
15. Read with auto precharge enabled or a Write with auto precharge enabled may be followed by any valid command to other banks provided that the timing restrictions in 8.4.14.2 “Precharge & Auto Precharge Clarification” table are followed.
16. A Read command may be applied after the completion of the Write burst; otherwise, a BST must be issued to end the Write prior to asserting a Read command.
17. Reset command is achieved through Mode Register Write command.
18. BST is allowed only if a Read or Write burst is ongoing.

8.5.5 Data Mask Truth Table

Name (Functional)	DM	DQs	Note
Write enable	L	Valid	1
Write inhibit	H	X	1

Note:
1. Used to mask write data, provided coincident with the corresponding data.

9 ELECTRICAL CHARACTERISTIC

9.1 Absolute Maximum DC Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Parameter	Symbol	Min	Max	Unit	Notes
V_{DD1} supply voltage relative to V_{SS}	VDD1	-0.4	+2.3	V	1
V_{DD2} supply voltage relative to V_{SS}	VDD2	-0.4	+1.6	V	1, 2
V_{DDQ} supply voltage relative to V_{SSQ}	VDDQ	-0.4	+1.6	V	1, 3
Voltage on any ball relative to V_{SS}	VIN, VOUT	-0.4	+1.6	V	
Storage Temperature	TSTG	-55	+125	℃	4

Notes:
1. See “Power Ramp” section.
2. $V_{REFCA} \leqq 0.6 \times V_{DD2}$; however, V_{REFCA} may be $\geqq V_{DD2}$ provided that $V_{REFCA} \leqq$ 300mV.
3. $V_{REFDQ} \leqq 0.6 \times V_{DDQ}$; however, V_{REFDQ} may be $\geqq V_{DDQ}$ provided that $V_{REFDQ} \leqq$ 300mV.
4. Storage Temperature is the case surface temperature on the center/top side of the LPDDR2 device. For the measurement conditions, please refer to JESD51-2 standard.

9.2 AC & DC Operating Conditions

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the LPDDR2 Device must be powered down and then restarted through the specialized initialization sequence before normal operation can continue.

9.2.1 Recommended DC Operating Conditions

9.2.1.1 Recommended DC Operating Conditions

Symbol	LPDDR2-S4B			DRAM	Unit
	Min	Typ	Max		
VDD1	1.7	1.8	1.95	Core Power1	V
VDD2	1.14	1.2	1.3	Core Power2	V
VDDQ	1.14	1.2	1.3	I/O Buffer Power	V

Note: VDD1 uses significantly less power than VDD2.

9.2.2 Input Leakage Current

Parameter / Condition	Symbol	Min	Max	Unit	Note
Input Leakage current					
For CA, CKE, CS_n, CK_t, CK_c Any input 0V $\leqq V_{IN} \leqq V_{DD2}$ (All other pins not under test = 0V)	I_L	-2	2	uA	1

Parameter / Condition	Symbol	Min	Max	Unit	Note
V_{REF} supply leakage current					
VREFDQ = VDDQ/2 or VREFCA = VDD2/2 (All other pins not under test = 0V)	IVREF	-1	1	uA	2

Notes:
1. Although DM is for input only, the DM leakage shall match the DQ and DQS_t/DQS_c output leakage specification.
2. The minimum limit requirement is for testing purposes. The leakage current on VREFCA and VREFDQ pins should be minimal.

9.2.3 Operating Temperature Conditions

Parameter / Condition	Symbol	Rating	Unit
Standard	T_{CASE}	-40 to +85	℃

Notes:
1. Operating temperature is the case surface temperature on the center/top side of the LPDDR2 device. For the measurement conditions, please refer to JESD51-2 standard.
2. Either the device case temperature rating or the temperature sensor may be used to set an appropriate refresh rate, determine the need for AC timing derating and/or monitor the operating temperature. When using the temperature sensor, the actual device case temperature may be higher than the T_{CASE} rating that applies for the Operating Temperature Range. For example, T_{CASE} may be above 85 ℃ when the temperature sensor indicates a temperature of less than 85 ℃.

9.2.4 AC and DC Input Measurement Levels

9.2.4.1 AC and DC Logic Input Levels for Single-Ended Signals

9.2.4.1.1 Single-Ended AC and DC Input Levels for CA and CS_n Inputs

Symbol	Parameter	Value		Unit	Note
		Min	Max		
VIHCA(AC)	AC input logic high	V_{REF} + 0.220	Note 2	V	1,2
VILCA(AC)	AC input logic low	Note 2	V_{REF} - 0.220	V	1,2
VIHCA(DC)	DC input logic high	V_{REF} + 0.130	VDD2	V	1
VILCA(DC)	DC input logic low	VSS	V_{REF} - 0.130	V	1
VREFCA(DC)	Reference Voltage for CA and CS_n inputs	0.49 * V_{DD2}	0.51 * V_{DD2}	V	3,4

Notes:
1. For CA and CS_n input only pins. $V_{REF} = V_{REFCA(DC)}$.
2. See “Overshoot and Undershoot Specifications” section.
3. The ac peak noise on V_{REFCA} may not allow V_{REFCA} to deviate from $V_{REFCA(DC)}$ by more than +/-1% V_{DD2} (for reference: approx. +/- 12 mV).
4. For reference: approx. V_{DD2}/2 +/- 12 mV.

9.2.4.1.2 Single-Ended AC and DC Input Levels for CKE

Symbol	Parameter	Min	Max	Unit	Note
VIHCKE	CKE Input High Level	0.8 * V_{DD2}	Note 1	V	1
VILCKE	CKE Input Low Level	Note 1	0.2 * V_{DD2}	V	1

Note: See "Overshoot and Undershoot Specifications" section.

9.2.4.1.3 Single-Ended AC and DC Input Levels for DQ and DM

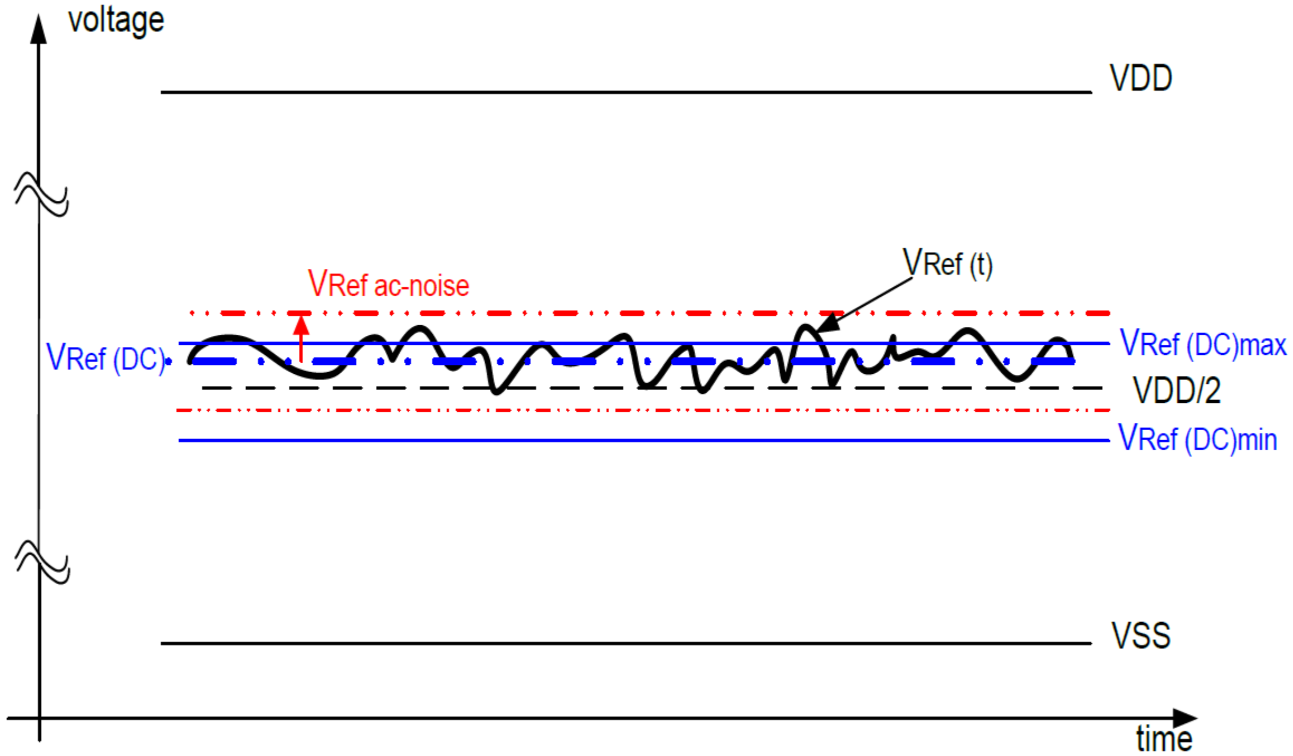
Symbol	Parameter	Value		Unit	Note
		Min	Max		
VIHDQ(AC)	AC input logic high	V_{REF} + 0.220	Note 2	V	1,2
VILDQ(AC)	AC input logic low	Note 2	V_{REF} - 0.220	V	1,2
VIHDQ(DC)	DC input logic high	V_{REF} + 0.130	VDDQ	V	1
VILDQ(DC)	DC input logic low	VSSQ	V_{REF} - 0.130	V	1
VREFDQ(DC)	Reference Voltage for DQ, DM inputs	0.49 * V_{DDQ}	0.51 * V_{DDQ}	V	3,4

Notes:
1. For DQ input only pins. V_{REF} = $V_{REFDQ(DC)}$.
2. See "Overshoot and Undershoot Specifications" section.
3. The ac peak noise on V_{REFDQ} may not allow V_{REFDQ} to deviate from $V_{REFDQ(DC)}$ by more than +/-1% V_{DDQ} (for reference: approx. +/- 12 mV).
4. For reference: approx. V_{DDQ}/2 +/- 12 mV.

9.2.4.2 Vref Tolerances

The DC tolerance limits and ac-noise limits for the reference voltages VRefCA and VRefDQ are illustrated in below "VRef(DC) Tolerance and VRef AC-Noise Limits" figure. It shows a valid reference voltage VRef(t) as a function of time. (VRef stands for VRefCA and VRefDQ likewise). VDD stands for VDD2 for VRefCA and VDDQ for VRefDQ. VRef(DC) is the linear average of VRef(t) over a very long period of time (e.g. 1 sec) and is specified as a fraction of the linear average of VDDQ or VDD2 also over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirements in 9.2.4.1.1 "Single-Ended AC and DC Input Levels for CA and CS_n Inputs" table. Furthermore VRef(t) may temporarily deviate from VRef(DC) by no more than ± 1% VDD. Vref(t) cannot track noise on VDDQ or VDD2 if this would send Vref outside these specifications.

9.2.4.2.1 VRef(DC) Tolerance and VRef AC-Noise Limits



The voltage levels for setup and hold time measurements VIH(AC), VIH(DC), VIL(AC) and VIL(DC) are dependent on VRef.

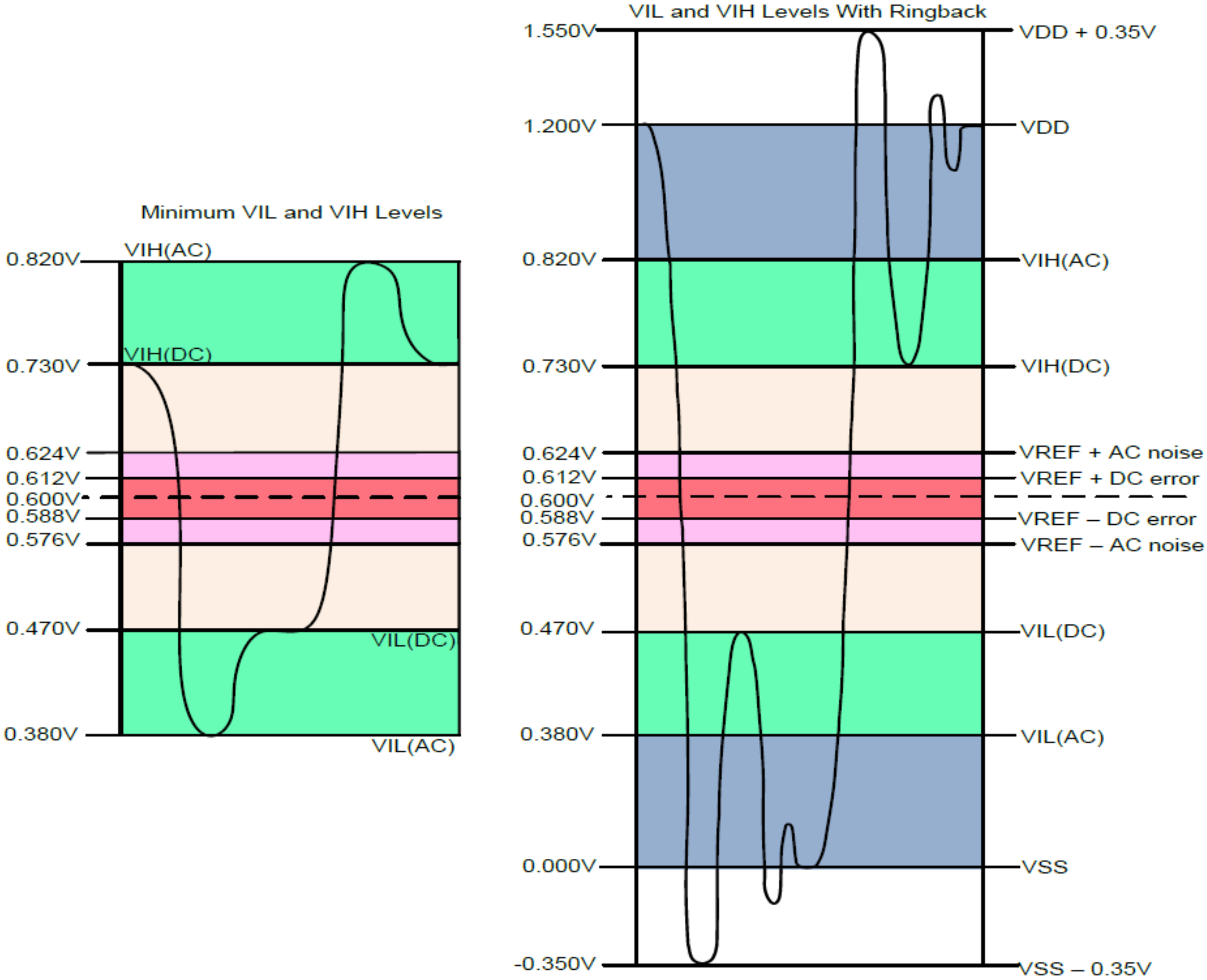
"VRef" shall be understood as VRef(DC), as defined in above "VRef(DC) Tolerance and VRef AC-Noise Limits" figure.

This clarifies that dc-variations of VRef affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. Devices will function correctly with appropriate timing deratings with VREF outside these specified levels so long as VREF is maintained between 0.44 x VDDQ (or VDD2) and 0.56 x VDDQ (or VDD2) and so long as the controller achieves the required single-ended AC and DC input levels from instantaneous VRef (see 9.2.4.1.1 "Single-Ended AC and DC Input Levels for CA and CS_n Inputs" table and 9.2.4.1.3 "Single-Ended AC and DC Input Levels for DQ and DM" table) Therefore, system timing and voltage budgets need to account for VREF deviations outside of this range.

This also clarifies that the LPDDR2 setup/hold specification and derating values need to include time and voltage associated with VRef ac-noise. Timing and voltage effects due to ac-noise on VRef up to the specified limit (± 1% of VDD) are included in LPDDR2 timings and their associated deratings.

9.2.4.3 Input Signal

9.2.4.3.1 LPDDR2-800/1066 Input Signal



Notes:
1. Numbers reflect nominal values.
2. For CA0-9, CK_t, CK_c, and CS_n, VDD stands for VDD2. For DQ, DM, DQS_t, and DQS_c, VDD stands for VDDQ.
3. For CA0-9, CK_t, CK_c, and CS_n, VSS stands for VSS itself. For DQ, DM, DQS_t, and DQS_c, VSS stands for VSSQ.

9.2.4.4 AC and DC Logic Input Levels for Differential Signals

9.2.4.4.1 Differential Signal Definition

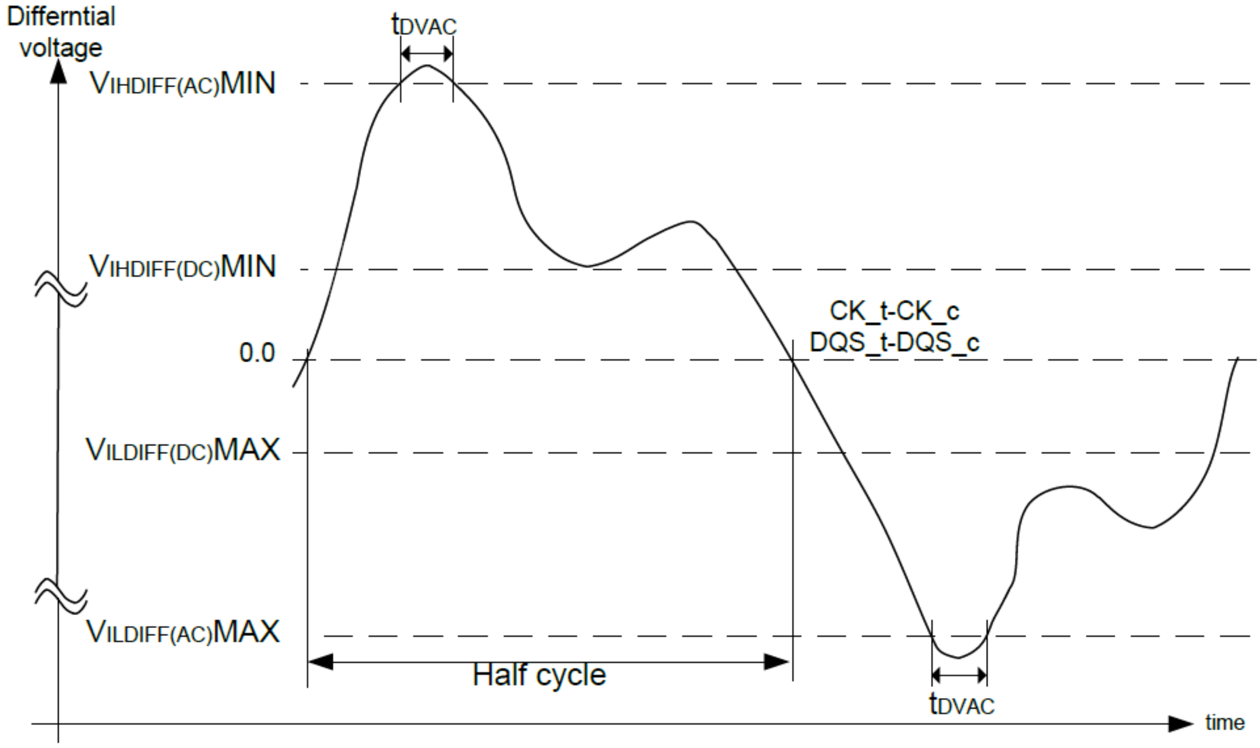


Figure 39: Definition of differential ac-swing and "time above ac-level" tDVAC

9.2.4.4.2 Differential Swing Requirements for Clock (CK_t - CK_c) and Strobe (DQS_t - DQS_c)

Table 6: Table of Differential AC and DC Input Levels

Symbol	Parameter	LPDDR2-800/1066		Unit	Notes
		Min	Max		
VIHdiff(dc)	Differential input high	2 x (VIH(dc) - Vref)	Note 3	V	1
VILdiff(dc)	Differential input logic low	Note 3	2 x (VIL(dc) - Vref)	V	1
VIHdiff(ac)	Differential input high ac	2 x (VIH(ac) - Vref)	Note 3	V	2
VILdiff(ac)	Differential input low ac	Note 3	2 x (VIL(ac) - Vref)	V	2

Notes:
1. Used to define a differential signal slew-rate. For CK_t - CK_c use VIH/VIL(dc) of CA and VREFCA; for DQS_t - DQS_c, use VIH/VIL(dc) of DQs and VREFDQ; if a reduced dc-high or dc-low level is used for a signal group, then the reduced level applies also here.
2. For CK_t - CK_c use VIH/VIL(ac) of CA and VREFCA; for DQS_t - DQS_c, use VIH/VIL(ac) of DQs and VREFDQ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.
3. These values are not defined, however the single-ended signals CK_t, CK_c, DQS_t, and DQS_c need to be within the respective limits (VIH(dc) max, VIL(dc)min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to section 9.2.5.5 "Overshoot and Undershoot Specifications".
4. For CK_t and CK_c, Vref = VrefCA(DC). For DQS_t and DQS_c, Vref = VrefDQ(DC).

Table 7: Allowed Time before RinGback (tDVAC) for CK_t - CK_c and DQS_t - DQS_c

Slew Rate [V/nS]	tDVAC [pS] @ |VIHdiff(ac) or VILdiff(ac)| = 440mV
> 4.0	175
4.0	170
3.0	167
2.0	163
1.8	162
1.6	161
1.4	159
1.2	155
1.0	150
< 1.0	150

9.2.4.5 Single-Ended Requirements for Differential Signals

Each individual component of a differential signal (CK_t, DQS_t, CK_c, or DQS_c) has also to comply with certain requirements for single-ended signals.

CK_t and CK_c shall meet VSEH(ac)min / VSEL(ac)max in every half-cycle.

DQS_t, DQS_c shall meet VSEH(ac)min / VSEL(ac)max in every half-cycle preceeding and following a valid transition.

Note that the applicable ac-levels for CA and DQ's are different per speed-bin.

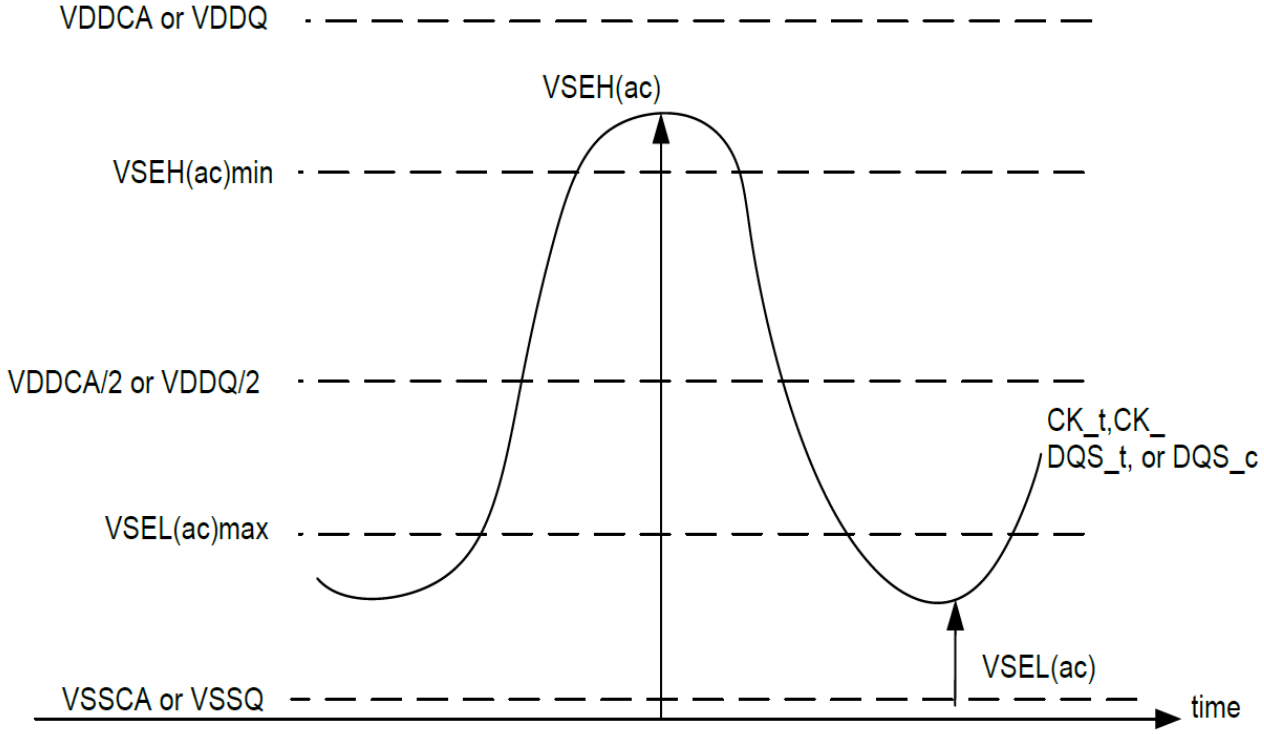


Figure 40: Single-Ended Requirement for Differential Signals

Note that while CA and DQ signal requirements are with respect to Vref, the single-ended components of differential signals have a requirement with respect to VDDQ/2 for DQS_t, DQS_c and VDD2/2 for CK_t, CK_c; this is nominally the same. The transition of single-ended signals through the ac-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach VSEL(ac)max, VSEH(ac)min has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

The signal ended requirements for CK_t, CK_c, DQS_t and DQS_c are found in 9.2.4.1.1 “Single-Ended AC and DC Input Levels for CA and CS_n Inputs” table and 9.2.4.1.3 “Single-Ended AC and DC Input Levels for DQ and DM” table, respectively.

Table 8: Single-Ended Levels for CK_t, DQS_t, CK_c, DQS_c

Symbol	Parameter	Value		Unit	Note
		Min	Max		
VSEH (AC)	Single-ended high-level for strobes	$(V_{DDQ}/2) + 0.220$	Note 3	V	1,2
	Single-ended high-level for CK_t, CK_c	$(V_{DD2}/2) + 0.220$	Note 3	V	1,2
VSEL (AC)	Single-ended low-level for strobes	Note 3	$(V_{DDQ}/2) - 0.220$	V	1,2
	Single-ended low-level for CK_t, CK_c	Note 3	$(V_{DD2}/2) - 0.220$	V	1,2

Notes:
1. For CK_t, CK_c use $V_{SEH}/V_{SEL(AC)}$ of CA; for strobes (DQS0_t, DQS0_c, DQS1_t, DQS1_c, DQS2_t, DQS2_c, DQS3_t, DQS3_c) use $V_{IH}/V_{IL(AC)}$ of DQs.
2. $V_{IH(AC)}/V_{IL(AC)}$ for DQs is based on V_{REFDQ}; $V_{SEH(AC)}/V_{SEL(AC)}$ for CA is based on V_{REFCA}; if a reduced AC high or AC low level is used for a signal group, then the reduced level applies also here.
3. These values are not defined, however the single-ended signals CK_t, CK_c, DQS0_t, DQS0_c, DQS1_t, DQS1_c, DQS2_t, DQS2_c, DQS3_t, DQS3_c need to be within the respective limits ($V_{IH(DC)}$ max, $V_{IL(DC)}$ min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to “Overshoot and Undershoot Specifications” section.

9.2.4.6 Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK_t, CK_c and DQS_t, DQS_c) must meet the requirements of above Single-ended levels for CK_t, DQS_t, CK_c, DQS_c table. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signals to the midlevel between of VDD and VSS.

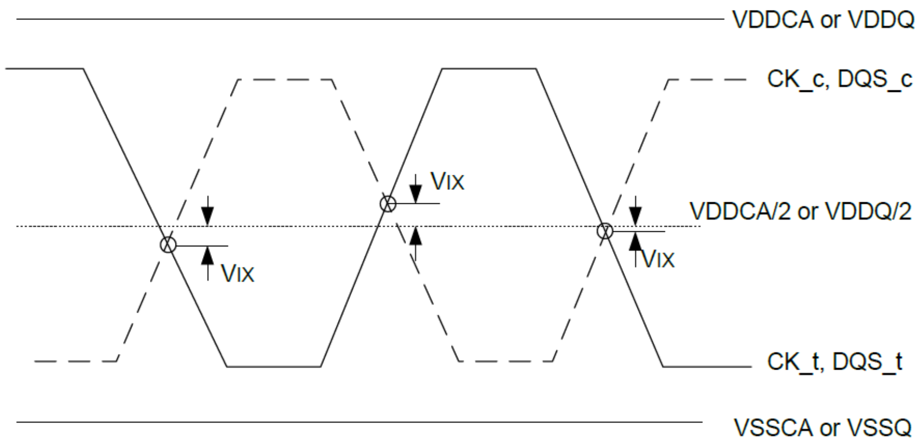


Figure 41: Figure of Vix Definition

Table 9: Table of Cross Point Voltage for Differential Input Signals (CK, DQS)

Symbol	Parameter	Value		Unit	Note
		Min	Max		
V_{IXCA}	Differential Input Cross Point Voltage relative to $V_{DD2}/2$ for CK_t, CK_c	-120	120	mV	1,2
V_{IXDQ}	Differential Input Cross Point Voltage relative to $V_{DDQ}/2$ for DQS_t, DQS_c	-120	120	mV	1,2

Notes:
1. The typical value of VIX(AC) is expected to be about 0.5 × VDD of the transmitting device, and VIX(AC) is expected to track variations in VDD. VIX(AC) indicates the voltage at which differential input signals must cross.
2. For CK_t and CK_c, Vref = VrefCA(DC). For DQS_t and DQS_c, Vref = VrefDQ(DC).

9.2.4.7 Slew Rate Definitions for Single-Ended Input Signals

See section **"CA and CS_n Setup, Hold and Derating"** for single-ended slew rate definitions for address and command signals.

See section **"Data Setup, Hold and Slew Rate Derating"** for single-ended slew rate definitions for data signals.

9.2.4.8 Slew Rate Definitions for Differential Input Signals

Input slew rate for differential signals (CK_t, CK_c and DQS_t, DQS_c) are defined and measured as shown in below table and figure.

Table 10: Differential Input Slew Rate Definition

Description	Measured		Defined by
	from	to	
Differential input slew rate for rising edge (CK_t - CK_c and DQS_t - DQS_c).	VILdiffmax	VIHdiffmin	[VIHdiffmin - VILdiffmax] / DeltaTRdiff
Differential input slew rate for falling edge (CK_t - CK_c and DQS_t - DQS_c).	VIHdiffmin	VILdiffmax	[VIHdiffmin - VILdiffmax] / DeltaTFdiff
Note: The differential signal (i.e. CK_t - CK_c and DQS_t - DQS_c) must be linear between these thresholds.			

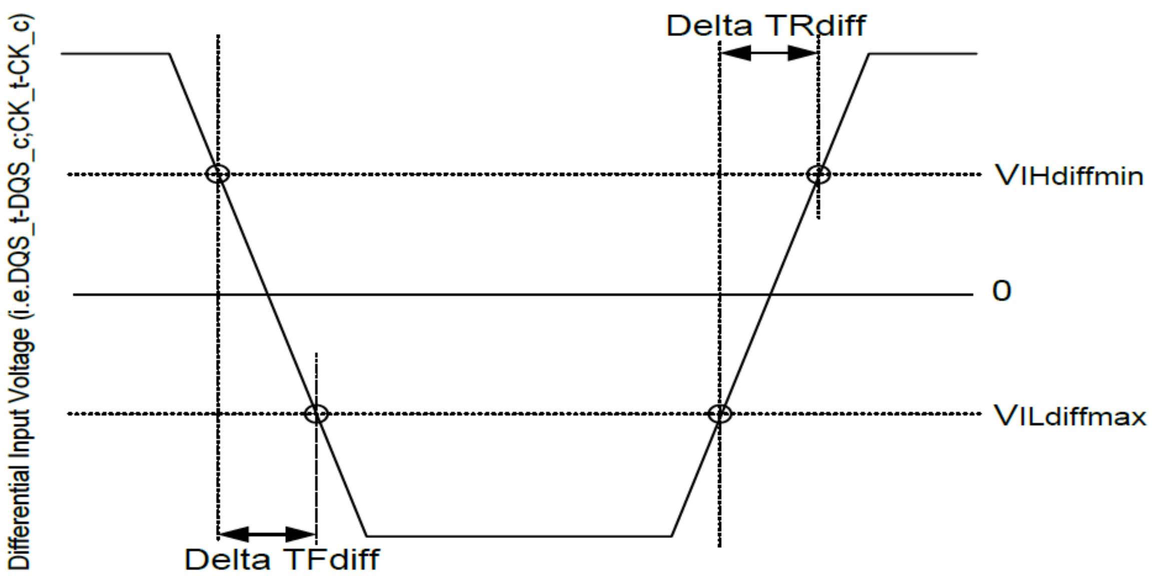


Figure 42: Differential Input Slew Rate Definition for DQS_t, DQS_c and CK_t, CK_c

9.2.5 AC and DC Output Measurement Levels

9.2.5.1 Single Ended AC and DC Output Levels

Table 11: Single-Ended AC and DC Output Levels

Symbol	Parameter	LPDDR2-800/1066		Unit	Notes
$V_{OH(DC)}$	DC output high measurement level (for IV curve linearity)	0.9 x V_{DDQ}		V	1
$V_{OL(DC)}$	DC output low measurement level (for IV curve linearity)	0.1 x V_{DDQ}		V	2
$V_{OH(AC)}$	AC output high measurement level (for output slew rate)	V_{REFDQ} + 0.12		V	
$V_{OL(AC)}$	AC output low measurement level (for output slew rate)	V_{REFDQ} - 0.12		V	
I_{OZ}	Output Leakage current (DQ, DM, DQS_t, DQS_c) (DQ, DQS_t, DQS_c are disabled;0V ≤ Vout ≤ VDDQ)	Min	-5	µA	
		Max	+5		
MM_{PUPD}	Delta RON between pull-up and pull-down for DQ/DM	Miin	-15	%	
		Max	+15		

Notes:
1. IOH = -0.1mA.
2. IOL = +0.1mA.

9.2.5.2 Differential AC and DC Output Levels

Table 12: Differential AC and DC Output Levels of (DQS_t, DQS_c)

Symbol	Parameter	LPDDR2-800/1066	Unit	Notes
$V_{OHdiff(AC)}$	AC differential output high measurement level (for output SR)	+ 0.20 x V_{DDQ}	V	
$V_{OLdiff(AC)}$	AC differential output low measurement level (for output SR)	- 0.20 x V_{DDQ}	V	

Notes:
1. IOH = -0.1mA.
2. IOL = +0.1mA.

9.2.5.3 Single Ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC) for single ended signals as shown in below table and figure.

Table 13: Single-Ended Output Slew Rate Definition

Description	Measured		Defined by
	from	to	
Single-ended output slew rate for rising edge	$V_{OL(AC)}$	$V_{OH(AC)}$	[$V_{OH(AC)}$ - $V_{OL(AC)}$] / DeltaTRse
Single-ended output slew rate for falling edge	$V_{OH(AC)}$	$V_{OL(AC)}$	[$V_{OH(AC)}$ - $V_{OL(AC)}$] / DeltaTFse
Note: Output slew rate is verified by design and characterization, and may not be subject to production test.			

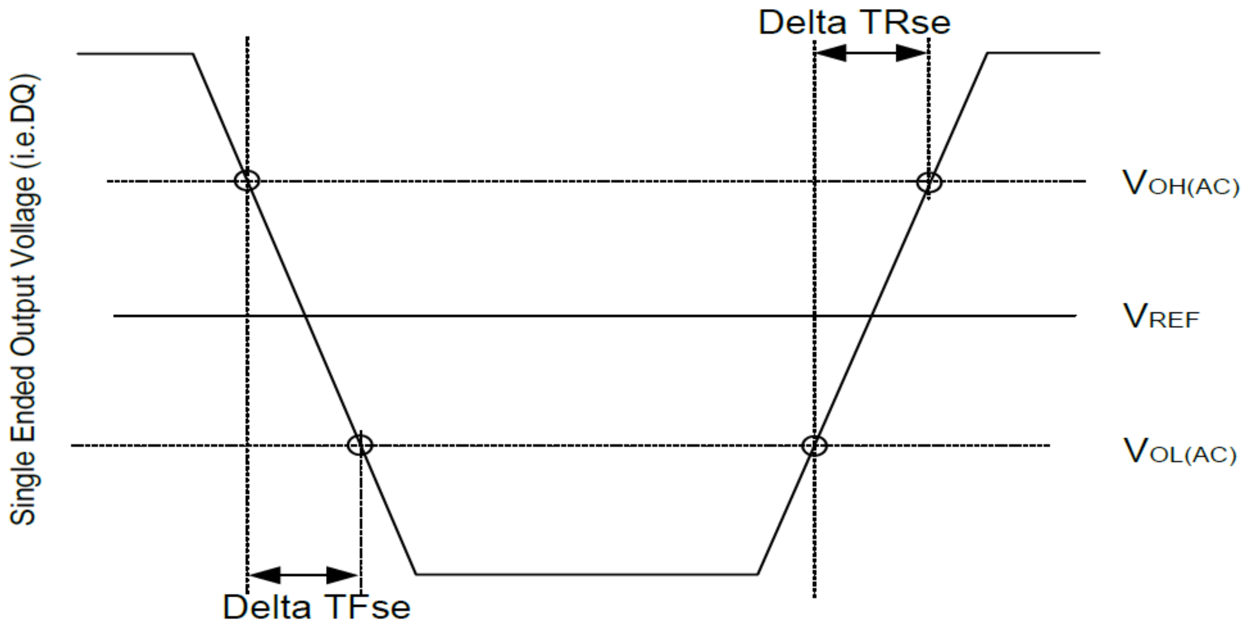


Figure 43: Single Ended Output Slew Rate Definition

Table 14: Output Slew Rate (Single-Ended)

Symbol	Parameter	LPDDR2-800/1066		Units
		Min	Max	
SRQse	Single-ended Output Slew Rate (RON = 40Ω ± 30%)	1.5	3.5	V/nS
SRQse	Single-ended Output Slew Rate (RON = 60Ω ± 30%)	1.0	2.5	V/nS
	Output slew-rate matching Ratio (Pull-up to Pull-down)	0.7	1.4	

Description:
SR: Slew Rate
Q: Query Output (like in DQ, which stands for Data-in, Query-Output)
se: Single-ended Signals

Notes:
1. Measured with output reference load.
2. The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pulldown drivers due to process variation.
3. The output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC).
4. Slew rates are measured under normal SSO conditions, with 1/2 of DQ signals per data byte driving logic high and 1/2 of DQ signals per data byte driving logic low.

9.2.5.4 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLdiff(AC) and VOHdiff(AC) for differential signals as shown in below table and figure.

Table 15: Differential Output Slew Rate Definition

Description	Measured		Defined by
	from	to	
Differential output slew rate for rising edge	VOLdiff(AC)	VOHdiff(AC)	[VOHdiff(AC) - VOLdiff(AC)] / DeltaTRdiff
Differential output slew rate for falling edge	VOHdiff(AC)	VOLdiff(AC)	[VOHdiff(AC) - VOLdiff(AC)] / DeltaTFdiff
Note: Output slew rate is verified by design and characterization, and may not be subject to production test.			

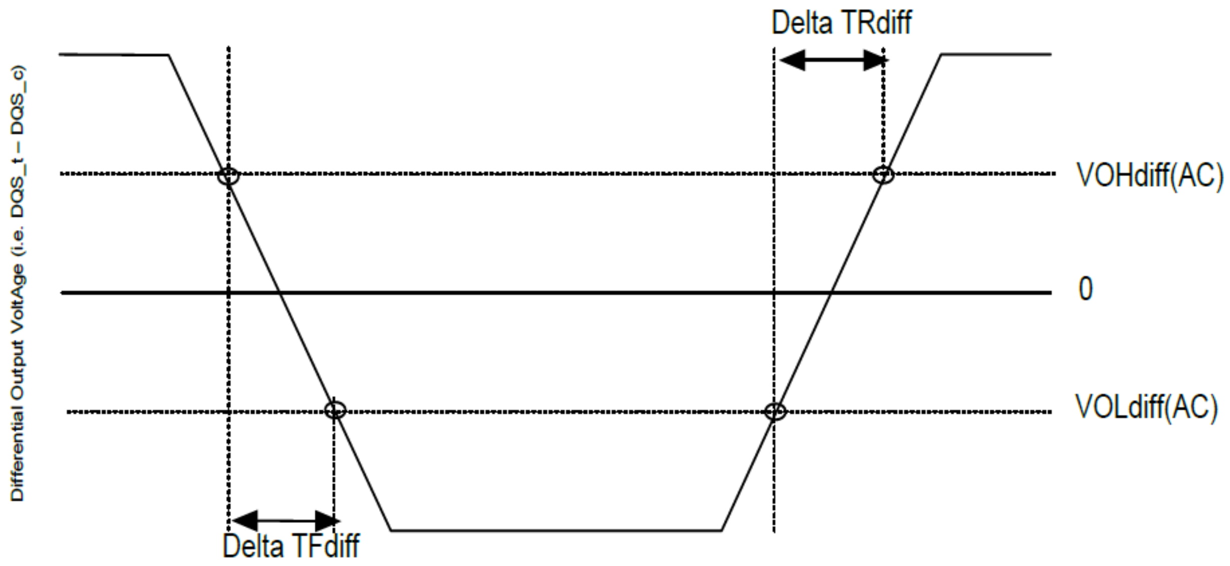


Table 16: Differential Output Slew Rate Definition

Table 17: Differential Output Slew Rate

Symbol	Parameter	LPDDR2-800/1066		Units
		Min	Max	
SRQdiff	Differential Output Slew Rate (RON = 40Ω ± 30%)	3.0	7.0	V/nS
SRQdiff	Differential Output Slew Rate (RON = 60Ω ± 30%)	2.0	5.0	V/nS

Description:
SR: Slew Rate
Q: Query Output (like in DQ, which stands for Data-in, Query-Output)
diff: differential Signals

Notes:
1. Measured with output reference load.
2. The output slew rate for falling and rising edges is defined and measured between VOLdiff(AC) and VOHdiff(AC).
3. Slew rates are measured under normal SSO conditions, with 1/2 of DQ signals per data byte driving logic-high and 1/2 of DQ signals per data byte driving logic-low.

9.2.5.5 Overshoot and Undershoot Specifications

Table 18: AC Overshoot/Undershoot Specification

Parameter		LPDDR2							Unit
		1066	933	800	667	533	400	333	
Maximum peak amplitude allowed for overshoot area. (See figure below)	Max	0.35							V
Maximum peak amplitude allowed for undershoot area. (See figure below)	Max	0.35							V
Maximum area above VDD. (See figure below)	Max	0.15	0.17	0.20	0.24	0.30	0.40	0.48	V-nS
Maximum area below VSS. (See figure below)	Max	0.15	0.17	0.20	0.24	0.30	0.40	0.48	V-nS

(CA0-9, CS_n, CKE, CK_t, CK_c, DQ, DQS_t, DQS_c, DM)

Notes:

1. For CA0-9, CK_t, CK_c, CS_n, and CKE, VDD stands for VDDCA. For DQ, DM, DQS_t, and DQS_c, VDD stands for VDDQ.
2. For CA0-9, CK_t, CK_c, CS_n, and CKE, VSS stands for VSSCA. For DQ, DM, DQS_t, and DQS_c, VSS stands for VSSQ.
3. Maximum peak amplitude values are referenced from actual VDD and VSS values.
4. Maximum area values are referenced from maximum operating VDD and VSS values.

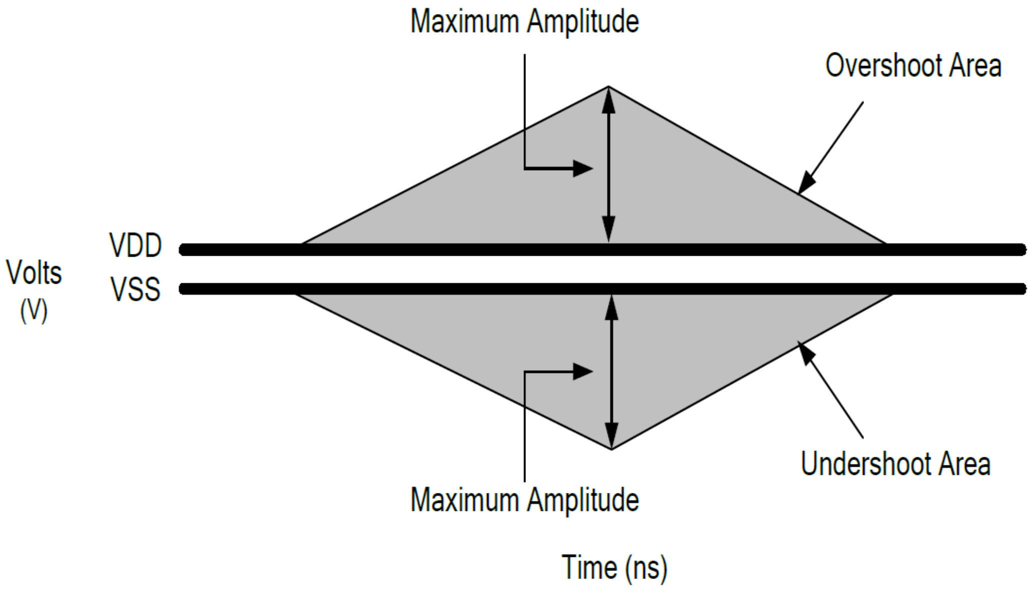


Figure 44: Overshoot and Undershoot Definition

Notes:
1. For CA0-9, CK_t, CK_c, CS_n, and CKE, VDD stands for VDD2. For DQ, DM, DQS_t, and DQS_c, VDD stands for VDDQ.
2. For CA0-9, CK_t, CK_c, CS_n, and CKE, VSS stands for VSS itself. For DQ, DM, DQS_t, and DQS_c, VSS stands for VSSQ.
3. Maximum peak amplitude values are referenced from actual VDD and VSS values.
4. Maximum area values are referenced from maximum operating VDD and VSS values.

9.2.6 Output buffer characteristics

9.2.6.1 HSUL_12 Driver Output Timing Reference Load

These 'Timing Reference Loads' are not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

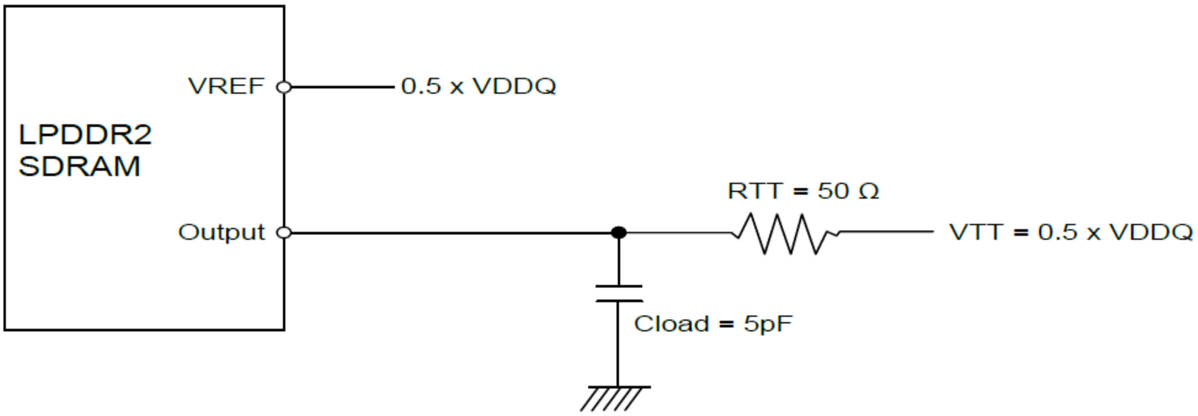


Figure 45: HSUL_12 Driver Output Reference Load for Timing and Slew Rate

Note:
All output timing parameter values (like tDQSCK, tDQSQ, tQHS, tHZ, tRPRE etc.) are reported with respect to this reference load. This reference load is also used to report slew rate.

9.2.6.2 RONPU and RONPD Resistor Definition

$$RONPU = \frac{(VDDQ - Vout)}{ABS(Iout)}$$

Note: This is under the condition that RONPD is turned off

$$RONPD = \frac{Vout}{ABS(Iout)}$$

Note: This is under the condition that RONPU is turned off

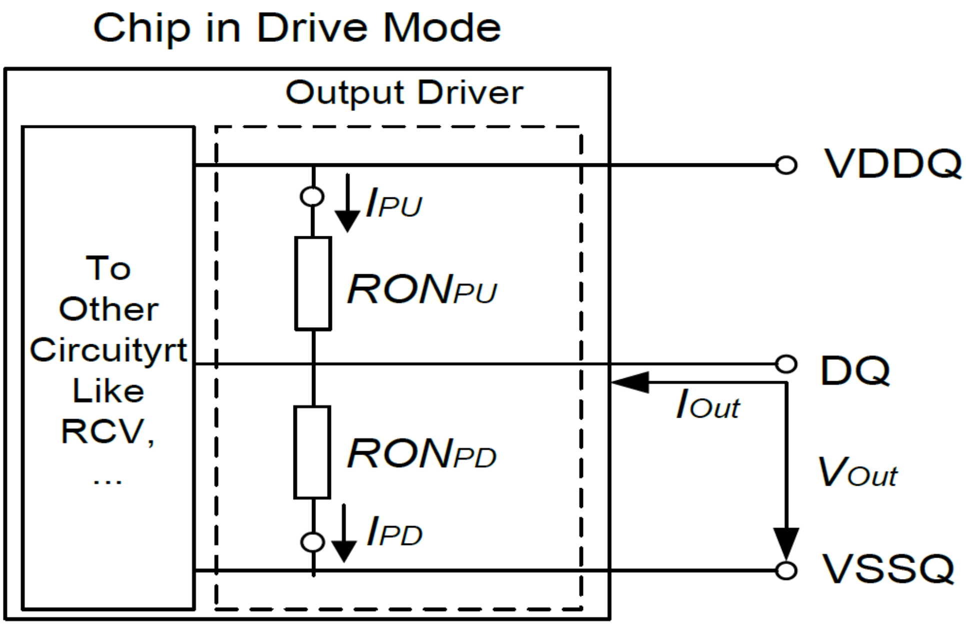


Figure 46: Output Driver Definition of Voltages and Currents

9.2.6.3 RONPU and RONPD Characteristics with ZQ Calibration

Output driver impedance RON is defined by the value of the external reference resistor RZQ. Nominal RZQ is 240Ω.

Table 19: Output Driver DC Electrical Characteristics with ZQ Calibration

RON_{NOM}	Resistor	Vout	Min	Nom	Max	Unit	Note
34.3Ω	RON34PD	0.5 x VDDQ	0.85	1.00	1.15	RZQ/7	1, 2, 3, 4
	RON34PU	0.5 x VDDQ	0.85	1.00	1.15	RZQ/7	1, 2, 3, 4
40.0Ω	RON40PD	0.5 x VDDQ	0.85	1.00	1.15	RZQ/6	1, 2, 3, 4
	RON40PU	0.5 x VDDQ	0.85	1.00	1.15	RZQ/6	1, 2, 3, 4
48.0Ω	RON48PD	0.5 x VDDQ	0.85	1.00	1.15	RZQ/5	1, 2, 3, 4
	RON48PU	0.5 x VDDQ	0.85	1.00	1.15	RZQ/5	1, 2, 3, 4
60.0Ω	RON60PD	0.5 x VDDQ	0.85	1.00	1.15	RZQ/4	1, 2, 3, 4
	RON60PU	0.5 x VDDQ	0.85	1.00	1.15	RZQ/4	1, 2, 3, 4
80.0Ω	RON80PD	0.5 x VDDQ	0.85	1.00	1.15	RZQ/3	1, 2, 3, 4
	RON80PU	0.5 x VDDQ	0.85	1.00	1.15	RZQ/3	1, 2, 3, 4
120.0Ω	RON120PD	0.5 x VDDQ	0.85	1.00	1.15	RZQ/2	1, 2, 3, 4
	RON120PU	0.5 x VDDQ	0.85	1.00	1.15	RZQ/2	1, 2, 3, 4
Mismatch between pull-up and pull-down	MM_{PUPD}		-15.00		+15.00	%	1, 2, 3, 4, 5

Notes:
1. Across entire operating temperature range, after calibration.
2. RZQ = 240Ω.
3. The tolerance limits are specified after calibration with fixed voltage and temperature. For behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
4. Pull-down and pull-up output driver impedances are recommended to be calibrated at 0.5 x VDDQ.
5. Measurement definition for mismatch between pull-up and pull-down: MMPUPD: Measure RONPU and RONPD, both at 0.5 x VDDQ:

$$MMPUPD = \frac{RONPU - RONPD}{RONNOM} \times 100$$

For example, with MMPUPD(max) = 15% and RONPD = 0.85, RONPU must be less than 1.0.

9.2.6.4 Output Driver Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to the tables shown below.

Table 20: Output Driver Sensitivity Definition

Resistor	Vout	Min	Max	Unit	Notes
RON_{PD}	0.5 x VDDQ	85 – (dR ONdT ×|ΔT|) – (dRON d V × |ΔV|)	115 + (dRONdT ×| ΔT|)+(dRONdV × |ΔV|)	%	1, 2
RON_{PU}					

Notes:
1. ΔT = T–T (@calibration), ΔV=V–V(@ calibration).
2. dRONdT and dRONdV are not subject to production test but are verified by design and characterization.

Table 21: Output Driver Temperature and Voltage Sensitivity

Symbol	Parameter	Min	Max	Unit	Note
dRONdT	RON Temperature Sensitivity	0.00	0.75	% / °C	
dRONdV	RON Voltage Sensitivity	0.00	0.20	% / mV	

9.2.6.5 RONPU and RONPD Characteristics without ZQ Calibration

Output driver impedance RON is defined by design and characterization as default setting.

Table 22: Output Driver DC Electrical Characteristics without ZQ Calibration

RON_{NOM}	Resistor	Vout	Min	Nom	Max	Unit	Note
34.3Ω	RON34PD	0.5 x V_{DDQ}	24	34.3	44.6	Ω	1
	RON34PU	0.5 x V_{DDQ}	24	34.3	44.6	Ω	1
40.0Ω	RON40PD	0.5 x V_{DDQ}	28	40	52	Ω	1
	RON40PU	0.5 x V_{DDQ}	28	40	52	Ω	1
48.0Ω	RON48PD	0.5 x V_{DDQ}	33.6	48	62.4	Ω	1
	RON48PU	0.5 x V_{DDQ}	33.6	48	62.4	Ω	1
60.0Ω	RON60PD	0.5 x V_{DDQ}	42	60	78	Ω	1
	RON60PU	0.5 x V_{DDQ}	42	60	78	Ω	1
80.0Ω	RON80PD	0.5 x V_{DDQ}	56	80	104	Ω	1
	RON80PU	0.5 x V_{DDQ}	56	80	104	Ω	1
120.0Ω	RON120PD	0.5 x V_{DDQ}	84	120	156	Ω	1
	RON120PU	0.5 x V_{DDQ}	84	120	156	Ω	1

Note: Across entire operating temperature range, without calibration.

9.2.6.6 RZQ I-V Curve

Table 23: RZQ I-V Curve

Voltage[V]	RON = 240Ω (RZQ)							
	Pull-Down				Pull-Up			
	Current [mA] / RON [Ohms]				Current [mA] / RON [Ohms]			
	default value after ZQReset		With Calibration		default value after ZQReset		With Calibration	
	Min	Max	Min	Max	Min	Max	Min	Max
	[mA]	[mA]	[mA]	[mA]	[mA]	[mA]	[mA]	[mA]
0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
0.05	0.19	0.32	0.21	0.26	-0.19	-0.32	-0.21	-0.26
0.10	0.38	0.64	0.40	0.53	-0.38	-0.64	-0.40	-0.53
0.15	0.56	0.94	0.60	0.78	-0.56	-0.94	-0.60	-0.78
0.20	0.74	1.26	0.79	1.04	-0.74	-1.26	-0.79	-1.04
0.25	0.92	1.57	0.98	1.29	-0.92	-1.57	-0.98	-1.29
0.30	1.08	1.86	1.17	1.53	-1.08	-1.86	-1.17	-1.53
0.35	1.25	2.17	1.35	1.79	-1.25	-2.17	-1.35	-1.79
0.40	1.40	2.46	1.52	2.03	-1.40	-2.46	-1.52	-2.03
0.45	1.54	2.74	1.69	2.26	-1.54	-2.74	-1.69	-2.26
0.50	1.68	3.02	1.86	2.49	-1.68	-3.02	-1.86	-2.49
0.55	1.81	3.30	2.02	2.72	-1.81	-3.30	-2.02	-2.72
0.60	1.92	3.57	2.17	2.94	-1.92	-3.57	-2.17	-2.94
0.65	2.02	3.83	2.32	3.15	-2.02	-3.83	-2.32	-3.15
0.70	2.11	4.08	2.46	3.36	-2.11	-4.08	-2.46	-3.36
0.75	2.19	4.31	2.58	3.55	-2.19	-4.31	-2.58	-3.55
0.80	2.25	4.54	2.70	3.74	-2.25	-4.54	-2.70	-3.74
0.85	2.30	4.74	2.81	3.91	-2.30	-4.74	-2.81	-3.91
0.90	2.34	4.92	2.89	4.05	-2.34	-4.92	-2.89	-4.05
0.95	2.37	5.08	2.97	4.23	-2.37	-5.08	-2.97	-4.23
1.00	2.41	5.20	3.04	4.33	-2.41	-5.20	-3.04	-4.33
1.05	2.43	5.31	3.09	4.44	-2.43	-5.31	-3.09	-4.44
1.10	2.46	5.41	3.14	4.52	-2.46	-5.41	-3.14	-4.52
1.15	2.48	5.48	3.19	4.59	-2.48	-5.48	-3.19	-4.59
1.20	2.50	5.55	3.23	4.65	-2.50	-5.55	-3.23	-4.65

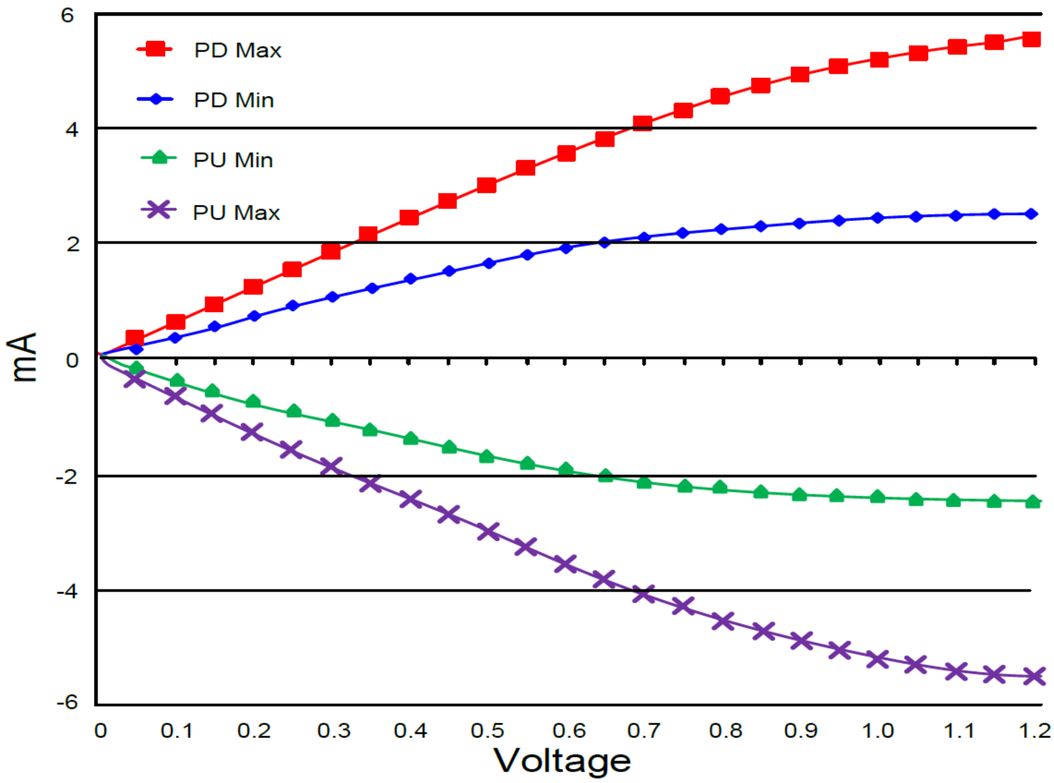


Figure 47: RON = 240 Ohms IV Curve after ZQReset

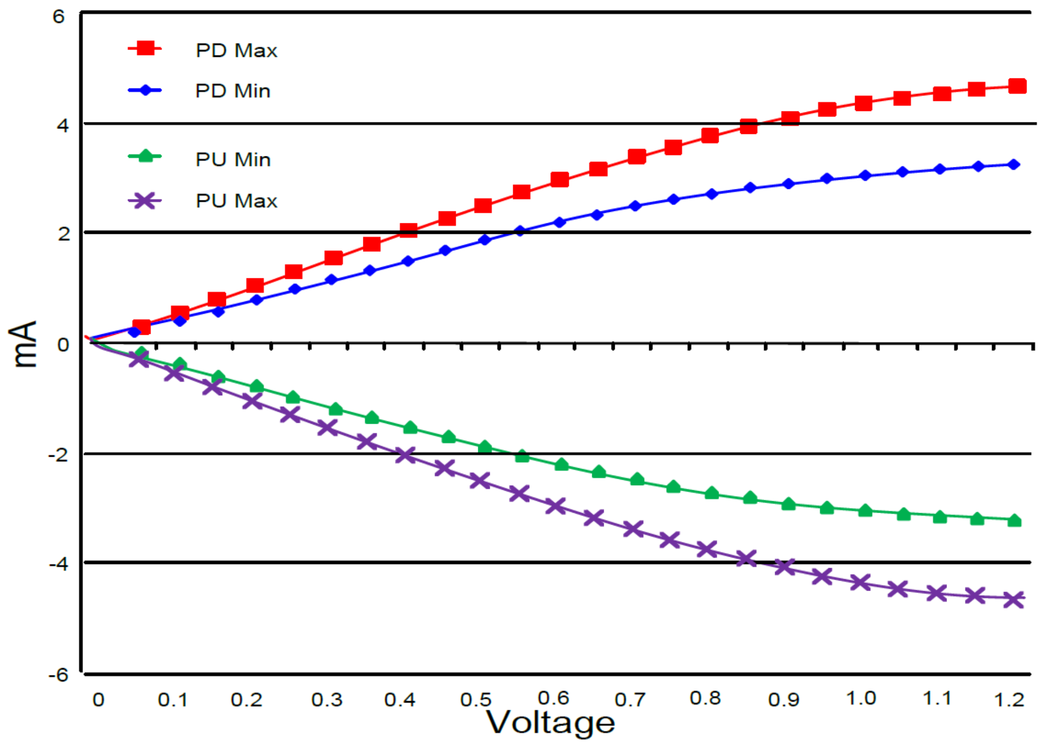


Figure 48: RON = 240 Ohms IV Curve after Calibration

9.2.6.7 Input/Output Capacitance

Table 24: Input/Output Capacitance

Parameter	Symbol	Min	Max	Units	Note
Input capacitance, CK_t and CK_c	C_{CK}	1	2	pF	1, 2
Input capacitance delta, CK_t and CK_c	C_{DCK}	0	0.2	pF	1, 2, 3
Input capacitance, all other input-only pads	C_I	1	2	pF	1, 2, 4
Input capacitance delta, all other input-only pads	C_{DI}	-0.4	0.4	pF	1, 2, 5
Input/output capacitance, DQ, DM, DQS_t, DQS_c	C_{IO}	1.25	2.5	pF	1, 2, 6, 7
Input/output capacitance delta, DQS_t, DQS_c	C_{DDQS}	0	0.25	pF	1, 2, 7, 8
Input/output capacitance delta, DQ, DM	C_{DIO}	-0.5	0.5	pF	1, 2, 7, 9
Input/output capacitance, ZQ Pad	C_{ZQ}	0	2.5	pF	1, 2

(-40°C ≤ Tj ≤ 85°C; VDDQ = 1.14- 1.3V; VDD2 = 1.14-1.3V; VDD1 = 1.7-1.95V, LPDDR2-S4 VDD2 = 1.14-1.3V).

Notes:
1. This parameter applies to die device only (does not include package capacitance).
2. This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA) with VDD1, VDD2, VDDQ, VSS, VSSQ applied and all other pads floating.
3. Absolute value of CCK_t - CCK_c.
4. CI applies to CS_n, CKE, CA0-CA9
5. CDI = CI - 0.5 * (CCK_t + CCK_c).
6. DM loading matches DQ and DQS.
7. MR3 I/O configuration DS OP3-OP0 = 0001B (34.3 Ohm typical).
8. Absolute value of CDQS_t and CDQS_c.
9. CDIO = CIO - 0.5 * (CDQS_t + CDQS_c) in byte lane.

9.3 IDD Specification Parameters and Test Conditions

9.3.1 IDD Measurement Conditions

The following definitions are used within the IDD measurement tables:
LOW: VIN ≤ VIL(DC) MAX
HIGH: VIN ≥ VIH(DC) MIN
STABLE: Inputs are stable at a HIGH or LOW level
SWITCHING: See tables below.

9.3.1.1 Definition of Switching for CA Input Signals

Switching for CA								
	CK_t (RISING) / Ck_C (FALLING)	CK_t (FALLING) / Ck_C (RISING)	CK_t (RISING) / Ck_C (FALLING)	CK_t (FALLING) / Ck_C (RISING)	CK_t (RISING) / Ck_C (FALLING)	CK_t (FALLING) / Ck_C (RISING)	CK_t (RISING) / Ck_C (FALLING)	CK_t (FALLING) / Ck_C (RISING)
Cycle	N		N+1		N+2		N+3	
CS_n	HIGH		HIGH		HIGH		HIGH	
CA0	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA1	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA2	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA3	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA4	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA5	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA6	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA7	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA8	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA9	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH

Notes:
1. CS_n must always be driven HIGH.
2. 50% of CA bus is changing between HIGH and LOW once per clock for the CA bus.
3. The above pattern (N, N+1, N+2, N+3...) is used continuously during IDD measurement for IDD values that require SWITCHING on the CA bus.

9.3.1.2 Definition of Switching for IDD4W

Clock	CKE	CS_n	Clock Cycle Number	Command	CA0-CA2	CA3-CA9	All DQ
Rising	HIGH	LOW	N	Write_Rising	HLL	LHLHLHL	L
Falling	HIGH	LOW	N	Write_Falling	LLL	LLLLLLL	L
Rising	HIGH	HIGH	N + 1	NOP	LLL	LLLLLLL	H
Falling	HIGH	HIGH	N + 1	NOP	HLH	HLHLLHL	L
Rising	HIGH	LOW	N + 2	Write_Rising	HLL	HLHLLHL	H
Falling	HIGH	LOW	N + 2	Write_Falling	LLL	HHHHHHH	H
Rising	HIGH	HIGH	N + 3	NOP	LLL	HHHHHHH	H
Falling	HIGH	HIGH	N + 3	NOP	HLH	LHLHLHL	L

Notes:
1. Data strobe (DQS) is changing between HIGH and LOW every clock cycle.
2. Data masking (DM) must always be driven LOW.
3. The above pattern (N, N+1...) is used continuously during IDD measurement for IDD4W.

9.3.2 IDD Specifications

9.3.2.1 LPDDR2 IDD Specification Parameters and Operating Conditions, -40°C~85°C

Parameter/Condition	Symbol	Power Supply	1066 x32	Unit	Notes
Operating one bank active-precharge Current: tCK=tCK(avg)min; tRC=tRCmin; CKE is High; CS_n is High between valid commands;	$IDD0_{1}$	VDD1	4.2	mA	1
	$IDD0_{2}$	VDD2	30	mA	1
	$IDD0_{IN}$	VDDCA VDDQ	0.2	mA	1,2
Idle power-down standby current: tCK=tCK(avg)min; CKE is Low; CS_n is High; All banks/RBs idle; CA bus inputs are SWITCHING;	$IDD2P_{1}$	VDD1	340	µA	1
	$IDD2P_{2}$	VDD2	1.5	mA	1
	$IDD2P_{IN}$	VDDCA VDDQ	50	µA	1,2
Idle power-down standby current with clock stop: CK_t=Low; CK_c=High; CKE is Low; CS_n is High; All banks/RBs idle; CA bus inputs are STABLE;	$IDD2PS_{1}$	VDD1	340	µA	1
	$IDD2PS_{2}$	VDD2	1.5	mA	1
	$IDD2PS_{IN}$	VDDCA VDDQ	50	µA	1,2
Idle non power-down standby current: tCK=tCK(avg)min; CKE is High; CS_n is High; All banks/RBs idle; CA bus inputs are SWITCHING;	$IDD2N_{1}$	VDD1	400	µA	1
	$IDD2N_{2}$	VDD2	15.2	mA	1
	$IDD2N_{IN}$	VDDCA VDDQ	100	µA	1,2
Idle non power-down standby current with clock stop: CK_t=Low; CK_c=High; CKE is High; CS_n is High; All banks/RBs idle; CA bus inputs are STABLE;	$IDD2NS_{1}$	VDD1	400	µA	1
	$IDD2NS_{2}$	VDD2	13.3	mA	1
	$IDD2NS_{IN}$	VDDCA VDDQ	100	µA	1,2
Active Power down standby current: tCK=tCK(avg)min; CKE is Low; CS_n is High; One bank/RB active; CA bus inputs are SWITCHING;	$IDD3P_{1}$	VDD1	680	µA	1
	$IDD3P_{2}$	VDD2	3	mA	1
	$IDD3P_{IN}$	VDDCA VDDQ	50	µA	1,2
Active Power down standby current with clock stop: CK_t= Low; CK_c= High; CKE is Low; CS_n is High; One bank/RB active; CA bus inputs are STABLE;	$IDD3PS_{1}$	VDD1	680	µA	1
	$IDD3PS_{2}$	VDD2	3	mA	1
	$IDD3PS_{IN}$	VDDCA VDDQ	50	µA	1,2
Active non Power down standby current: tCK=tCK(avg)min; CKE is High; CS_n is High; One bank/RB active; CA bus inputs are SWITCHING;	$IDD3N_{1}$	VDD1	710	µA	1
	$IDD3N_{2}$	VDD2	17.1	mA	1
	$IDD3N_{IN}$	VDDCA VDDQ	100	µA	1,2
Active non Power down standby current with clock stop: CK_t= Low; CK_c= High; CKE is High; CS_n is High; One bank/RB active; CA bus inputs are STABLE;	$IDD3NS_{1}$	VDD1	710	µA	1
	$IDD3NS_{2}$	VDD2	15.3	mA	1
	$IDD3NS_{IN}$	VDDCA VDDQ	100	µA	1,2
Operating burst read current: tCK=tCK(avg)min; CS_n is High between valid commands; One bank/RB active BL=4; RL=RLmin	$IDD4R_{1}$	VDD1	750	µA	1
	$IDD4R_{2}$	VDD2	155	mA	1
	$IDD4R_{IN}$	VDDQ	/	mA	1

Operating burst write current: tCK=tCK(avg)min; CS_n is High between valid commands; One bank/RB active	IDD4W$_{1}$	VDD1	750	μA	1
	IDD4W$_{2}$	VDD2	172	mA	1
	IDD4W$_{IN}$	VDDCA VDDQ	39.5	mA	1

All bank Refresh Burst current:
tCK=tCK(avg)min;
CKE is High between valid commands;
tRC=tRFCabmin;
	IDD5$_{1}$	VDD1	33	mA	1

	IDD5$_{2}$	VDD2	81.8	mA	1
	IDD5$_{IN}$	VDDCA VDDQ	100	μA	1,2

All bank Refresh average current:
tCK=tCK(avg)min;
CKE is High between valid commands;
tRC=tREFI;
	IDDAB5$_{1}$	VDD1	900	μA	1

	IDD5AB$_{2}$	VDD2	21.1	mA	1
	IDD5AB$_{IN}$	VDDCA VDDQ	100	μA	1,2
Deep Power down current: CK_t=Low; CK_c=High; CKE is Low; CA bus inputs are STABLE; Data bus inputs are STABLE;	IDD8$_{1}$	VDD1	20	μA	1
	IDD8$_{2}$	VDD2	50	μA	1
	IDD8$_{IN}$	VDDCA VDDQ	50	μA	1,2

Notes:
1. IDD values published are the maximum of the distribution of the arithmetic mean.
2. Measured currents are the summation of VDDQ and VDD2.
3. IDD current specifications are tested after the device is properly initialized.

9.3.2.2 IDD6 Partial Array Self-Refresh Current, 85°C

Parameter		Symbol	Power Supply	400MHz	533MHz	Condition	Unit
IDD6 partial array Self-Refresh Current	Full Array	IDD6$_{1}$	VDD1	1.31	1.31	Self Refresh Current: CK_t=Low; CK_c=High; CKE is Low; CA bus inputs are STABLE; Data bus inputs are STABLE;	mA
		IDD6$_{2}$	VDD2	2.76	2.76		
		IDD6$_{IN}$	VDDCA/VDDQ	0.05	0.05		

Notes:
1. LPDDR2-S4B SDRAM uses the same PASR scheme & IDD6 current value categorization as LPDDR2 (JESD209).
2. IDD values published are the maximum of the distribution of the arithmetic mean.
3. Maximum 1x Self-Refresh rate

9.4 Clock Specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input clocks violating the min/max values may result in malfunction of the LPDDR2 device.

9.4.1 Definition for $t_{CK(avg)}$ and n_{CK}

tCK(avg) is calculated as the average clock period across any consecutive 200 cycle window, where each clock period is calculated from rising edge to rising edge.

$$tCK(avg) = \left[\sum_{j=1}^{N} tCK_j\right] / N \qquad where \quad N = 200$$

Unit ‘tCK(avg)’ represents the actual clock average tCK(avg) of the input clock under operation. Unit ‘nCK’ represents one clock cycle of the input clock, counting the actual clock edges.

tCK(avg) may change by up to ± 1% within a 100 clock cycle window, provided that all jitter and timing specs are met.

9.4.2 Definition for $t_{CK(abs)}$

tCK(abs) is defined as the absolute clock period, as measured from one rising edge to the next consecutive rising edge.

tCK(abs) is not subject to production test.

9.4.3 Definition for $t_{CH(avg)}$ and $t_{CL(avg)}$

tCH(avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

$$tCH(avg) = \left[\sum_{j=1}^{N} tCH_j\right] / (N \times tCK(avg)) \qquad where \quad N = 200$$

tCL(avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$tCL(avg) = \left[\sum_{j=1}^{N} tCL_j\right] / (N \times tCK(avg)) \qquad where \quad N = 200$$

9.4.4 Definition for $t_{JIT(per)}$

tJIT(per) is the single period jitter defined as the largest deviation of any signal tCK from tCK(avg).
tJIT(per) = Min/max of {tCKi - tCK(avg) where i = 1 to 200}.
tJIT(per),act is the actual clock jitter for a given system.
tJIT(per),allowed is the specified allowed clock period jitter.
tJIT(per) is not subject to production test.

9.4.5 Definition for $t_{JIT(cc)}$

tJIT(cc) is defined as the absolute difference in clock period between two consecutive clock cycles.
tJIT(cc) = Max of |{tCKi +1 - tCKi}|.
tJIT(cc) defines the cycle to cycle jitter.
tJIT(cc) is not subject to production test.

9.4.6 Definition for $t_{ERR(nper)}$

tERR(nper) is defined as the cumulative error across n multiple consecutive cycles from tCK(avg).
tERR(nper),act is the actual clock jitter over n cycles for a given system.
tERR(nper),allowed is the specified allowed clock period jitter over n cycles.
tERR(nper) is not subject to production test.

$$tERR(nper) = \left[\sum_{j=i}^{i+n-1} tCK_j\right] - n \times tCK(avg)$$

tERR(nper),min can be calculated by the formula shown below:

$$tERR(nper), min = (1 + 0.68LN(n)) \times tJIT(per), min$$

tERR(nper),max can be calculated by the formula shown below:

$$tERR(nper), max = (1 + 0.68LN(n)) \times tJIT(per), max$$

Using these equations, tERR(nper) tables can be generated for each tJIT(per),act value.

9.4.7 Definition for Duty Cycle Jitter $t_{JIT(duty)}$

tJIT(duty) is defined with absolute and average specification of tCH / tCL.

tJIT(duty),min = MIN((tCH(abs),min – tCH(avg),min),(tCL(abs),min – tCL(avg),min)) x tCK(avg)

tJIT(duty),max = MAX((tCH(abs),max – tCH(avg),max),(tCL(abs),max – tCL(avg),max)) x tCK(avg)

9.4.8 Definition for $t_{CK(abs)}$, $t_{CH(abs)}$) and $t_{CL(abs)}$

These parameters are specified per their average values, however it is understood that the following relationship between the average timing and the absolute instantaneous timing holds at all times.

Table 25: Definition for tCK(abs), tCH(abs), and tCL(abs)

Parameter	Symbol	Min	Unit
Absolute Clock Period	tCK(abs)	tCK(avg),min + tJIT(per),min	PS
Absolute Clock HIGH Pulse Width	tCH(abs)	tCH(avg),min + tJIT(duty),min / tCK(avg)min	tCK(avg)
Absolute Clock LOW Pulse Width	tCL(abs)	tCL(avg),min + tJIT(duty),min / tCK(avg)min	tCK(avg)

Notes:
1. tCK(avg),min is expressed is pS for this table.
2. tJIT(duty),min is a negative value.

9.5 Period Clock Jitter

LPDDR2 devices can tolerate some clock period jitter without core timing parameter de-rating. This section describes device timing requirements in the presence of clock period jitter (tJIT(per)) in excess of the values found in section 9.7.1 “LPDDR2 AC Timing” table and how to determine cycle time de-rating and clock cycle de-rating.

9.5.1 Clock Period Jitter Effects on Core Timing Parameters

(tRCD, tRP, tRTP, tWR, tWRA, tWTR, tRC, tRAS, tRRD, tFAW)

Core timing parameters extend across multiple clock cycles. Period clock jitter will impact these parameters when measured in numbers of clock cycles. When the device is operated with clock jitter within the specification limits, the LPDDR2 device is characterized and verified to support tnPARAM = RU{tPARAM / tCK(avg)}.

When the device is operated with clock jitter outside specification limits, the number of clocks or tCK(avg) may need to be increased based on the values for each core timing parameter.

9.5.1.1 Cycle Time De-rating for Core Timing Parameters

For a given number of clocks (tnPARAM), for each core timing parameter, average clock period (tCK(avg)) and actual cumulative period error (tERR(tnPARAM),act) in excess of the allowed cumulative period error (tERR(tnPARAM),allowed), the equation below calculates the amount of cycle time de-rating (in nS) required if the equation results in a positive value for a core timing parameter (tCORE).

$$CycleTimeDerating = MAX\left\{\left(\frac{tPARAM + tERR(tnPARAM),act - tERR(tnPARAM),allowed}{tnPARAM} - tCK(avg)\right), 0\right\}$$

A cycle time derating analysis should be conducted for each core timing parameter. The amount of cycle time derating required is the maximum of the cycle time de-ratings determined for each individual core timing parameter.

9.5.1.2 Clock Cycle De-rating for Core Timing Parameters

For a given number of clocks (tnPARAM) for each core timing parameter, clock cycle de-rating should be specified with amount of period jitter (tJIT(per)).

For a given number of clocks (tnPARAM), for each core timing parameter, average clock period (tCK(avg)) and actual cumulative period error (tERR(tnPARAM),act) in excess of the allowed cumulative period error (tERR(tnPARAM),allowed), the equation below calculates the clock cycle derating (in clocks) required if the equation results in a positive value for a core timing parameter (tCORE).

$$ClockCycleDerating = RU\left\{\frac{tPARAM + tERR(tnPARAM),act - tERR(tnPARAM),allowed}{tCK(avg)}\right\} - tnPARAM$$

A clock cycle de-rating analysis should be conducted for each core timing parameter.

9.5.2 Clock Jitter Effects on Command/Address Timing Parameters

(tIS, tIH, tISCKE, tIHCKE, tISb, tIHb, tISCKEb, tIHCKEb)

These parameters are measured from a command/address signal (CKE, CS, CA0 - CA9) transition edge to its respective clock signal (CK_t/CK_c) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), as the setup and hold are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values shall be met.

9.5.3 Clock Jitter Effects on Read Timing Parameters

9.5.3.1 tRPRE

When the device is operated with input clock jitter, tRPRE needs to be de-rated by the actual period jitter (tJIT(per), act, max) of the input clock in excess of the allowed period jitter (tJIT(per),allowed, max). Output de-ratings are relative to the input clock.

$$tRPRE(min,\ derated) = 0.9 - \left(\frac{tJIT(per)\ ,act\ ,max\ - tJIT\ (per\ ),allowed\ \ ,max}{tCK\ (avg\ )} \right)$$

For example,
if the measured jitter into a LPDDR2-800 device has tCK(avg) = 2500 pS, tJIT(per),act, min = -172 pS and tJIT(per),act, max = + 193 pS, then
tRPRE, min, derated = 0.9 - (tJIT(per), act, max - tJIT(per),allowed, max)/tCK(avg) = 0.9 - (193 - 100)/2500= .8628 tCK(avg)

9.5.3.2 tLZ(DQ), tHZ(DQ), tDQSCK, tLZ(DQS), tHZ(DQS)

These parameters are measured from a specific clock edge to a data signal (DMn, DQm: n=0,1,2,3. m=0–31) transition and will be met with respect to that clock edge. Therefore, they are not affected by the amount of clock jitter applied (i.e. tJIT(per).

9.5.3.3 tQSH, tQSL

These parameters are affected by duty cycle jitter which is represented by tCH(abs)min and tCL(abs)min.
tQSH(abs)min = tCH(abs)min – 0.05
tQSL(abs)min = tCL(abs)min – 0.05
These parameters determine absolute Data-Valid window at the LPDDR2 device pad.
Absolute min data-valid window @ LPDDR2 device pad = min { (tQSH(abs)min * tCK(avg)min – tDQSQmax – tQHSmax) , (tQSL(abs)min * tCK(avg)min – tDQSQmax – tQHSmax) }
This minimum data-valid window shall be met at the target frequency regardless of clock jitter.

9.5.3.4 tRPST

tRPST is affected by duty cycle jitter which is represented by tCL(abs). Therefore tRPST(abs)min can be specified by tCL(abs)min.
tRPST(abs)min = tCL(abs)min – 0.05 = tQSL(abs)min

9.5.4 Clock Jitter Effects on Write Timing Parameters

9.5.4.1 tDS, tDH

These parameters are measured from a data signal (DMn, DQm.: n=0,1,2,3. m=0–31) transition edge to its respective data strobe signal (DQSn_t, DQSn_c: n=0,1,2,3) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), as the setup and hold are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values shall be met.

9.5.4.2 tDSS, tDSH

These parameters are measured from a data strobe signal (DQSx_t, DQSx_c) crossing to its respective clock signal (CK_t/CK_c) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), as the setup and hold are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values shall be met.

9.5.4.3 tDQSS

This parameter is measured from a data strobe signal (DQSx_t, DQSx_c) crossing to the subsequent clock signal (CK_t/CK_c) crossing. When the device is operated with input clock jitter, this parameter needs to be de-rated by the actual period jitter tJIT(per),act of the input clock in excess of the allowed period jitter tJIT(per),allowed.

$$tDQSS(min, derated) = 0.75 - \frac{tJIT(per), act, min - tJIT(per), allowed, min}{tCK(avg)}$$

$$tDQSS(max, derated) = 1.25 - \frac{tJIT(per), act, max - tJIT(per), allowed, max}{tCK(avg)}$$

For example,
if the measured jitter into a LPDDR2-800 device has tCK(avg) = 2500 pS, tJIT(per), act, min = -172 pS and tJIT(per),act ,max = + 193 pS, then
tDQSS,(min, derated) = 0.75 - (tJIT(per), act, min - tJIT(per), allowed, min)/tCK(avg) = 0.75 - (-172 + 100)/2500 = .7788 tCK(avg)
and
tDQSS,(max, derated) = 1.25 - (tJIT(per), act, max - tJIT(per), allowed, max)/tCK(avg) = 1.25 - (193 - 100)/2500 = 1.2128 tCK(avg)

9.6 Refresh Requirements

9.6.1 Refresh Requirement Parameters

Parameter		Symbol	Value	Unit
Number of Banks			4	
Refresh Window				
T_{CASE} ≦ 85 ℃		tREFW	32	ms
Required number of REFRESH commands (min)		R	4,096	
Average time between REFRESH commands (for reference only) T_{CASE} ≦ 85 ℃	REFab	tREFI	7.8	us
	REFpb	tREFIpb	(REFpb not allowed below 1Gb.)	us
Refresh Cycle time		tRFCab	90	ns
Pre Bank Refresh Cycle time		tRFCpb	NA	ns
Burst Refresh Window = 4 x 8 x t_{RFCab}		tREFBW	2.88	us

9.7 AC Timings

9.7.1 LPDDR2 AC Timing

(Note 6 apply to the entire table)

Parameter	Symbol	min / max	min tCK	Data Rate							Unit
				1066	933	800	667	533	400	333	
Max. Frequency[*4]		~		533	466	400	333	266	200	166	MHz
Clock Timing											
Average Clock Period	tCK(avg)	MIN		1.875	2.15	2.5	3	3.75	5	6	nS
		MAX		100							
Average high pulse width	tCH(avg)	MIN		0.45							tCK(avg)
		MAX		0.55							
Average low pulse width	tCL(avg)	MIN		0.45							tCK(avg)
		MAX		0.55							
Absolute Clock Period	tCK(abs)	MIN		tCK(avg)min + tJIT(per)min							pS
Absolute clock HIGH pulse width (with allowed jitter)	tCH(abs), allowed	MIN		0.43							tCK(avg)
		MAX		0.57							
Absolute clock LOW pulse width (with allowed jitter)	tCL(abs), (allowed)	MIN		0.43							tCK(avg)
		MAX		0.57							
Clock Period Jitter (with allowed jitter)	tJIT(per), (allowed)	MIN		-90	-95	-100	-110	-120	-140	-150	pS
		MAX		90	95	100	110	120	140	150	
Maximum Clock Jitter between two consecutive clock cycles (with allowed jitter)	tJIT(cc), allowed	MAX		180	190	200	220	240	280	300	pS
Duty cycle Jitter (with allowed jitter)	tJIT(duty), allowed	MIN		MIN ((tCH(abs),min - tCH(avg),min), (tCL(abs),min - tCL(avg),min)) * tCK(avg)							pS
		MAX		MAX ((tCH(abs),max - tCH(avg),max), (tCL(abs),max - tCL(avg),max)) * tCK(avg)							pS
Cumulative error across 2 cycles	tERR(2per), (allowed)	MIN		-132	-140	-147	-162	-177	-206	-221	pS
		MAX		132	140	147	162	177	206	221	
Cumulative error across 3 cycles	tERR(3per), (allowed)	MIN		-157	-166	-175	-192	-210	-245	-262	pS
		MAX		157	166	175	192	210	245	262	
Cumulative error across 4 cycles	tERR(4per), (allowed)	MIN		-175	-185	-194	-214	-233	-272	-291	pS
		MAX		175	185	194	214	233	272	291	
Cumulative error across 5 cycles	tERR(5per), (allowed)	MIN		-188	-199	-209	-230	-251	-293	-314	pS
		MAX		188	199	209	230	251	293	314	
Cumulative error across 6 cycles	tERR(6per), (allowed)	MIN		-200	-211	-222	-244	-266	-311	-333	pS
		MAX		200	211	222	244	266	311	333	
Cumulative error across 7 cycles	tERR(7per), (allowed)	MIN		-209	-221	-232	-256	-279	-325	-348	pS
		MAX		209	221	232	256	279	325	348	
Cumulative error across 8 cycles	tERR(8per), (allowed)	MIN		-217	-229	-241	-266	-290	-338	-362	pS
		MAX		217	229	241	266	290	338	362	
Cumulative error across 9 cycles	tERR(9per), (allowed)	MIN		-224	-237	-249	-274	-299	-349	-374	pS
		MAX		224	237	249	274	299	349	374	
Cumulative error across 10 cycles	tERR(10per), (allowed)	MIN		-231	-244	-257	-282	-308	-359	-385	pS
		MAX		231	244	257	282	308	359	385	
Cumulative error across 11 cycles	tERR(11per), (allowed)	MIN		-237	-250	-263	-289	-316	-368	-395	pS
		MAX		237	250	263	289	316	368	395	
Cumulative error across 12 cycles	tERR(12per), (allowed)	MIN		-242	-256	-269	-296	-323	-377	-403	pS
		MAX		242	256	269	296	323	377	403	
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR(nper), (allowed)	MIN		tERR(nper),allowed,min = (1 + 0.68ln(n)) * tJIT(per),allowed,min							pS
		MAX		tERR(nper),allowed,max = (1 + 0.68ln(n)) * tJIT(per),allowed,max							

Parameter	Symbol	min / max	min tCK	Data Rate 1066	933	800	667	533	400	333	Unit
ZQ Calibration Parameters											
Initialization Calibration Time	tZQINIT	MIN		1							μS
Full Calibration Time	tZQCL	MIN	6	360							nS
Short Calibration Time	tZQCS	MIN	6	90							nS
Calbration Reset Time	tZQRESET	MIN	3	50							nS
Read Parameters[*11]											
DQS output access time from CK_t/CK_c	tDQSCK	MIN		2500							pS
		MAX		5500							
DQSCK Delta Short[*15]	tDQSCKDS	MAX		330	380	450	540	670	900	1080	pS
DQSCK Delta Medium[*16]	tDQSCKDM	MAX		680	780	900	1050	1350	1800	1900	pS
DQSCK Delta Long[*17]	tDQSCKDL	MAX		920	1050	1200	1400	1800	2400	-	pS
DQS - DQ skew	tDQSQ	MAX		200	220	240	280	340	400	500	pS
Data hold skew factor	tQHS	MAX		230	260	280	340	400	480	600	pS
DQS Output High Pulse Width	tQSH	MIN		tCH(abs) - 0.05							tCK(avg)
DQS Output Low Pulse Width	tQSL	MIN		tCL(abs) - 0.05							tCK(avg)
Data Half Period	tQHP	MIN		min(tQSH, tQSL)							tCK(avg)
DQ / DQS output hold time from DQS	tQH	MIN		tQHP - tQHS							pS
Read preamble[*12,*13]	tRPRE	MIN		0.9							tCK(avg)
Read postamble[*12,*14]	tRPST	MIN		tCL(abs) - 0.05							tCK(avg)
DQS low-Z from clock[*12]	tLZ(DQS)	MIN		tDQSCK(MIN) - 300							pS
DQ low-Z from clock[*12]	tLZ(DQ)	MIN		tDQSCK(MIN) - (1.4 * tQHS(MAX))							pS
DQS high-Z from clock[*12]	tHZ(DQS)	MAX		tDQSCK(MAX) - 100							pS
DQ high-Z from clock[*12]	tHZ(DQ)	MAX		tDQSCK(MAX) + (1.4 * tDQSQ(MAX))							pS
Write Parameters[*11]											
DQ and DM input hold time (Vref based)	tDH	MIN		210	235	270	350	430	480	600	pS
DQ and DM input setup time (Vref based)	tDS	MIN		210	235	270	350	430	480	600	pS
DQ and DM input pulse width	tDIPW	MIN		0.35							tCK(avg)
Write command to 1st DQS latching transition	tDQSS	MIN		0.75							tCK(avg)
		MAX		1.25							
DQS input high-level width	tDQSH	MIN		0.4							tCK(avg)
DQS input low-level width	tDQSL	MIN		0.4							tCK(avg)
DQS falling edge to CK setup time	tDSS	MIN		0.2							tCK(avg)
DQS falling edge hold time from CK	tDSH	MIN		0.2							tCK(avg)
Write postamble	tWPST	MIN		0.4							tCK(avg)
Write preamble	tWPRE	MIN		0.35							tCK(avg)
CKE Input Parameters											
CKE min. pulse width (high and low pulse width)	tCKE	MIN	3	3							tCK(avg)
CKE input setup time	tISCKE[*2]	MIN		0.25							tCK(avg)
CKE input hold time	tIHCKE[*3]	MIN		0.25							tCK(avg)

Parameter	Symbol	min / max	min tCK	Data Rate							Unit
				1066	933	800	667	533	400	333	
Command Address Input Parameters[*11]											
Address and control input setup time (Vref based)	tIS[*1]	MIN		220	250	290	370	460	600	740	pS
Address and control input hold time (Vref based)	tIH[*1]	MIN		220	250	290	370	460	600	740	pS
Address and control input pulse width	tIPW	MIN		0.40							tCK(avg)
Boot Parameters (10 MHz - 55 MHz)[*5, 7, 8]											
Clock Cycle Time	tCKb	MAX		100							nS
		MIN		18							
CKE Input Setup Time	tISCKEb	MIN		2.5							nS
CKE Input Hold Time	tIHCKEb	MIN		2.5							nS
Address & Control Input Setup Time	tISb	MIN		1150							pS
Address & Control Input Hold Time	tIHb	MIN		1150							pS
DQS Output Data Access Time from CK_t/CK_c	tDQSCKb	MIN		2.0							nS
		MAX		10.0							
Data Strobe Edge to Ouput Data Edge tDQSQb - 1.2	tDQSQb	MAX		1.2							nS
Data Hold Skew Factor	tQHSb	MAX		1.2							nS
Mode Register Parameters											
MODE REGISTER Write command period	tMRW	MIN	5	5							tCK(avg)
Mode Register Read command period	tMRR	MIN	2	2							tCK(avg)
LPDDR2 SDRAM Core Parameters[*9]											
Read Latency	RL	MIN	3	8	7	6	5	4	3	3	tCK(avg)
Write Latency	WL	MIN	1	4	4	3	2	2	1	1	tCK(avg)
ACTIVE to ACTIVE command period	tRC	MIN		tRAS + tRPab (with all-bank Precharge) tRAS + tRPpb (with per-bank Precharge)							nS
CKE min. pulse width during Self-Refresh (low pulse width during Self-Refresh)	tCKESR	MIN	3	15							nS
Self refresh exit to next valid command delay	tXSR	MIN	2	tRFCab + 10							nS
Exit power down to next valid command delay	tXP	MIN	2	7.5							nS
CAS to CAS delay	tCCD	MIN	2	2							tCK(avg)
Internal Read to Precharge command delay	tRTP	MIN	2	7.5							nS
RAS to CAS Delay	tRCD	Fast	3	15							nS
Row Precharge Time (single bank)	tRPpb	Fast	3	15							nS
Row Precharge Time (all banks)	tRPab 4-bank	Fast	3	15							nS
Row Active Time	tRAS	MIN	3	42							nS
		MAX	-	70							µs
Write Recovery Time	tWR	MIN	3	15							nS
Internal Write to Read Command Delay	tWTR	MIN	2	7.5					10		nS
Active bank A to Active bank B	tRRD	MIN	2	10							nS
Four Bank Activate Window	tFAW	MIN	8	50						60	nS
Minimum Deep Power Down Time	tDPD	MIN		500							µS

Parameter	Symbol	min / max	min tCK	Data Rate							Unit
				1066	933	800	667	533	400	333	
LPDDR2 Temperature De-Rating											
tDQSCK De-Rating	tDQSCK (Derated)	MAX		5620	6000						pS
Core Timings Temperature De-Rating	tRCD (Derated)	MIN		tRCD + 1.875							nS
	tRC (Derated)	MIN		tRC + 1.875							nS
	tRAS (Derated)	MIN		tRAS + 1.875							nS
	tRP (Derated)	MIN		tRP + 1.875							nS
	tRRD (Derated)	MIN		tRRD + 1.875							nS

Notes:
1. Input set-up/hold time for signal (CA[0:n], CS_n).
2. CKE input setup time is measured from CKE reaching high/low voltage level to CK_t/CK_c crossing.
3. CKE input hold time is measured from CK_t/CK_c crossing to CKE reaching high/low voltage level.
4. Frequency values are for reference only. Clock cycle time (tCK) shall be used to determine device capabilities.
5. To guarantee device operation before the LPDDR2 device is configured a number of AC boot timing parameters are defined in this table. Boot parameter symbols have the letter b appended, e.g. tCK during boot is tCKb.
6. Frequency values are for reference only. Clock cycle time (tCK or tCKb) shall be used to determine device capabilities.
7. The SDRAM will set some Mode register default values upon receiving a RESET (MRW) command as specified in “Mode Register Definition”.
8. The output skew parameters are measured with Ron default settings into the reference load.
9. The min tCK column applies only when tCK is greater than 6nS for LPDDR2-S4 devices.
10. All AC timings assume an input slew rate of 1V/nS.
11. Read, Write, and Input Setup and Hold values are referenced to Vref.
12. For low-to-high and high-to-low transitions, the timing reference will be at the point when the signal crosses VTT. tHZ and tLZ transitions occur in the same access time (with respect to clock) as valid data transitions. These parameters are not referenced to a specific voltage level but to the time when the device output is no longer driving (for tRPST, tHZ(DQS) and tHZ(DQ)), or begins driving (for tRPRE, tLZ(DQS), tLZ(DQ)). Below “HSUL_12 Driver Output Reference Load for Timing and Slew Rate” figure shows a method to calculate the point when device is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.

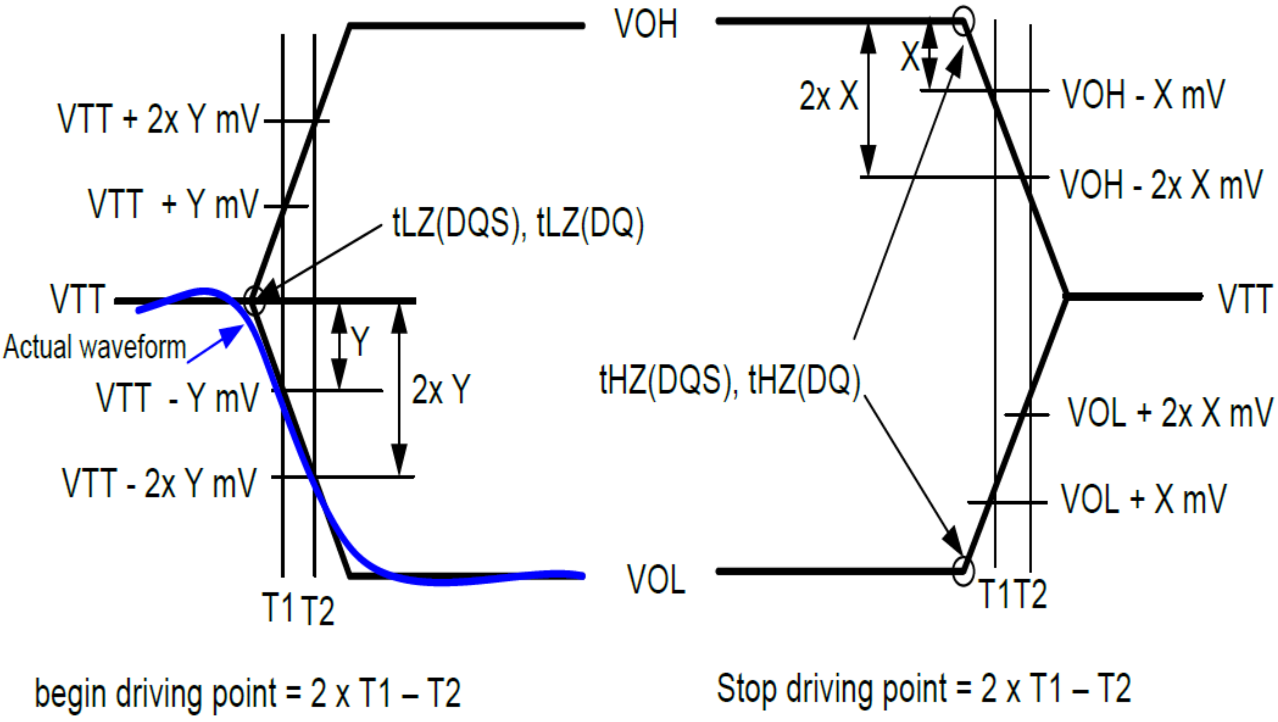


Figure 49: HSUL_12 Driver Output Reference Load for Timing and Slew Rate

The parameters tLZ(DQS), tLZ(DQ), tHZ(DQS), and tHZ(DQ) are defined as single-ended. The timing parameters tRPRE and tRPST are determined from the differential signal DQS_t-DQS_c.

13. Measured from the start driving of DQS_t - DQS_c to the start driving the first rising strobe edge.
14. Measured from the from start driving the last falling strobe edge to the stop driving DQS_t , DQS_c.
15. tDQSCKDS is the absolute value of the difference between any two tDQSCK measurements (within a byte lane) within a contiguous sequence of bursts within a 160nS rolling window. tDQSCKDS is not tested and is guaranteed by design. Temperature drift in the system is < 10°C/s. Values do not include clock jitter.
16. tDQSCKDM is the absolute value of the difference between any two tDQSCK measurements (within a byte lane) within a 1.6µs rolling window. tDQSCKDM is not tested and is guaranteed by design. Temperature drift in the system is < 10°C/s. Values do not include clock jitter.
17. tDQSCKDL is the absolute value of the difference between any two tDQSCK measurements (within a byte lane) within a 32mS rolling window. tDQSCKDL is not tested and is guaranteed by design. Temperature drift in the system is < 10°C/s. Values do not include clock jitter.

9.7.2 CA and CS_n Setup, Hold and Derating

For all input signals (CA and CS_n) the total tIS (setup time) and tIH (hold time) required is calculated by adding the data sheet tIS(base) and tIH(base) value (see 9.7.2.1 “CA and CS_n Setup and Hold Base-Values for 1V/nS” table) to the ΔtIS and ΔtIH derating value (see 9.7.2.2 “Derating Values LPDDR2 tIS/tIH - AC/DC Based AC220” table). Example: tIS (total setup time) = tIS(base) + ΔtIS.

Setup (tIS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of VIH(ac)min. Setup (tIS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of VIL(ac)max. If the actual signal is always earlier than the nominal slew rate line between shaded ‘VREF(dc) to ac region’, use nominal slew rate for derating value (see 9.7.2.4 “Nominal Slew Rate and tVAC for Setup Time tIS for CA and CS_n with Respect to Clock” figure). If the actual signal is later than the nominal slew rate line anywhere between shaded ‘VREF(dc) to ac region’, the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value (see 9.7.2.6 “Tangent Line for Setup Time tIS for CA and CS_n with Respect to Clock” figure).

Hold (tIH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(dc)max and the first crossing of VREF(dc). Hold (tIH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(dc)min and the first crossing of VREF(dc). If the actual signal is always later than the nominal slew rate line between shaded ‘dc to VREF(dc) region’, use nominal slew rate for derating value (see 9.7.2.5 “Nominal Slew Rate for Hold Time tIH for CA and CS_n with Respect to Clock” figure). If the actual signal is earlier than the nominal slew rate line anywhere between shaded ‘dc to VREF(dc) region’, the slew rate of a tangent line to the actual signal from the dc level to VREF(dc) level is used for derating value (see 9.7.2.7 “Tangent Line for Hold Time tIH for CA and CS_n with Respect to Clock” figure).

For a valid transition the input signal has to remain above/below VIH/IL(ac) for some time tVAC (see 9.7.2.3 “Required Time tVAC above VIH(ac) {below VIL(ac)} for Valid Transition” table).
Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached VIH/IL(ac) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach VIH/IL(ac).

For slew rates in between the values listed in 9.7.2.2 “Derating Values LPDDR2 tIS/tIH - AC/DC Based AC220” table, the derating values may obtained by linear interpolation. These values are typically not subject to production test. They are verified by design and characterization.

9.7.2.1 CA and CS_n Setup and Hold Base-Values for 1V/nS

Unit [pS]	LPDDR2-1066	LPDDR2-800	reference
$t_{IS(base)}$	0	70	$V_{IH/L(ac)} = V_{REF(dc)} \pm 220mV$
$t_{IH(base)}$	90	160	$V_{IH/L(dc)} = V_{REF(dc)} \pm 130mV$

Note: ac/dc referenced for 1V/nS CA and CS_n slew rate and 2V/nS differential CK_t-CK_c slew rate.

9.7.2.2 Derating Values LPDDR2 tIS/tIH - AC/DC Based AC220

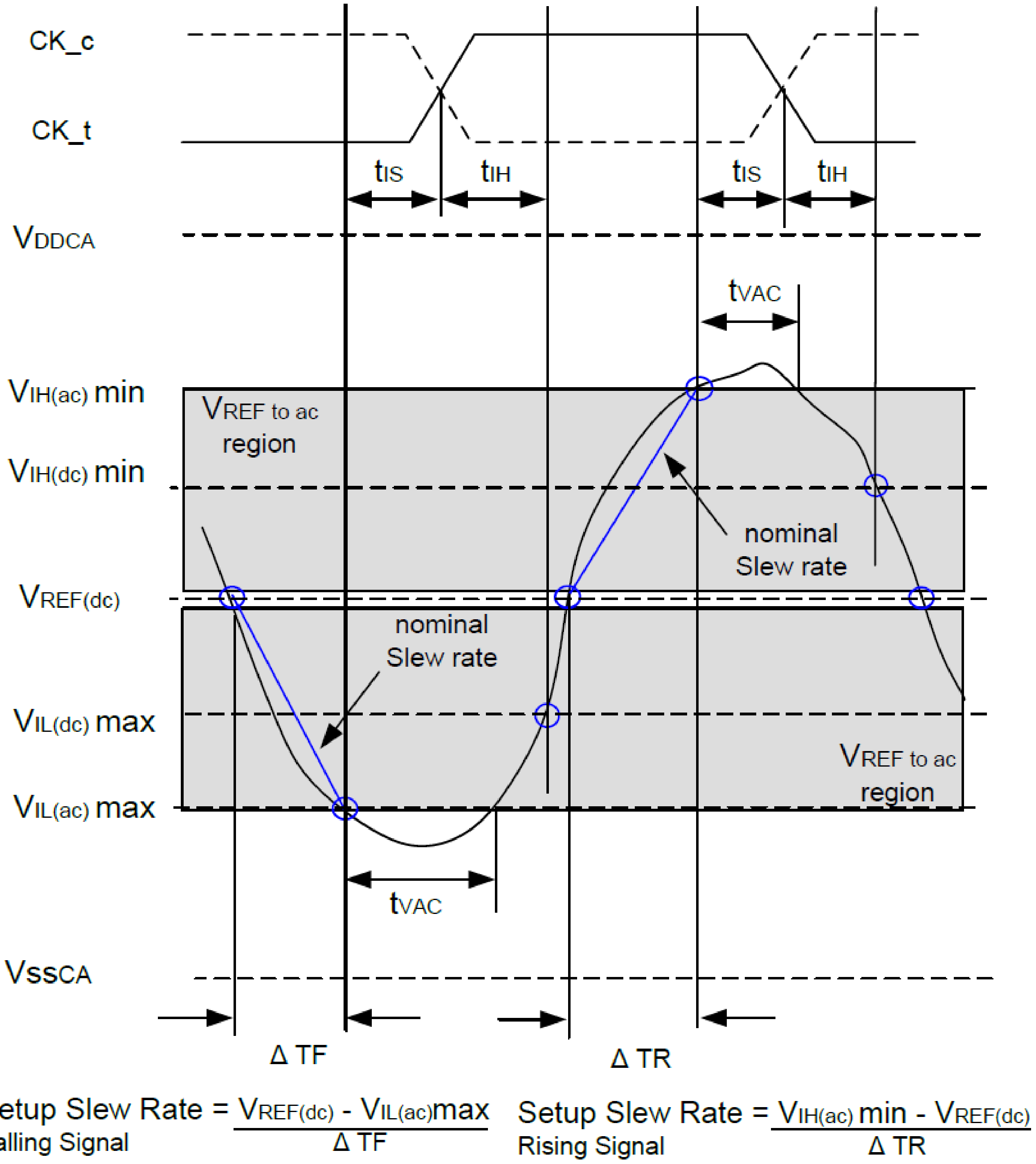
ΔtIS, ΔtIH derating in [pS] AC/DC based AC220 Threshold -> VIH(ac)=VREF(dc)+220mV, VIL(ac)=VREF(dc)-220mV DC130 Threshold -> VIH(dc)=VREF(dc)+130mV, VIL(dc)=VREF(dc)-130mV																
CA, CS_n Slew Rate V/nS	CK_t,CK_c Differential Slew Rate															
	4.0 V/nS		3.0 V/nS		2.0 V/nS		1.8 V/nS		1.6 V/nS		1.4 V/nS		1.2 V/nS		1.0 V/nS	
	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
2.0	110	65	110	65	110	65	-	-	-	-	-	-	-	-	-	-
1.5	74	43	73	43	73	43	89	59	-	-	-	-	-	-	-	-
1.0	0	0	0	0	0	0	16	16	32	32	-	-	-	-	-	-
0.9	-	-	-3	-5	-3	-5	13	11	29	27	45	43	-	-	-	-
0.8	-	-	-	-	-8	-13	8	3	24	19	40	35	56	55	-	-
0.7	-	-	-	-	-	-	2	-6	18	10	34	26	50	46	66	78
0.6	-	-	-	-	-	-	-	-	10	-3	26	13	42	33	58	65
0.5	-	-	-	-	-	-	-	-	-	-	4	-4	20	16	36	48
0.4	-	-	-	-	-	-	-	-	-	-	-	-	-7	2	17	34

Note: Cell contents '-' are defined as not supported.

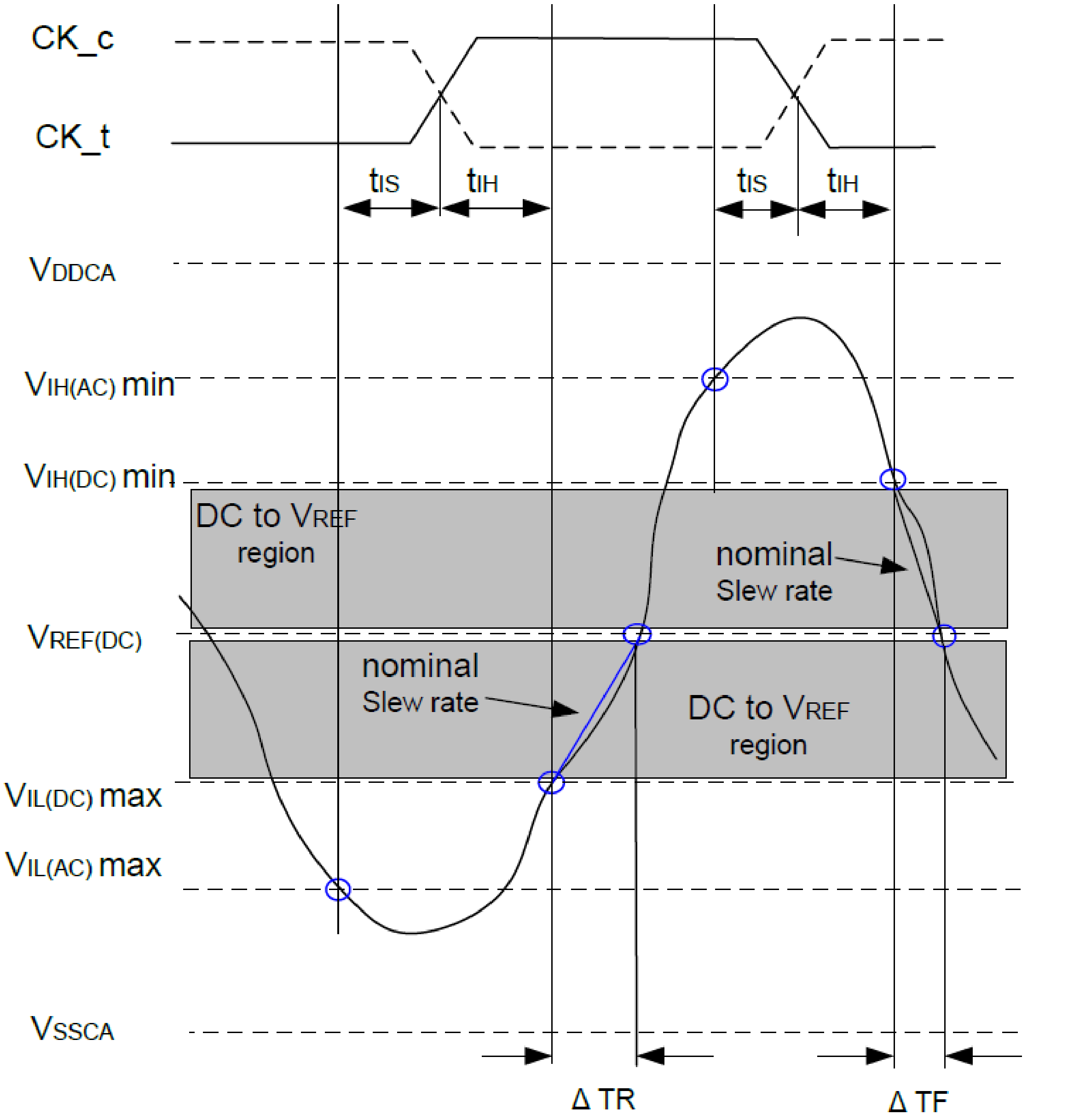
9.7.2.3 Required Time tVAC above VIH(ac) {below VIL(ac)} for Valid Transition

Slew Rate [V/nS]	tVAC @ 220mV [pS]	
	min	max
> 2.0	175	-
2.0	170	-
1.5	167	-
1.0	163	-
0.9	162	-
0.8	161	-
0.7	159	-
0.6	155	-
0.5	150	-
<0.5	150	-

9.7.2.4 Nominal Slew Rate and tVAC for Setup Time tIS for CA and CS_n with Respect to Clock



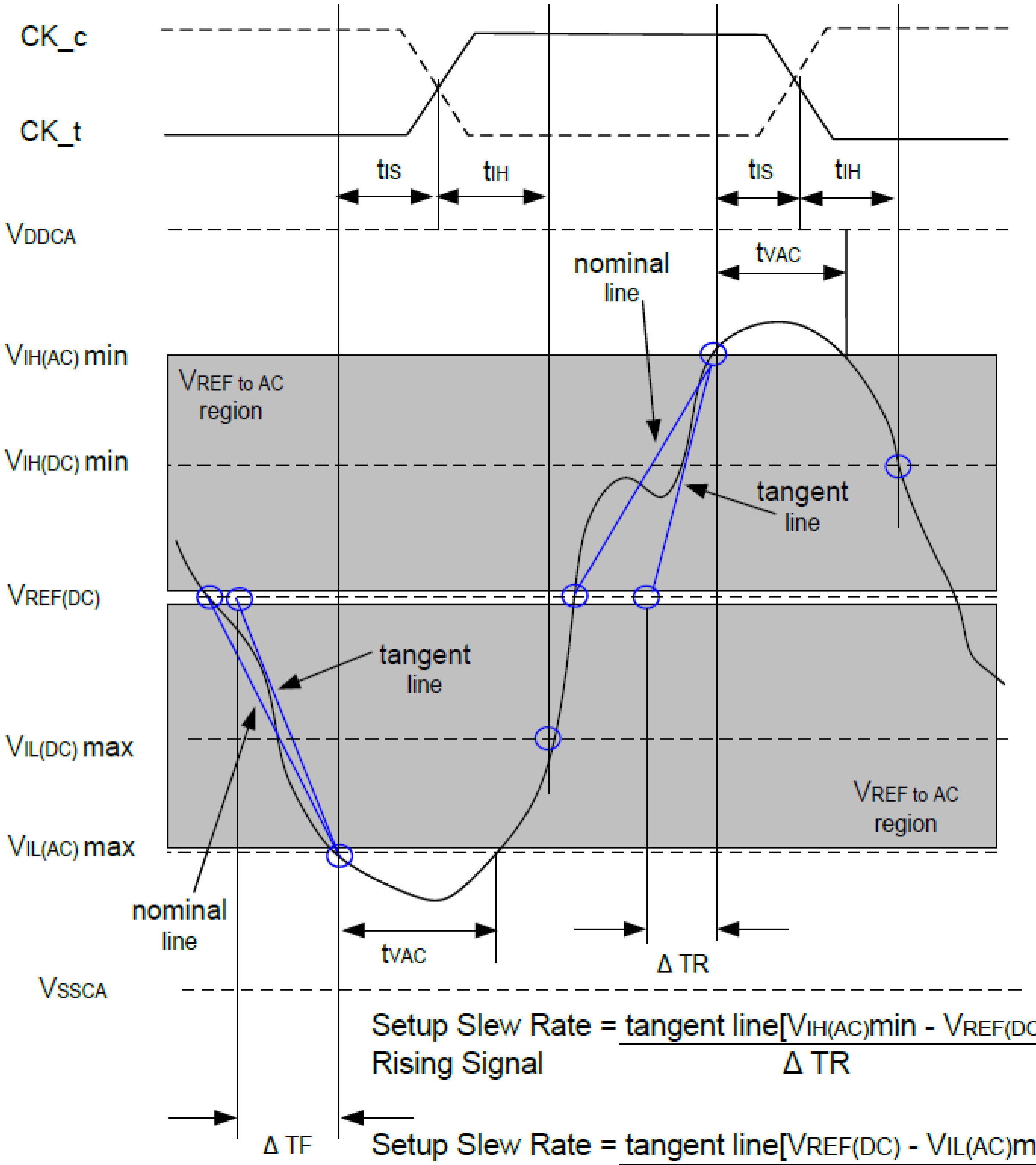
9.7.2.5 Nominal Slew Rate for Hold Time tIH for CA and CS_n with Respect to Clock



$$\text{Hold Slew Rate Rising Signal} = \frac{V_{REF(DC)} - V_{IL(DC)}max}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{V_{IH(DC)}min - V_{REF(DC)}}{\Delta TF}$$

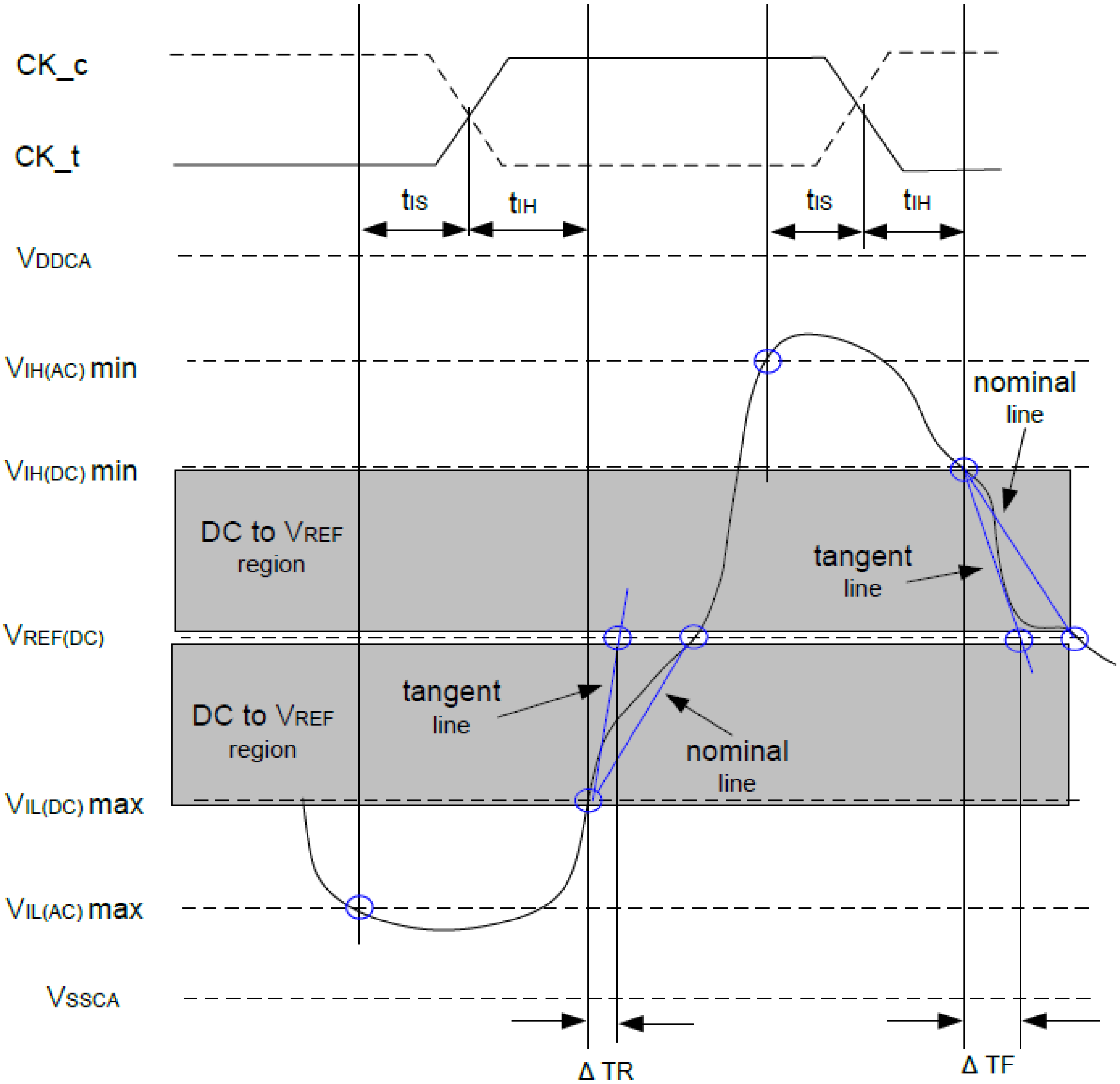
9.7.2.6 Tangent Line for Setup Time tIS for CA and CS_n with Respect to Clock



$$\text{Setup Slew Rate Rising Signal} = \frac{\text{tangent line}[V_{IH(AC)}min - V_{REF(DC)}]}{\Delta TR}$$

$$\text{Setup Slew Rate Falling Signal} = \frac{\text{tangent line}[V_{REF(DC)} - V_{IL(AC)}max]}{\Delta TF}$$

9.7.2.7 Tangent Line for Hold Time tIH for CA and CS_n with Respect to Clock



$$\text{Hold Slew Rate Rising Signal} = \frac{\text{tangent line } [V_{REF(DC)} - V_{IL(DC)}max]}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{\text{tangent line } [V_{IH(DC)}min - V_{REF(DC)}]}{\Delta TF}$$

9.7.3 Data Setup, Hold and Slew Rate Derating

For all input signals (DQ, DM) the total tDS (setup time) and tDH (hold time) required is calculated by adding the data sheet tDS(base) and tDH(base) value (see 9.7.3.1 “Data Setup and Hold Base-Values” table) to the ΔtDS and ΔtDH (see 9.7.3.2 “Derating Values LPDDR2 tDS/tDH - AC/DC Based AC220” table) derating value respectively. Example: tDS (total setup time) = tDS(base) + ΔtDS.

Setup (tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of VIH(ac)min. Setup (tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of VIL(ac)max (see 9.7.3.4 “Nominal Slew Rate and tVAC for Setup Time tDS for DQ with Respect to Strobe” figure). If the actual signal is always earlier than the nominal slew rate line between shaded ‘VREF(dc) to ac region’, use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded ‘VREF(dc) to ac region’, the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value (see 9.7.3.6 “Tangent Line for Setup Time tDS for DQ with Respect to Strobe” figure).

Hold (tDH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(dc)max and the first crossing of VREF(dc). Hold (tDH) nominal slew rate for a falling sig5nal is defined as the slew rate between the last crossing of VIH(dc)min and the first crossing of VREF(dc) (see 9.7.3.5 “Nominal Slew Rate for Hold Time tDH for DQ with Respect to Strobe” figure). If the actual signal is always later than the nominal slew rate line between shaded ‘dc level to VREF(dc) region’, use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded ‘dc to VREF(dc) region’, the slew rate of a tangent line to the actual signal from the dc level to VREF(dc) level is used for derating value (see 9.7.3.7 “Tangent Line for Hold Time tDH for DQ with Respect to Strobe” figure).

For a valid transition the input signal has to remain above/below VIH/IL(ac) for some time tVAC (see 9.7.3.3 “Required Time tVAC above VIH(ac) {below VIL(ac)} for Valid Transition” table).

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached VIH/IL(ac) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach VIH/IL(ac).
For slew rates in between the values listed in 9.7.3.2 “Derating Values LPDDR2 tDS/tDH - AC/DC Based AC220” table, the derating values may obtained by linear interpolation. These values are typically not subject to production test. They are verified by design and characterization.

9.7.3.1 Data Setup and Hold Base-Values

Unit [pS]	LPDDR2-1066	LPDDR2-800	reference
$t_{DS(base)}$	-10	50	$V_{IH/L(ac)} = V_{REF(dc)} \pm 220mV$
$t_{DH(base)}$	80	140	$V_{IH/L(dc)} = V_{REF(dc)} \pm 130mV$

Note: ac/dc referenced for 1V/nS DQ,DM slew rate and 2V/nS differential DQS_t-DQS_c slew rate.

9.7.3.2 Derating Values LPDDR2 tDS/tDH - AC/DC Based AC220

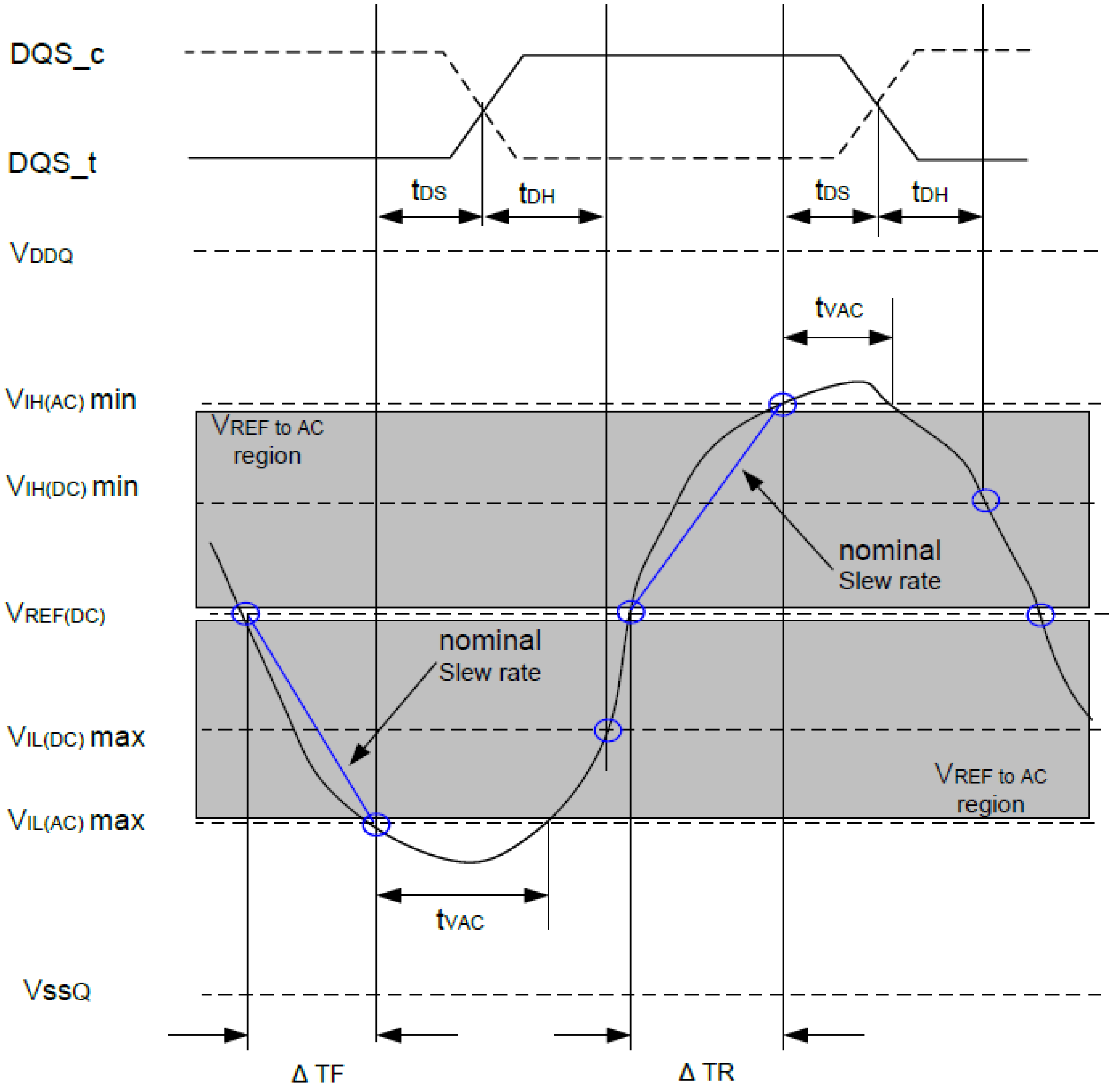
ΔtDS, ΔDH derating in [pS] AC/DC based a AC220 Threshold -> VIH(ac) = VREF(dc) + 220mV, VIL(ac) = VREF(dc) - 220mV DC130 Threshold -> VIH(dc) = VREF(dc) + 130mV, VIL(dc) = VREF(dc) - 130mV																
DQ, DM Slew Rate V/nS	DQS_t, DQS_c Differential Slew Rate															
	4.0 V/nS		3.0 V/nS		2.0 V/nS		1.8 V/nS		1.6 V/nS		1.4 V/nS		1.2 V/nS		1.0 V/nS	
	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
2.0	110	65	110	65	110	65	-	-	-	-	-	-	-	-	-	-
1.5	74	43	73	43	73	43	89	59	-	-	-	-	-	-	-	-
1.0	0	0	0	0	0	0	16	16	32	32	-	-	-	-	-	-
0.9	-	-	-3	-5	-3	-5	13	11	29	27	45	43	-	-	-	-
0.8	-	-	-	-	-8	-13	8	3	24	19	40	35	56	55	-	-
0.7	-	-	-	-	-	-	2	-6	18	10	34	26	50	46	66	78
0.6	-	-	-	-	-	-	-	-	10	-3	26	13	42	33	58	65
0.5	-	-	-	-	-	-	-	-	-	-	4	-4	20	16	36	48
0.4	-	-	-	-	-	-	-	-	-	-	-	-	-7	2	17	34

Note: Cell contents '-' are defined as not supported.

9.7.3.3 Required Time tVAC above VIH(ac) {below VIL(ac)} for Valid Transition

Slew Rate [V/nS]	**tVAC @ 220mV [pS]**	
	min	**max**
> 2.0	175	-
2.0	170	-
1.5	167	-
1.0	163	-
0.9	162	-
0.8	161	-
0.7	159	-
0.6	155	-
0.5	150	-
<0.5	150	-

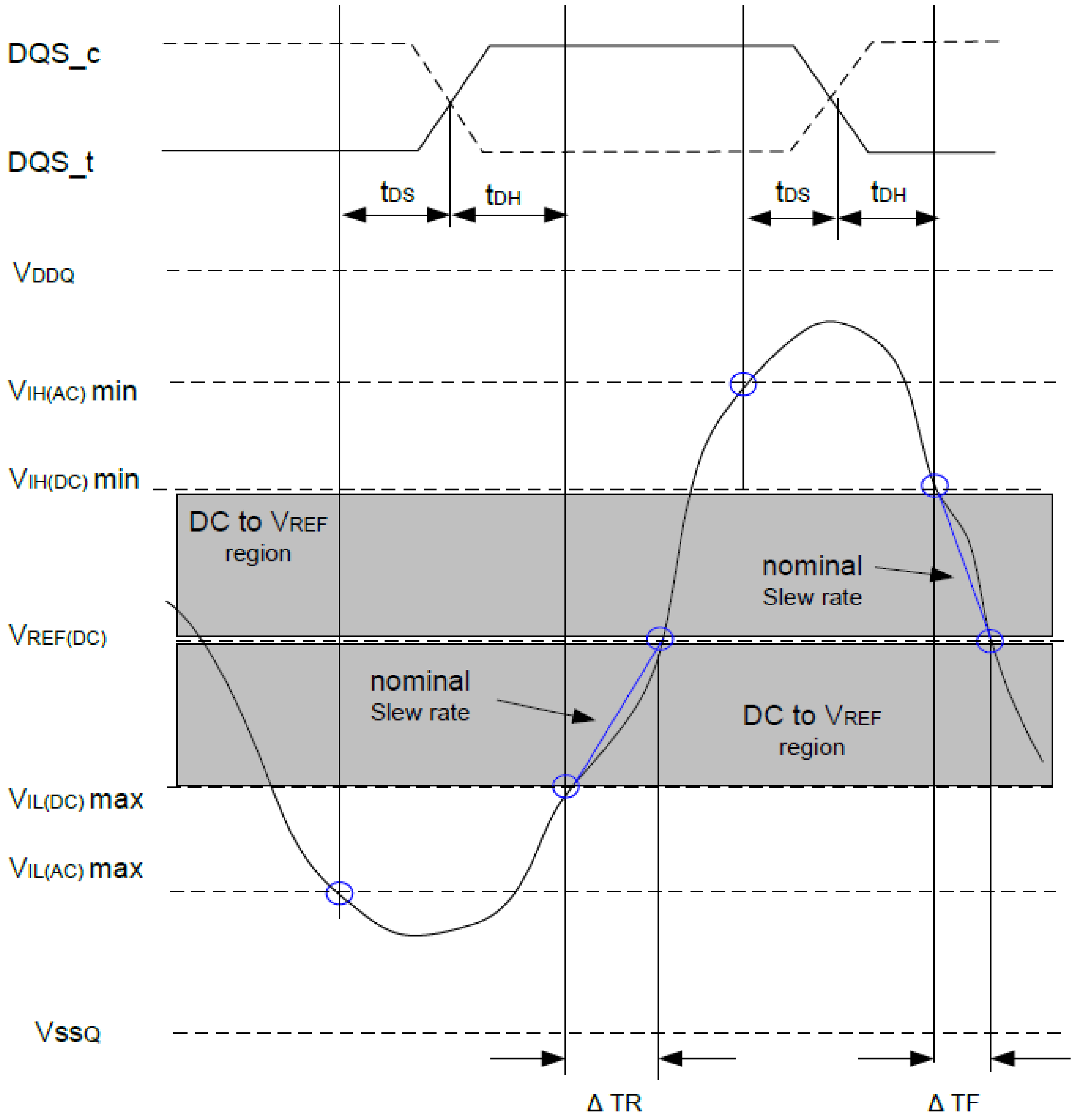
9.7.3.4 Nominal Slew Rate and tVAC for Setup Time tDS for DQ with Respect to Strobe



$$\text{Setup Slew Rate Falling Signal} = \frac{V_{REF(DC)} - V_{IL(AC)}max}{\Delta TF}$$

$$\text{Setup Slew Rate Rising Signal} = \frac{V_{IH(AC)}min - V_{REF(DC)}}{\Delta TR}$$

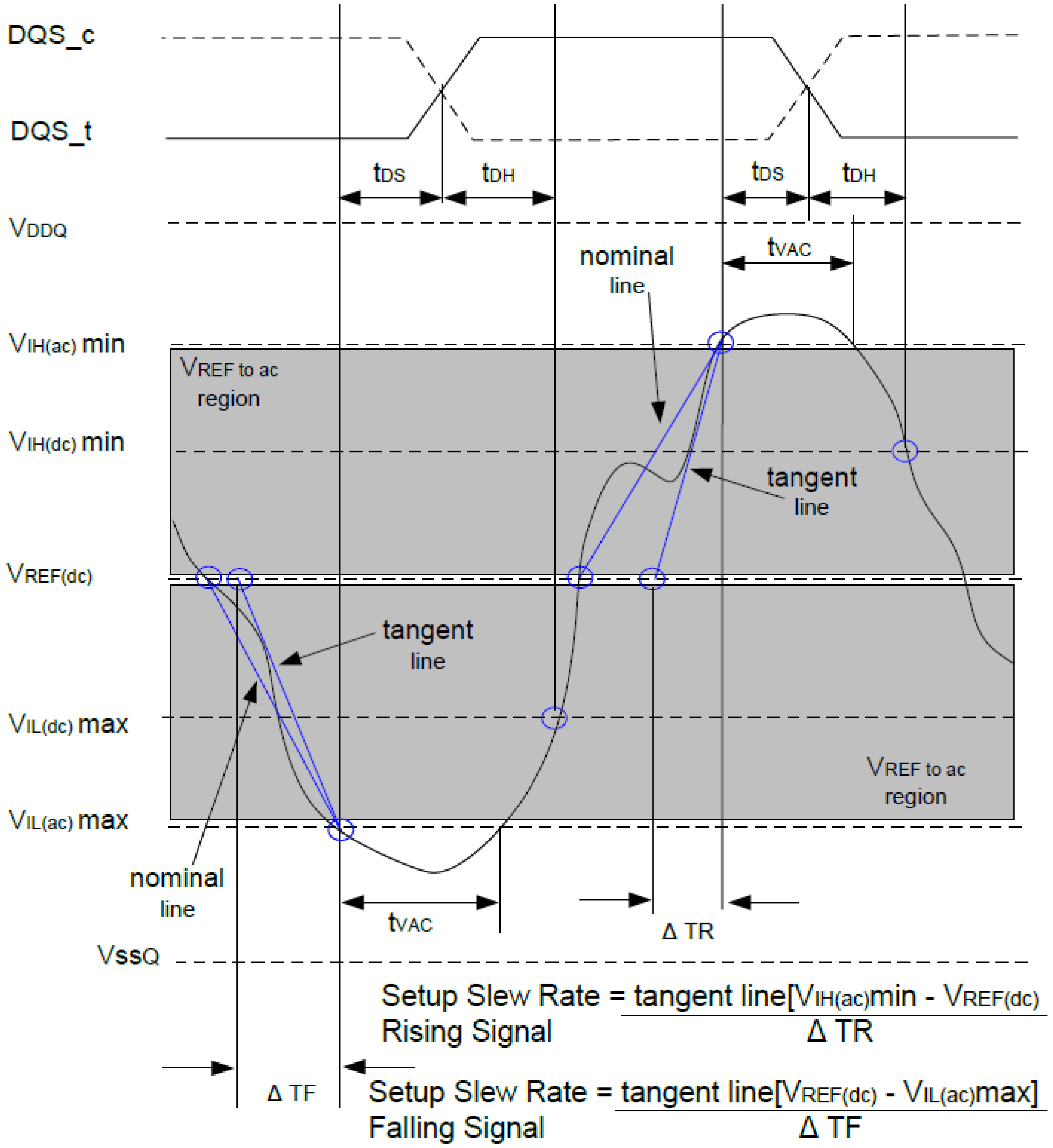
9.7.3.5 Nominal Slew Rate for Hold Time tDH for DQ with Respect to Strobe



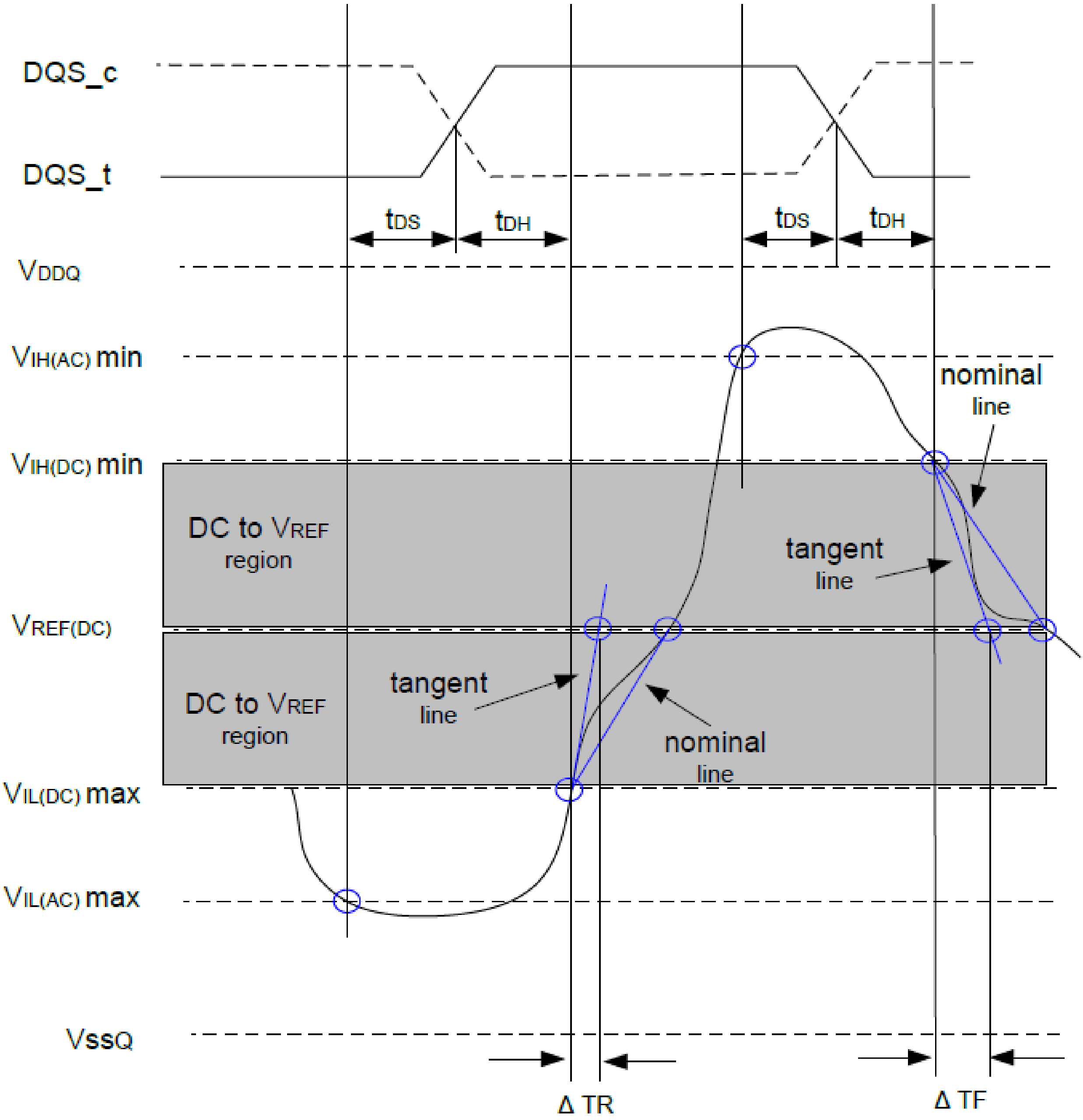
$$\text{Hold Slew Rate Rising Signal} = \frac{V_{REF(DC)} - V_{IL(DC)max}}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{V_{IH(DC)min} - V_{REF(DC)}}{\Delta TF}$$

9.7.3.6 Tangent Line for Setup Time tDS for DQ with Respect to Strobe



9.7.3.7 Tangent Line for Hold Time tDH for DQ with Respect to Strobe



Hold Slew Rate Rising Signal = tangent line [VREF(DC) - VIL(DC)max] / Δ TR

Hold Slew Rate Falling Signal = tangent line [VIH(DC)min - VREF(DC)] / Δ TF

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