Sep. 2022

SCC16GP03H4F1C-32AA
SCC32GP13H4F1C-32AA

288-Pin DDR4 Registered DIMM(X72,ECC)

EU RoHS Compliant

Data Sheet

Rev. C

Revision History		
Date	**Revision**	**Subjects (major changes since last revision)**
2021-07	A	Initial Release
2022-07	B	Modify the pin table
2022-09	C	Optimize Module Description

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1 Overview

This chapter gives an overview of the 288-pin DDR4 Parity Registered DIMM product family and describes its main characteristics.

1.1 Features

- 288-Pin PC4-3200 DDR4 Parity Registered DIMM
- Frequency/CAS latency:
  0.625ns @ CL = 22 (DDR4-3200)
- VDD = 1.2V ±60mV
- VPP = 2.5V (2.375V~2.75V)
- VDDSPD = 2.5V
- Programmable CAS latency 9, 10,11, 12, 13, 14, 15
  16, 17, 18, 19, 20, 21, 22 and 24 supported
- Programmable additive latency 0, CL-1, and CL-2
  supported (x4/x8 only)
- Programmable CAS Write latency (CWL) = 9, 10, 11, 12,
  14, 16,18 , 20
- Programmable burst length 4/8 with both nibble
  sequential and interleave mode
- Data bus inversion (DBI) for data bus
- Fly-by topology
- Terminated control command and address bus
- BL switch on the fly
- 16 internal banks; 4 groups of 4 banks each
- Nominal and dynamic on-die termination (ODT)
  for strobe, and mask signals
- Low-power auto self refresh (LPASR)
- On-die VREFDQ generation and calibration
- Fixed burst chop (BC) of 4 and burst length (BL)
  of 8 via the mode register set (MRS)
- Gold edge contacts
- Halogen-free
- Average Refresh Cycle (Tcase of 0 °C ~ 95 °C)
  - 7.8 μs at 0 °C ~ 85 °C
  - 3.9 μs at 85 °C ~ 95 °C

Table 1 - Module Performance Table

UnilC Speed Code		**-32AA**	**Unit**	**Note**
DRAM Speed Grade	**DDR4**	**-3200**		
CAS-RCD-RP latencies		**-22-22-22**	t_{CK}	
Min. RAS-CAS-Delay	t_{RCD}	13.75	ns	
Min. Row Precharge Time	t_{RP}	13.75	ns	
Min. Row Active Time	t_{RAS}	32	ns	
Min. Row Cycle Time	t_{RC}	45.75	ns	

1.2 Description

The UniIC 16GB/32GB module family are Parity Registered DIMM with 31.25mm height based on DDR4 technology. DIMMs intended for mounting into 288-pin connector sockets.

The memory array is designed with 16Gbit Double-Data- Rate-Four (DDR4) Synchronous DRAMs. Decoupling capacitors are mounted on the PCB board. The DIMMs feature serial presence detect based on a serial E^2PROM device using the 2-pin I^2C protocol.

Table 2 - Ordering Information

Product Type[1]	Compliance Code[2]	Description	SDRAM Technology
SCC16GP03H4F1C-32AA	16GB 1R×8 PC4-3200P-22-22-22	1Rank	16Gbit (×8)
SCC32GP13H4F1C-32AA	32GB 2R×8 PC4-3200P-22-22-22	2Ranks	16Gbit (×8)

1) For detailed information regarding Product Type of UniIC please see chapter "Product Type Nomenclature" of this data sheet.
2) This describes the speed grade, for example "PC4-3200P-22-22-22" where 3200 means DIMM modules with 3200MT/s data rate and "22-22-22" means Column Address Strobe (CAS) latency=22, Row Column Delay (RCD) latency = 22 and Row Precharge (RP) latency = 22.

Table 3 - Address Format

DIMM Density	16GB(1Rx8,X72)	32GB(2Rx8,X72)
Row address	128K A[16:0]	128K A[16:0]
Column address	1K A[9:0]	1K A[9:0]
Device bank group address	4 BG[1:0]	4 BG[1:0]
Device bank address per group	4 BA[1:0]	4 BA[1:0]
Device configuration	16Gb(2Gx8)	16Gb(2Gx8)
Module rank address	1 CS_n[0]	2CS_n[1:0]
Device Quantity	9	18

2 Pin Configurations

2.1 Pin Configurations

The pin configuration of the 288-Pin Parity Registered DIMM is listed by function in **Table 4** (288 pins).

Table 4 - Pin Configuration RDIMM (288 pin)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	NC	145	NC	39	VSS	183	DQ25	77	VTT	221	VTT	114	VSS	258	DQ47
2	VSS	146	VREFCA	40	DQS12_t/ TDQS12_t	184	VSS	KEY				115	DQ42	259	VSS
3	DQ4	147	VSS	41	DQS12_c/ TDQS12_c	185	DQS3_c	78	EVENT_n	222	PARITY	116	VSS	260	DQ43
4	VSS	148	DQ5	42	VSS	186	DQS3_t	79	A0	223	VDD	117	DQ52	261	VSS
5	DQ0	149	VSS	43	DQ30	187	VSS	80	VDD	224	BA1	118	VSS	262	DQ53
6	VSS	150	DQ1	44	VSS	188	DQ31	81	BA0	225	A10/AP	119	DQ48	263	VSS
7	DQS9_t/ TDQS9_t	151	VSS	45	DQ26	189	VSS	82	RAS_n/A16	226	VDD	120	VSS	264	DQ49
8	DQS9_c/ TDQS9_c	152	DQS0_c	46	VSS	190	DQ27	83	VDD	227	RFU	121	DQS15_t/ TDQS15_t	265	VSS
9	VSS	153	DQS0_t	47	CB4	191	VSS	84	CS0_n	228	WE_n /A14	122	DQS15_c/ TDQS15_c	266	DQS6_c
10	DQ6	154	VSS	48	VSS	192	CB5,	85	VDD	229	VDD	123	VSS	267	DQS6_t
11	VSS	155	DQ7	49	CB0	193	VSS	86	CAS_n /A15	230	NC	124	DQ54	268	VSS
12	DQ2	156	VSS	50	VSS	194	CB1	87	ODT0	231	VDD	125	VSS	269	DQ55
13	VSS	157	DQ3	51	DQS17_t/ TDQS17_t	195	VSS	88	VDD	232	A13	126	DQ50	270	VSS
14	DQ12	158	VSS	52	DQS17_c/ TDQS17_c	196	DQS8_c	89	CS1_n	233	VDD	127	VSS	271	DQ51
15	VSS	159	DQ13	53	VSS	197	DQS8_t	90	VDD	234	NC	128	DQ60	272	VSS
16	DQ8	160	VSS	54	CB6	198	VSS	91	ODT1	235	NC	129	VSS	273	DQ61
17	VSS	161	DQ9	55	VSS	199	CB7	92	VDD	236	VDD	130	DQ56	274	VSS
18	DQS10_t/ TDQS10_t	162	VSS	56	CB2	200	VSS	93	NC	237	NC	131	VSS	275	DQ57
19	DQS10_c/ TDQS10_c	163	DQS1_c	57	VSS	201	CB3	94	VSS	238	SA2	132	DQS16_t/ TDQS16_t	276	VSS
20	VSS	164	DQS1_t	58	RESET_n	202	VSS	95	DQ36	239	VSS	133	DQS16_c/ TDQS16_c	277	DQS7_c
21	DQ14	165	VSS	59	VDD	203	CKE1	96	VSS	240	DQ37	134	VSS	278	DQS7_t
22	VSS	166	DQ15	60	CKE0	204	VDD	97	DQ32	241	VSS	135	DQ62	279	VSS

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
23	DQ10	167	VSS	61	VDD	205	RFU	98	VSS	242	DQ33	136	VSS	280	DQ63
24	VSS	168	DQ11	62	ACT_n	206	VDD	99	DQS13_t/ TDQS13_t	243	VSS	137	DQ58	281	VSS
25	DQ20	169	VSS	63	BG0	207	BG1	100	DQS13_c/ TDQS13_c	244	DQS4_c	138	VSS	282	DQ59
26	VSS	170	DQ21	64	VDD	208	ALERT_n	101	VSS	245	DQS4_t	139	SA0	283	VSS
27	DQ16	171	VSS	65	A12 /BC_n	209	VDD	102	DQ38	246	VSS	140	SA1	284	VDDSPD
28	VSS	172	DQ17	66	A9	210	A11	103	VSS	247	DQ39	141	SCL	285	SDA
29	DQS11_t/ TDQS11_t	173	VSS	67	VDD	211	A7	104	DQ34	248	VSS	142	VPP	286	VPP
30	DQS11_c/ TDQS11_c	174	DQS2_c	68	A8	212	VDD	105	VSS	249	DQ35	143	VPP	287	VPP
31	VSS	175	DQS2_t	69	A6	213	A5	106	DQ44	250	VSS	144	RFU	288	VPP
32	DQ22	176	VSS	70	VDD	214	A4	107	VSS	251	DQ45				
33	VSS	177	DQ23	71	A3	215	VDD	108	DQ40	252	VSS				
34	DQ18	178	VSS	72	A1	216	A2	109	VSS	253	DQ41				
35	VSS	179	DQ19	73	VDD	217	VDD	110	DQS14_t/ TDQS14_t	254	VSS				
36	DQ28	180	VSS	74	CK0_t	218	CK1_t	111	DQS14_c/ TDQS14_c	255	DQS5_c				
37	VSS	181	DQ29	75	CK0_c	219	CK1_c	112	VSS	256	DQS5_t				
38	DQ24	182	VSS	76	VDD	220	VDD	113	DQ46	257	VSS				

2.2 Pin Descriptions

Table 5 – Pin Descriptions

Symbol	Type	Function
CKx_t, CKx_c,	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKEx	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates internal clock signals and device input buffers and output drivers. Taking CKE LOW provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t, CK_c, ODT and CKE, are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CSx_n	Input	Chip Select: All commands are masked when CS-n is registered HIGH. CS_n provides for external Rank selection. CS_n is considered part of the command code.
Cx	Input	Chip ID : Chip ID is only used for 3DS for 2,4,8 high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code.
ODTx	Input	On Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c, TDQS_t and TDQS_c signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	Activation Command Input: ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14
RAS_n/A16. CAS_n/A15. WE_n/A14	Input	Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, these are Addresses like A16, A15 and A14 but for non-activation command with ACT_n High, these are Command pins for Read, Write and other command defined in command truth table
BGx	Input	Bank Group Inputs: BG0 - BG1 define which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle.
BAx	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
Ax	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions. See other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is only defined for 16 Gb x4 SDRAM configurations.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.

Symbol	Type	Function
A12/BC_n	Input	Burst Chop: A12/BC_n is sampled during Read and Write commands to determine if burst chop (on-thefly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
Parity	Input	Command and Address Parity Input: DDR4 Supports Even Parity check in SDRAMs with MR setting. Once it's enabled via Register in MR5, then SDRAM calculates Parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG0-BG1, BA0-BA1, A17-A0. Input parity should be maintained at the rising edge of the clock and at the same time with command & address with CS_n LOW
SAx	Input	Serial address inputs: Used to configure the temperature sensor/SPD EEPROM address range on the I2C bus.
SCL	Input	Serial clock for temperature sensor/SPD EEPROM: Used to synchronize communication to and from the temperature sensor/SPD EEPROM on the I2C bus.
RESET_n	CMOS Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation.
DQx, CBx	I/O	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific data sheets to determine which DQ is used.
DQSx_t-DQSx_c	I/O	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. The data strobe DQS_t is paired with differential signals DQS_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.
DM_n/DBI_n/ TDQS_t (DMU_n, DBIU_n), (DML_n/ DBII_n)	I/O	Input data mask and data bus inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a write access. DM_n is sampled on both edges of DQS. DM is multiplexed with the DBI function by the mode register A10, A11, and A12 settings in MR5. For a x8 device, the function of DM or TDQS is enabled by the mode register A11 setting in MR1. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/ output after inversion inside the DDR4 device and not inverted if DBI_n is HIGH. TDQS is only supported in x8 SDRAM configurations (TDQS is not valid for UDIMMs).
SDA	I/O	Serial Data: Bidirectional signal used to transfer data in or out of the EEPROM or EEPROM/TS combo device.
ALERT_n	Output	Alert: It has multi functions such as CRC error flag, Command and Address Parity error flag as Output signal. If there is error in CRC, then ALERT_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then ALERT_n goes LOW for relatively long period until ongoing SDRAM internal recovery transaction is complete. During Connectivity Test mode this pin functions as an input.
EVENT_n	Output	Temperature event: The EVENT_n pin is asserted by the temperature sensor when critical temperature thresholds have been exceeded. This pin has no function (NF) on modules without temperature sensors.
TDQS_t TDQS_c (x8 DRAM-based RDIMM only)	Output	Termination data strobe: When enabled via the mode register, the DRAM device enables the same RTT termination resistance on TDQS_t and TDQS_c that is applied to DQS_t and DQS_c. When the TDQS function is disabled via the mode register, the DM/TDQS_t pin provides the data mask (DM) function, and the TDQS_c pin is not used. The TDQS function must be disabled in the mode register for both the x4 and x16 configurations. The DM function is supported only in x8 and x16 configurations. DM, DBI, and TDQS are a shared pin and are enabled/disabled by mode register settings. For more information about TDQS, see the DDR4 DRAM component datasheet (TDQS_t and TDQS_c are not valid for UDIMMs).
VDD	Supply	Module power supply: 1.2V (TYP).
VPP	Supply	DRAM activating power supply: 2.5V -0.125V / +0.250V.

Symbol	Type	Function
VREFCA	Supply	Reference voltage for control, command, and address pins.
VSS	Supply	Ground.
VTT	Supply	Power supply for termination of address, command, and control VDD/2.
VDDSPD	Supply	Power supply used to power the I2C bus for SPD.
RFU	-	Reserved for Future Use: No on DIMM electrical connection is present
NC	-	No Connect: No on DIMM electrical connection is present

3 General Description

3.1 General Description

High-speed DDR4 SDRAM modules use DDR4 SDRAM devices with 2 or 4 internal memory bank groups. DDR4 SDRAM modules utilizing 4- and 8-bit-wide DDR4 SDRAM have 4 internal bank groups consisting of 4 memory banks each, providing a total of 16 banks. Sixteen-bit-wide DDR4 SDRAM has 2 internal bank groups consisting of 4 memory banks each, providing a total of 8 banks. DDR4 SDRAM modules benefit from DDR4 SDRAM's use of an 8n-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single READ or WRITE operation for the DDR4 SDRAM effectively consists of a single 8n-bit-wide, four-clock data transfer at the internal DRAM core and eight corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.
DDR4 modules use two sets of differential signals: DQS, DQS# to capture data and CK and CK# to capture commands, addresses, and control signals. Differential clocks and data strobes ensure exceptional noise immunity for these signals and provide precise crossing points to capture input signals.

3.2 Serial Presence-Detect EEPROM Operation

DDR4 SDRAM modules incorporate serial presence-detect. The SPD data is stored in a 512-byte EEPROM. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I2C bus using the DIMM’s SCL (clock) SDA (data), and SA (address) pins. Write protect (WP) is connected to VSS, permanently disabling hardware write protection.

3.3 Function Block Diagram

Figure 1 - Function Block Diagram_SCC16GP03H4F1C-32AA

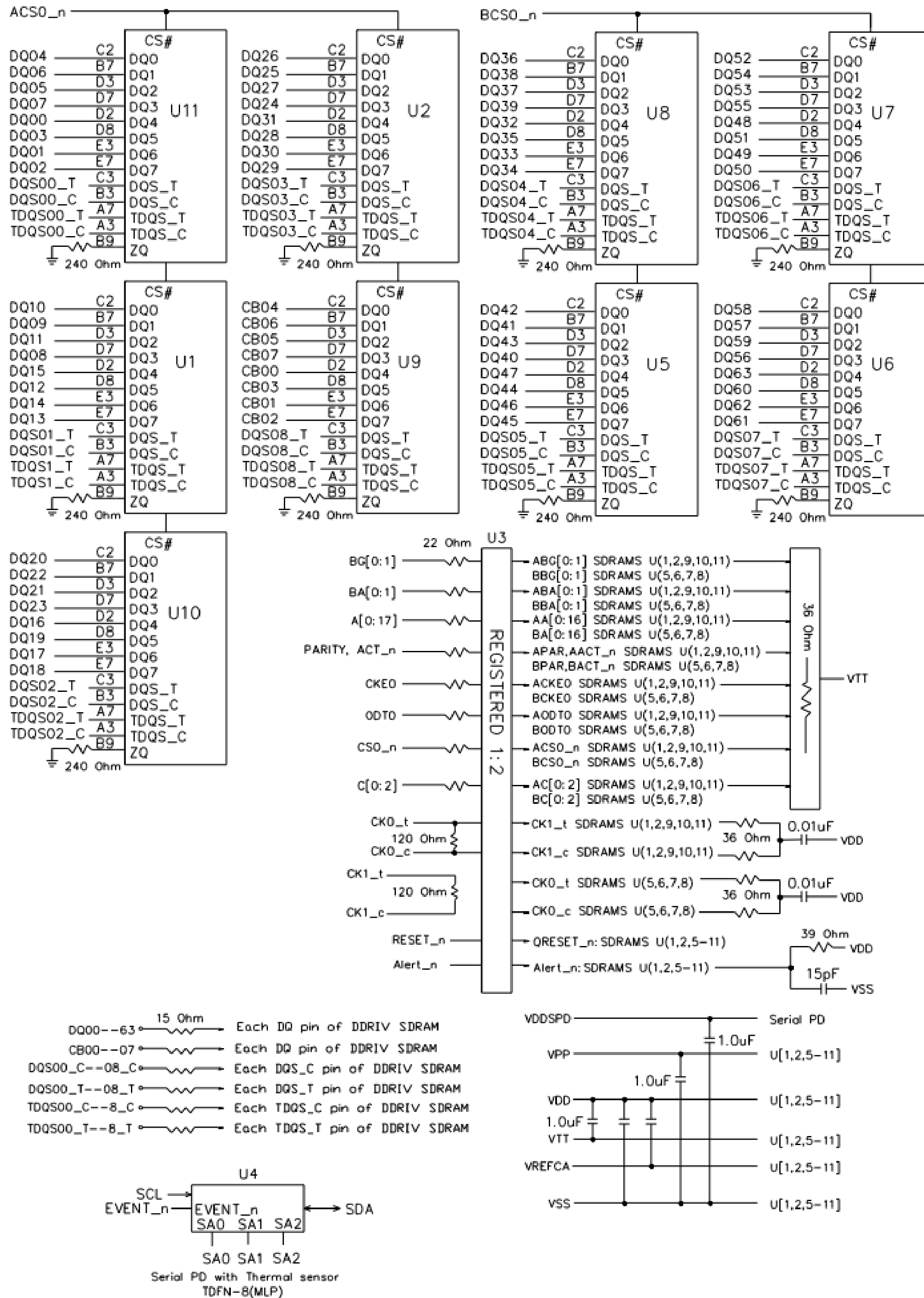
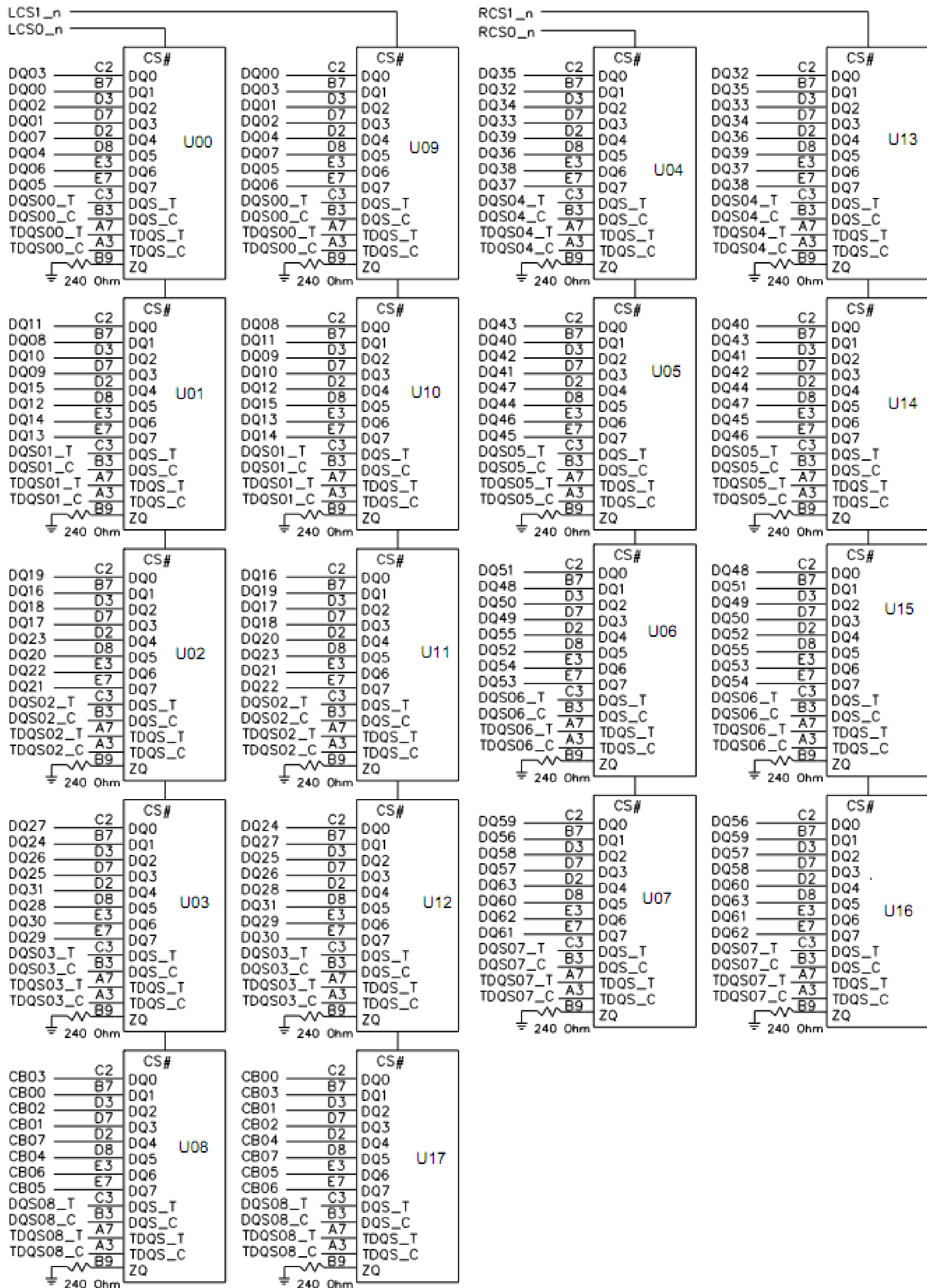
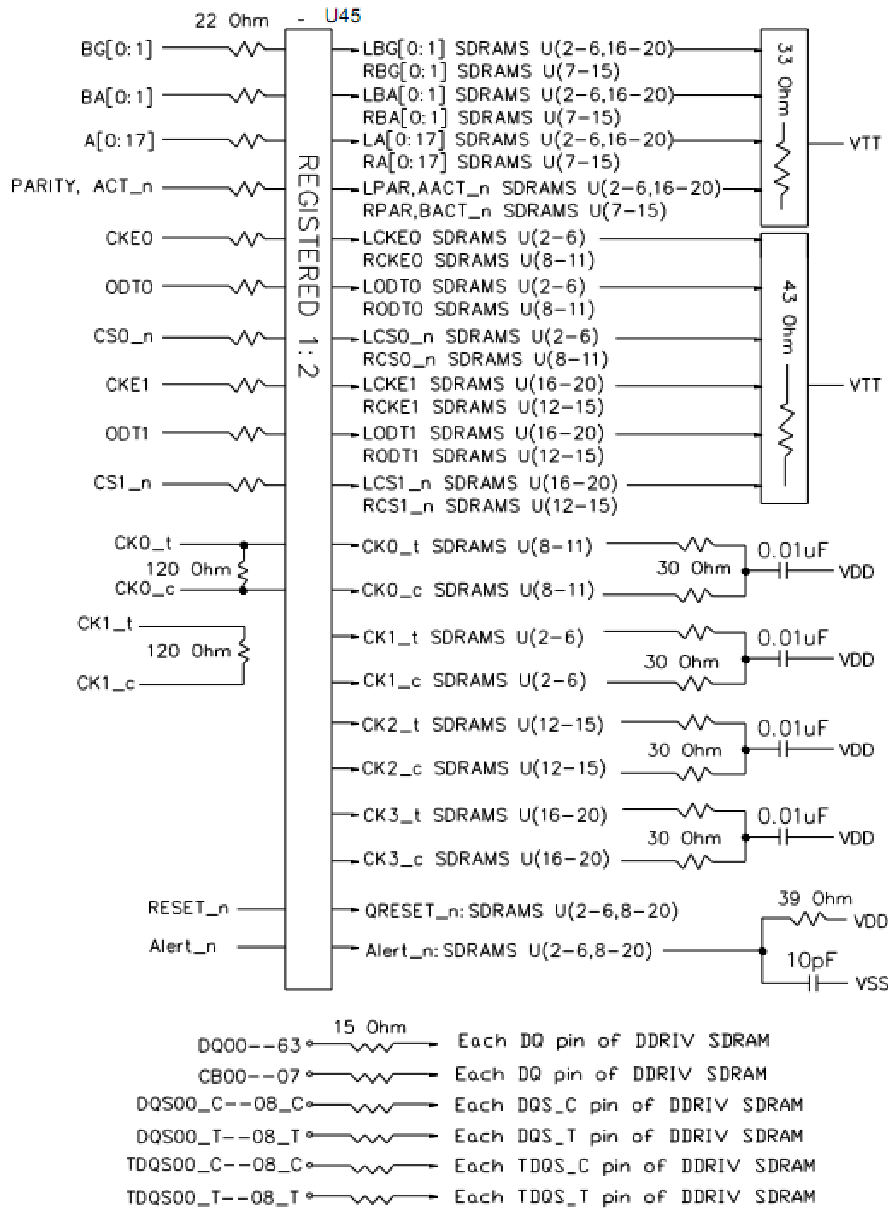
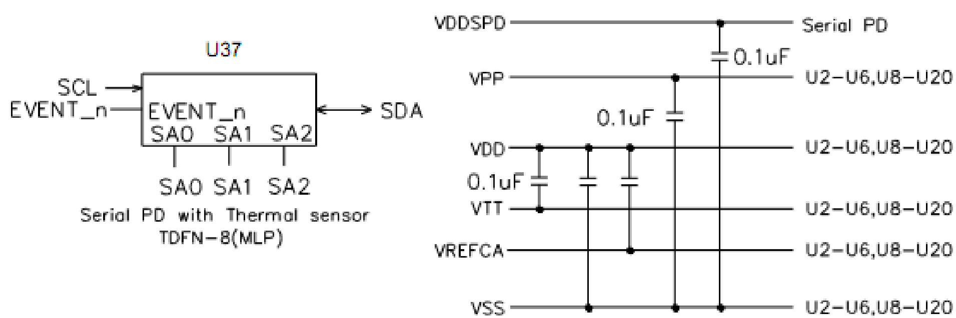


Figure 2 - Function Block Diagram_SCC32GP13H4F1C-32AA




22 Ohm
U45
BG[0:1]
BA[0:1]
A[0:17]
PARITY, ACT_n
CKE0
ODT0
CS0_n
CKE1
ODT1
CS1_n
REGISTERED 1:2
LBG[0:1] SDRAMS U(2-6,16-20)
RBG[0:1] SDRAMS U(7-15)
LBA[0:1] SDRAMS U(2-6,16-20)
RBA[0:1] SDRAMS U(7-15)
LA[0:17] SDRAMS U(2-6,16-20)
RA[0:17] SDRAMS U(7-15)
LPAR,AACT_n SDRAMS U(2-6,16-20)
RPAR,BACT_n SDRAMS U(7-15)
33 Ohm
VTT
LCKE0 SDRAMS U(2-6)
RCKE0 SDRAMS U(8-11)
LODT0 SDRAMS U(2-6)
RODT0 SDRAMS U(8-11)
LCS0_n SDRAMS U(2-6)
RCS0_n SDRAMS U(8-11)
LCKE1 SDRAMS U(16-20)
RCKE1 SDRAMS U(12-15)
LODT1 SDRAMS U(16-20)
RODT1 SDRAMS U(12-15)
LCS1_n SDRAMS U(16-20)
RCS1_n SDRAMS U(12-15)
43 Ohm
VTT
CK0_t
120 Ohm
CK0_c
CK1_t
120 Ohm
CK1_c
CK0_t SDRAMS U(8-11)
CK0_c SDRAMS U(8-11)
30 Ohm
0.01uF
VDD
CK1_t SDRAMS U(2-6)
CK1_c SDRAMS U(2-6)
30 Ohm
0.01uF
VDD
CK2_t SDRAMS U(12-15)
CK2_c SDRAMS U(12-15)
30 Ohm
0.01uF
VDD
CK3_t SDRAMS U(16-20)
CK3_c SDRAMS U(16-20)
30 Ohm
0.01uF
VDD
RESET_n
Alert_n
QRESET_n: SDRAMS U(2-6,8-20)
Alert_n: SDRAMS U(2-6,8-20)
39 Ohm
VDD
10pF
VSS
15 Ohm
DQ00--63
CB00--07
DQS00_C--08_C
DQS00_T--08_T
TDQS00_C--08_C
TDQS00_T--08_T
Each DQ pin of DDRIV SDRAM
Each DQ pin of DDRIV SDRAM
Each DQS_C pin of DDRIV SDRAM
Each DQS_T pin of DDRIV SDRAM
Each TDQS_C pin of DDRIV SDRAM
Each TDQS_T pin of DDRIV SDRAM


U37
SCL
EVENT_n
EVENT_n
SA0 SA1 SA2
SDA
SA0 SA1 SA2
Serial PD with Thermal sensor
TDFN-8(MLP)
VDDSPD
Serial PD
0.1uF
VPP
U2-U6,U8-U20
0.1uF
VDD
U2-U6,U8-U20
0.1uF
VTT
U2-U6,U8-U20
VREFCA
U2-U6,U8-U20
VSS
U2-U6,U8-U20

3.4 DQ Map

Table 6 - DQ Map_SCC16GP03H4F1C-32AA

Module Pin No.	Module DQ	Damping RES.	IC No.	IC DQ	Module Pin No.	Module DQ	Damping RES.	IC No.	IC DQ
5	0	R8	U11	4	16	8	R14	U1	3
150	1	R129		6	161	9	R123		1
12	2	R12		7	23	10	R18		0
157	3	R125		5	168	11	R119		2
3	4	R7		0	14	12	R13		5
148	5	R130		2	159	13	R124		7
10	6	R11		1	21	14	R17		6
155	7	R126		3	166	15	R120		4
27	16	R20	U10	4	38	24	R26	U2	3
172	17	R117		6	183	25	R111		1
34	18	R24		7	45	26	R30		0
179	19	R113		5	190	27	R107		2
25	20	R19		0	36	28	R25		5
170	21	R118		2	181	29	R112		7
32	22	R23		1	43	30	R29		6
177	23	R114		3	188	31	R108		4
49	CB0	R32	U9	4	97	32	R41	U8	4
194	CB1	R105		6	242	33	R93		6
56	CB2	R36		7	104	34	R45		7
201	CB3	R101		5	249	35	R89		5
47	CB4	R31		0	95	36	R40		0
192	CB5	R106		2	240	37	R94		2
54	CB6	R35		1	102	38	R44		1
199	CB7	R102		3	247	39	R90		3
108	40	R47	U5	3	119	48	R53	U7	4
253	41	R87		1	264	49	R81		6
115	42	R51		0	126	50	R57		7
260	43	R83		2	271	51	R77		5
106	44	R46		5	117	52	R52		0
251	45	R88		7	262	53	R82		2
113	46	R50		6	124	54	R56		1
258	47	R84		4	269	55	R78		3
130	56	R59	U6	3					
275	57	R75		1					
137	58	R63		0					
282	59	R71		2					
128	60	R58		5					
273	61	R76		7					
135	62	R62		6					
280	63	R72		4					

Table 7 - DQ Map_SCC32GP13H4F1C-32AA

Module Pin NO.	Module DQ NO.	Damping RES.	R0 IC NO.	R0 IC DQ	R1 IC NO.	R1 IC DQ	Module Pin NO.	Module DQ NO.	Damping RES.	R0 IC NO.	R0 IC DQ	R1 IC NO.	R1 IC DQ
5	0	RDQ00	U00	1	U09	0	16	8	RDQ08	U01	1	U10	0
150	1	RDQ01		3		2	161	9	RDQ09		3		2
12	2	RDQ02		2		3	23	10	RDQ10		2		3
157	3	RDQ03		0		1	168	11	RDQ11		0		1
3	4	RDQ04		5		4	14	12	RDQ12		5		4
148	5	RDQ05		7		6	159	13	RDQ13		7		6
10	6	RDQ06		6		7	21	14	RDQ14		6		7
155	7	RDQ07		4		5	166	15	RDQ15		4		5
27	16	RDQ16	U02	0	U11	4	38	24	RDQ24	U03	0	U12	0
172	17	RDQ17		2		6	183	25	RDQ25		2		2
34	18	RDQ18		3		5	45	26	RDQ26		3		3
179	19	RDQ19		1		7	190	27	RDQ27		1		1
25	20	RDQ20		4		0	36	28	RDQ28		4		4
170	21	RDQ21		6		2	181	29	RDQ29		6		6
32	22	RDQ22		7		1	43	30	RDQ30		7		7
177	23	RDQ23		5		3	188	31	RDQ31		5		5
49	CB0	RDQ64	U08	1	U17	0	97	32	RDQ32	U04	1	U13	0
194	CB1	RDQ65		3		2	242	33	RDQ33		3		2
56	CB2	RDQ66		2		3	104	34	RDQ34		2		3
201	CB3	RDQ67		0		1	249	35	RDQ35		0		1
47	CB4	RDQ68		5		4	95	36	RDQ36		5		4
192	CB5	RDQ69		7		6	240	37	RDQ37		7		6
54	CB6	RDQ70		6		7	102	38	RDQ38		6		7
199	C1	RDQ71		4		5	247	39	RDQ39		4		5
108	40	RDQ40	U05	1	U14	0	119	48	RDQ48	U06	3	U15	0
253	41	RDQ41		3		2	264	49	RDQ49		1		2
115	42	RDQ42		2		3	126	50	RDQ50		2		3
260	43	RDQ43		0		1	271	51	RDQ51		0		1
106	44	RDQ44		5		4	117	52	RDQ52		7		4
251	45	RDQ45		7		6	262	53	RDQ53		5		6
113	46	RDQ46		6		7	124	54	RDQ54		6		7
258	47	RDQ47		4		5	269	55	RDQ55		4		5
130	56	RDQ56	U07	1	U16	2							
275	57	RDQ57		3		0							
137	58	RDQ58		2		3							
282	59	RDQ59		0		1							
128	60	RDQ60		5		6							
273	61	RDQ61		7		4							
135	62	RDQ62		6		7							
280	63	RDQ63		4		5							

4 Electrical Characteristics

This chapter contains speed grade definition, AC timing parameter and ODT tables.

4.1 Absolute Maximum Ratings

Attention: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 8 - Absolute Maximum Ratings

Symbol	Parameter	Rating		Unit	Note
		Min.	Max.		
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}	-0.4	+1.5	V	
V_{DDQ}	Voltage on V_{DDQ} pin relative to V_{SS}	-0.4	+1.5	V	
V_{PP}	Voltage on V_{PP} pin relative to V_{SS}	-0.4	3.0	V	
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	-0.4	+1.5	V	
T_{STG}	Storage Temperature	-50	+100	℃	

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to integrated circuit.

Table 9 - DRAM Component Operating Temperature Range

Symbol	Parameter	Rating		Unit	Note
		Min.	Max.		
T_{CASE}	Operating Temperature	0	95	°C	1)2)3)4)

1) Operating Temperature is the case surface temperature on the center / top side of the DRAM.
2) The operating temperature ranges are the temperatures where all DRAM specification will be supported. During operation, the DRAM case temperature must be maintained between 0 - 95 °C under all other specification parameters.
3) Above 85 ℃ the Auto-Refresh command interval has to be reduced to t_{REFI}= 3.9 µs
4) When operating this product in the 85 °C to 95 °C T_{CASE} temperature range, the High Temperature Self Refresh has to be enabled by setting EMR(2) bit A7 to "1".

4.2 Operating Conditions

Table 10 - Supply Voltage Levels and AC / DC Operating Conditions

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Device Supply Voltage	V_{DD}	1.14	1.2	1.26	V	1),2),3)
Output Supply Voltage	V_{DDQ}	1.14	1.2	1.26	V	1),2),3)
Peak-to-Peak Voltage	V_{PP}	2.375	2.5	2.75	V	3)
Input Reference Voltage	V_{REF}	$0.49 \times V_{DD}$	$0.5 \times V_{DDQ}$	$0.51 \times V_{DD}$	V	
DC Input Logic High	$V_{IH.CA(DC65)}$	$V_{REFCA} + 0.065$	—	V_{DD}	V	
DC Input Logic Low	$V_{IL.CA\ (DC65)}$	Vss	—	$V_{REFCA} - 0.065$	V	
AC Input Logic High	$V_{IH.CA(AC90)}$	$V_{REF} + 0.09$	—		V	
AC Input Logic Low	$V_{IL.CA\ (AC90)}$		—	$V_{REF} - 0.09$	V	

Notes:

1) Under all conditions VDDQ must be less than or equal to VDD.
2) VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3) DC bandwidth is limited to 20MHz.

4.3 Module and Component Speed Grades

DDR4 components may exceed the listed module speed grades; module may not be available in all listed speed grades

Table 11 - Module and Component Speed Grades

Module Speed Grade	Component Speed Grade
-32AA	3200-22-22-22

4.4 I_{DD}/ I_{PP} Specifications and Conditions

List of tables defining I_{DD} /I_{PP} Specifications and Conditions.

Table 12 - I_{DD} / I_{PP} Measurement Conditions

Symbol	Description
IDD0 IPP0	Operating One Bank Active-Precharge Current (AL=0) CKE: High; External clock: On; tCK, nRC, nRAS, CL: Refer to Component Datasheet for detail pattern; BL: 8[1]; AL: 0; CS_n: High between ACT and PRE; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern
IDD1 IPP1	Operating One Bank Active-Read-Precharge Current (AL=0) CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: Refer to Component Datasheet for detail pattern; BL: 8[1]; AL: 0; CS_n: High between ACT, RD and PRE; Command, Address, Bank Group Address, Bank Address Inputs, Data IO: partially toggling; DM_n: stable at 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern
IDD2N IPP2N	Precharge Standby Current (AL=0) CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8[1]; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern
IDD2NT	Precharge Standby ODT Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8[1]; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VSSQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: toggling according ; Pattern Details: Refer to Component Datasheet for detail pattern
IDD2P IPP2P	Precharge Power-Down Current CKE: Low; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8[1]; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at 0
IDD2Q	Precharge Quiet Standby Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8[1]; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1;Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at 0

Symbol	Description
IDD3N IPP3N	Active Standby Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8[1]; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling Data IO: VDDQ; DM_n: stable at 1;Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at 0; Pattern Details:Refer to Component Datasheet for detail pattern
IDD3P IPP3P	Active Power-Down Current CKE: Low; External clock: On; tCK, CL: sRefer to Component Datasheet for detail pattern; BL: 8[1]; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at 0
IDD4R IPP4R	Operating Burst Read Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8[2]; AL: 0; CS_n: High between RD; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: seamless read data burst with different data between one burst and the next one according ; DM_n: stable at 1; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern
IDD4W IPP4W	Operating Burst Write Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8[1]; AL: 0; CS_n: High between WR; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: seamless write data burst with different data between one burst and the next one ; DM_n: stable at 1; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at HIGH; Pattern Details: Refer to Component Datasheet for detail pattern
IDD5B IPP5B	Burst Refresh Current (1X REF) CKE: High; External clock: On; tCK, CL, nRFC: Refer to Component Datasheet for detail pattern; BL: 8[1]; AL: 0; CS_n: High between REF; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: REF command every nRFC ; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern
IDD5F2 IPP5F2	Burst Refresh Current (2X REF) tRFC=tRFC_x2,
IDD5F4 IPP5F4	Burst Refresh Current (4X REF) tRFC=tRFC_x4,
IDD6N IPP6N	Self Refresh Current: Normal Temperature Range Tcase: 0 - 85°C; Low Power Array Self Refresh (LP ASR) : Normal4; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 8[1]; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM n: stable at 1; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MIDLEVEL
IDD6E IPP6E	Self-Refresh Current: Extended Temperature Range) TCase: 0 - 95°C; Low Power Array Self Refresh (LP ASR) : Extended4; CKE: Low; External clock: Off; CK_t and CK_c: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 8[1]; AL: 0; CS_n, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MID-LEVEL

Symbol	Description
IDD6R IPP6R	Self-Refresh Current: Reduced Temperature Range TCase: 0 - 45°C; Low Power Array Self Refresh (LP ASR) : Reduced[4]; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 8[1]; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: MID-LEVEL
IDD6A IPP6A	Auto Self-Refresh Current TCase: 0 - 95°C; Low Power Array Self Refresh (LP ASR) : Auto[4]; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 8[1]; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Auto Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: MID-LEVEL
IDD7 IPP7	Operating Bank Interleave Read Current CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: Refer to Component Datasheet for detail pattern; BL: 8[1]; AL: CL-1; CS_n: High between ACT and RDA; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: read data bursts with different data between one burst and the next one ; DM_n: stable at 1; Bank Activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern
IDD8 IPP8	Maximum Power Down Current TBD

Notes :

1. Burst Length: BL8 fixed by MRS: set MR0 [A1:0=00].
2. Output Buffer Enable - set MR1 [A12 = 0] : Qoff = Output buffer enabled - set MR1 [A2:1 = 00] : Output Driver Impedance Control = RZQ/7 RTT_Nom enable - set MR1 [A10:8 = 011] : RTT_NOM = RZQ/6 RTT_WR enable - set MR2 [A10:9 = 01] : RTT_WR = RZQ/2 RTT_PARK disable - set MR5 [A8:6 = 000]
3. CAL enabled : set MR4 [A8:6 = 001] : 1600MT/s 010] : 1866MT/s, 2133MT/s 011] : 2400MT/s Gear Down mode enabled :set MR3 [A3 = 1] : 1/4 Rate DLL disabled : set MR1 [A0 = 0] CA parity enabled :set MR5 [A2:0 = 001] : 1600MT/s,1866MT/s, 2133MT/s 010] : 2400MT/s Read DBI enabled : set MR5 [A12 = 1] Write DBI enabled : set :MR5 [A11 = 1]
4. Low Power Array Self Refresh (LP ASR) : set MR2 [A7:6 = 00] : Normal 01] : Reduced Temperature range 10] : Extended Temperature range 11] : Auto Self Refresh

Table 13 - I_{DD} Specification for SCC16GP03H4F1C-32AA and SCC32GP13H4F1C-32AA

Product Type	SCC16GP03H4F1C-32AA	SCC32GP13H4F1C-32AA	Unit	Note
Organization	16GB	32GB		
	1 Rank (×8)	2Rank (×8)		
	×72	×72		
	-32AA	-32AA		
Symbol	Current	Current		
IDD0	414	648	mA	2)
IDD1	486	720	mA	2)
IDD2N	324	648	mA	3)
IDD2NT	360	594	mA	2)
IDD2P	234	468	mA	3)
IDD2Q	306	612	mA	3)
IDD3N	666	1332	mA	3)
IDD3P	585	1170	mA	3)
IDD4R	1341	1575	mA	2)
IDD4W	1287	1521	mA	2)
IDD5B	5211	5445	mA	2)
IDD5F2	3591	3825	mA	2)
IDD5F4	2979	3213	mA	2)
IDD6N	423	846	mA	3)
IDD6E	630	1260	mA	3)
IDD6R	198	396	mA	3)
IDD6A	693	1386	mA	3)
IDD7	1440	1674	mA	2)
IDD8	135	270	mA	3)

1) Calculated values from Device data.
2) One module rank in the active IDD/IPP, the other rank in IDD2P/IPP3N.
3) All ranks in this IDD/IPP condition

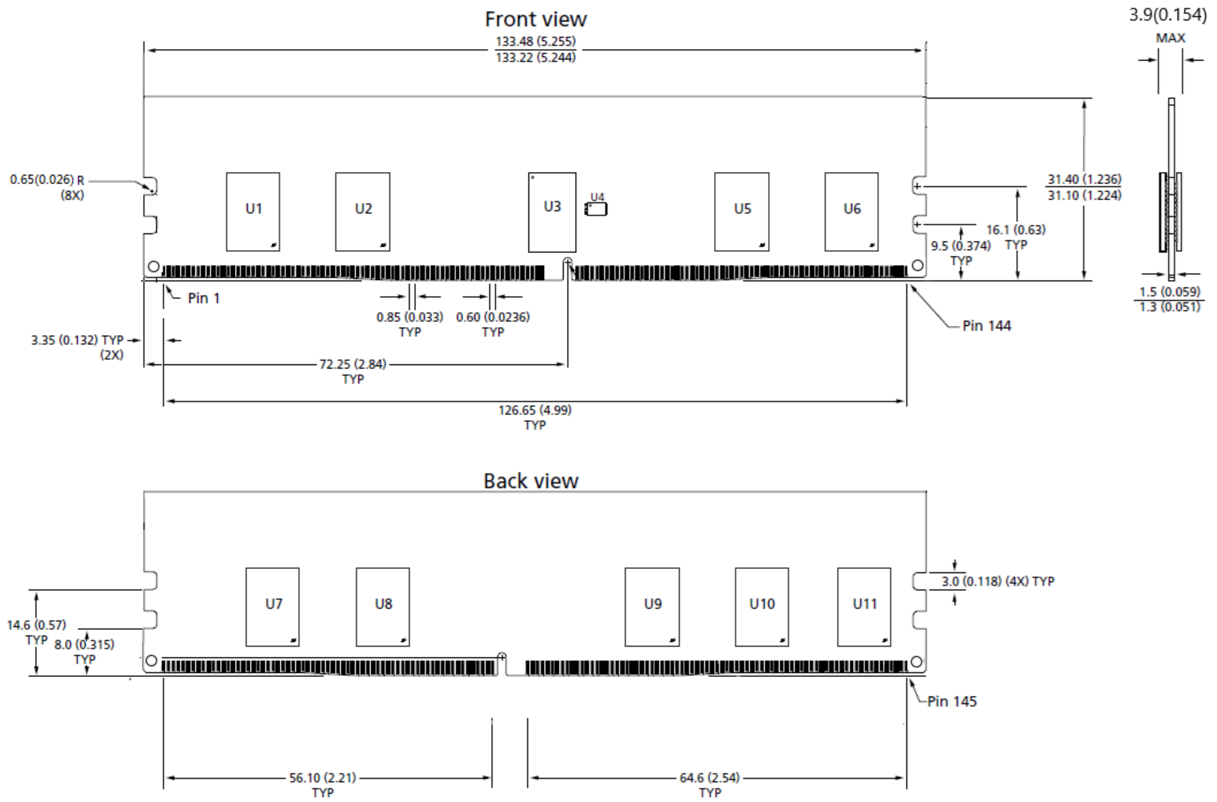
Table 14 - I_{PP} Specification for SCC16GP03H4F1C-32AA and SCC32GP13H4F1C-32AA

Product Type	SCC16GP03H4F1C-32AA	SCC32GP13H4F1C-32AA	Unit	Note
Organization	16GB	32GB		
	1 Rank (×8)	2Rank (×8)		
	×72	×72		
	-32AA	-32AA		
Symbol	Current	Current		
IPP0	28.8	48.6	mA	2)
IPP1	31.5	51.3	mA	2)
IPP2N	17.1	34.2	mA	3)
IPP2P	17.1	34.2	mA	3)
IPP3N	19.8	39.6	mA	3)
IPP3P	19.8	39.6	mA	3)
IPP4R	46.8	66.6	mA	2)
IPP4W	46.8	66.6	mA	2)
IPP5B	513	532.8	mA	2)
IPP5F2	360	379.8	mA	2)
IPP5F4	297	316.8	mA	2)
IPP6N	43.2	86.4	mA	3)
IPP6E	68.4	136.8	mA	3)
IPP6R	26.1	52.2	mA	3)
IPP6A	60.3	120.6	mA	3)
IPP7	136.8	156.6	mA	2)
IPP8	17.1	34.2	mA	3)

1) Calculated values from Device data.
2) One module rank in the active IDD/IPP, the other rank in IDD2P/IPP3N.
3) All ranks in this IDD/IPP condition

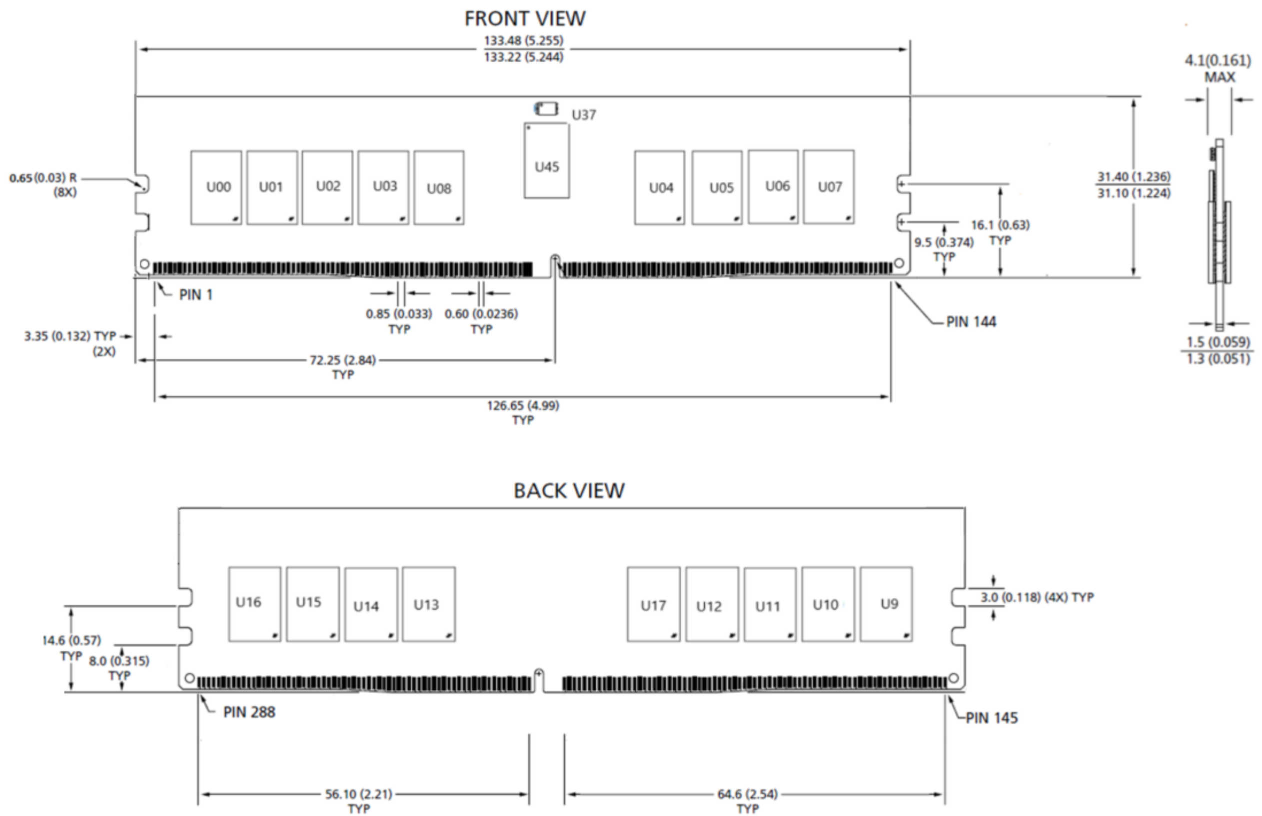
5 Package Dimensions

Figure 3 - Package Dimensions_SCC16GP03H4F1C-32AA



Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only.

Figure 4 - Package Dimensions_SCC32GP13H4F1C-32AA



Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only.

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Edition 2022-09
Published by
Xi'an UniIC Semiconductors Co., Ltd.

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