

Jan. 2021



HXMSH16P13A2F2CL16K

**240-Pin DDR3 Low Power Registered DIMM (x72, ECC)
EU RoHS Compliant**

Data Sheet

Rev. A

| Revision History | | |
|------------------|----------|--|
| Date | Revision | Subjects (major changes since last revision) |
| 2021-01 | A | Initial Release |

We Listen to Your Comments

Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to: info@unisemicon.com

Contents

| | |
|---|----|
| Contents..... | 3 |
| 1 Overview..... | 4 |
| 1.1 Features | 4 |
| 1.2 Description | 5 |
| 2 Pin Configurations..... | 6 |
| 2.1 Pin Configurations | 6 |
| 3 General Description | 14 |
| 3.1 General Description..... | 14 |
| 3.2 Fly-by topology | 14 |
| 3.3 Serial Presence-Detect EEPROM Operation | 14 |
| 3.4 Register and PLL Operation | 14 |
| 4 Electrical Characteristics..... | 15 |
| 4.1 Absolute Maximum Ratings | 15 |
| 4.2 Operating Conditions | 16 |
| 4.3 Module and Component Speed Grades | 17 |
| 4.4 AC Timing Requirements | 18 |
| 4.5 I_{DD} Specifications and Conditions..... | 19 |
| 5 Package Dimensions | 22 |
| List of Figures..... | 23 |
| List of Tables | 24 |

1 Overview

This chapter gives an overview of the 240-pin Low Power Register DDR3 SDRAM modules product family and describes its main characteristics.

1.1 Features

- 240-Pin PC3-12800 DDR3 LowPower RDIMM.
- 16GB Modules built with 8Gbit DDR3 SDRAMs in chipsize package FBGA-78 ball.
- VDD=1.35V(1.283~1.45V)
- VDD=1.5V(1.425~1.575V)
- All speed grades faster than DDR3-1600 complies with DDR3-1600 timing specifications.
- Programmable CAS Latencies (6, 7, 8, 9,10,11), Burst Length 8, Burst Chop 4 (BC4) .
- Auto Refresh (CBR) and Self Refresh.
- Auto Refresh for temperatures above 85 °C $t_{REFI} = 3.9 \mu\text{s}$.
- Programmable self refresh rate via EMRS2 setting.
- Programmable partial array refresh via EMRS2 settings.
- DCC enabling via EMRS2 setting.
- All inputs and outputs SSTL_1.5 compatible.
- Off-Chip Driver Impedance Adjustment (OCD) and On-Die Termination (ODT).
- Serial Presence Detect with E²PROM.
- RDIMM Dimensions (nominal): 30mm high, 133.35 mm wide
- Based on standard reference layouts.

Table 1 - Module Performance Table

| UnilC Speed Code | | -16K | Unit | Note |
|-------------------------|-----------|----------|----------|------|
| DRAM Speed Grade | DDR3 | -1600 | MT/S | |
| CAS-RCD-RP latencies | | 11-11-11 | t_{CK} | |
| Min. RAS-CAS-Delay | t_{RCD} | 13.125 | ns | |
| Min. Row Precharge Time | t_{RP} | 13.125 | ns | |
| Min. Row Active Time | t_{RAS} | 35 | ns | |
| Min. Row Cycle Time | t_{RC} | 48.125 | ns | |

1.2 Description

The UnilC 16GB module family is Register DIMM modules with 30mm height based on DDR3 technology. DIMMs are intended for mounting into 240-pin connector sockets.

The memory array is designed with 8Gbit Double-Data- Rate-Three (DDR3) Synchronous DRAMs. Decoupling capacitors are mounted on the PCB board. The DIMMs feature serial presence detect based on a serial E²PROM device using the 2-pin I²C protocol. The first 128 bytes are programmed with configuration data and are write protected; the second 128 bytes are available to the customer.



Table 2 - Ordering Information

| Product Type ¹⁾ | Compliance Code ²⁾ | Description | SDRAM Technology |
|------------------------------|-------------------------------|--------------|------------------|
| PC3L-12800 (11-11-11) | | | |
| HXMSH16P13A2F2CL16K | 16GB 2R×8 PC3L-12800-11-11-11 | 2 Ranks, ECC | 8Gbit (×8) |

- 1) For detailed information regarding Product Type of UnilC please see chapter "Product Type Nomenclature" of this data sheet.
- 2) The Compliance Code is printed on the module label and describes the speed grade, for example "PC3-12800-11-11-11" where 12800 means Register DIMM modules with 12.80 GB/sec Module Bandwidth and "11-11-11" means Column Address Strobe (CAS) latency=11, Row Column Delay (RCD) latency = 11 and Row Precharge (RP) latency = 11.

Table 3 - Address Format

| | |
|-----------------------------|-----------------------|
| DIMM Density | 16GB(2Rx8,X72) |
| Row address | 64K A[15:0] |
| Column address | 2K A[11, 9:0] |
| Device bank address | 8 BA[2:0] |
| Device configuration | 8Gb(1024Mx8) |
| Module rank address | 2 CS_n[1:0] |
| Device Quantity | 18 |

2 Pin Configurations

2.1 Pin Configurations

The pin configuration of the DDR3 RDIMM is listed by function in [Table 4](#) (240 pins). The abbreviations used in columns Pin Type and Buffer Type are explained in [Table 5](#) and [Table 6](#) respectively. The Pin numbering is depicted in [Table 7](#)

Table 4 - Pin Configuration of DDR3 RDIMM

| Pin No. | Name | Pin Type | Buffer Type | Function |
|------------------------|------|----------|-------------|--|
| Clock Signals | | | | |
| 184 | CK0 | I | SSTL | Clock Signals CK0, Complement Clock Signals bCK0 The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and the falling edge of bCK. A Delay Locked Loop (DLL) circuit is driven from the clock inputs and output timing for read operations is synchronized to the input clock. |
| 185 | bCK0 | I | SSTL | |
| 50 | CKE0 | I | SSTL | Clock Enable Rank 1:0 Activates the DDR3 SDRAM CK signal when HIGH and deactivates the CK signal when LOW. By deactivating the clocks, CKE LOW initiates the Power Down Mode or the Self Refresh Mode. <i>Note: 2 Ranks module</i> |
| 169 | CKE1 | I | SSTL | |
| | NC | NC | — | Not Connected |
| Control Signals | | | | |
| 193 | bS0 | I | SSTL | Chip Select Rank 1:0 Enables the associated DDR3 SDRAM command decoder when LOW and disables the command decoder when HIGH. When the command decoder is disabled, new commands are ignored but previous operations continue. Rank 0 is selected by bS0; Rank 1 is selected by bS1. Rank 2 is selected by Bs2; Rank 3 is selected by bS3. Ranks are also called "Physical banks". |
| 76 | bS1 | I | SSTL | |
| 79 | bS2 | I | SSTL | |
| 198 | bS3 | I | SSTL | |
| 192 | bRAS | I | SSTL | Row Address Strobe When sampled at the cross point of the rising edge of CK, and falling edge of bCK, bRAS, bCAS and bWE define the operation to be executed by the SDRAM. |
| 74 | bCAS | I | SSTL | Column Address Strobe |

| Pin No. | Name | Pin Type | Buffer Type | Function |
|------------------------|--------|----------|-------------|---|
| 73 | bWE | I | SSTL | Write Enable |
| 168 | bRESET | I | SSTL | Register Reset |
| Address Signals | | | | |
| 71 | BA0 | I | SSTL | Bank Address Bus 2:0 Selects which DDR3 SDRAM internal bank of four or eight is activated. |
| 190 | BA1 | I | SSTL | |
| 52 | BA2 | I | SSTL | Bank Address Bus 2 Greater than 512Mb DDR3 SDRAMS |
| | NC | NC | SSTL | Less than 1Gb DDR3 SDRAMS |
| 188 | A0 | I | SSTL | Address Bus 12:0 During a Bank Activate command cycle, defines the row address when sampled at the cross-point of the rising edge of CK and falling edge of bCK. During a Read or Write command cycle, defines the column address when sampled at the cross point of the rising edge of CK and falling edge of bCK. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is HIGH, autoprecharge is selected and BA0-BAn defines the bank to be precharged. If AP is LOW, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0-BAn to control which bank(s) to precharge. If AP is HIGH, all banks will be precharged regardless of the state of BA0-BAn inputs. If AP is LOW, then BA0-BAn are used to define which bank to precharge. |
| 181 | A1 | I | SSTL | |
| 61 | A2 | I | SSTL | |
| 180 | A3 | I | SSTL | |
| 59 | A4 | I | SSTL | |
| 58 | A5 | I | SSTL | |
| 178 | A6 | I | SSTL | |
| 56 | A7 | I | SSTL | |
| 177 | A8 | I | SSTL | |
| 175 | A9 | I | SSTL | |
| 70 | A10 | I | SSTL | |
| | AP | I | SSTL | |
| 55 | A11 | I | SSTL | |
| 174 | A12 | I | SSTL | Address Signal 12 <i>Note: Module based on 256 Mbit or larger dies</i> |
| 196 | A13 | I | SSTL | Address Signal 13 <i>Note: 1 Gbit based module</i> |
| | NC | NC | — | Not Connected <i>Note: Module based on 512 Mbit or smaller dies</i> |
| 172 | A14 | I | SSTL | Address Signal 14 <i>Note: 2 Gbit based module</i> |
| 171 | A15 | I | SSTL | Address Signal 15 <i>Note: 4 Gbit based module</i> |
| Data Signals | | | | |
| 3 | DQ0 | I/O | SSTL | Data Bus 63:0 <i>Note: Data Input / Output pins</i> |
| 4 | DQ1 | I/O | SSTL | |
| 9 | DQ2 | I/O | SSTL | |
| 10 | DQ3 | I/O | SSTL | |
| 122 | DQ4 | I/O | SSTL | |
| 123 | DQ5 | I/O | SSTL | |
| 128 | DQ6 | I/O | SSTL | |
| 129 | DQ7 | I/O | SSTL | |
| 12 | DQ8 | I/O | SSTL | |

| Pin No. | Name | Pin Type | Buffer Type | Function |
|---------|------|----------|-------------|---|
| 13 | DQ9 | I/O | SSTL | Data Bus 63:0 <i>Note: Data Input / Output pins</i> |
| 18 | DQ10 | I/O | SSTL | |
| 19 | DQ11 | I/O | SSTL | |
| 131 | DQ12 | I/O | SSTL | |
| 132 | DQ13 | I/O | SSTL | |
| 137 | DQ14 | I/O | SSTL | |
| 138 | DQ15 | I/O | SSTL | |
| 21 | DQ16 | I/O | SSTL | |
| 22 | DQ17 | I/O | SSTL | |
| 27 | DQ18 | I/O | SSTL | |
| 28 | DQ19 | I/O | SSTL | |
| 140 | DQ20 | I/O | SSTL | |
| 141 | DQ21 | I/O | SSTL | |
| 146 | DQ22 | I/O | SSTL | |
| 147 | DQ23 | I/O | SSTL | |
| 30 | DQ24 | I/O | SSTL | |
| 31 | DQ25 | I/O | SSTL | |
| 36 | DQ26 | I/O | SSTL | |
| 37 | DQ27 | I/O | SSTL | |
| 149 | DQ28 | I/O | SSTL | |
| 150 | DQ29 | I/O | SSTL | |
| 155 | DQ30 | I/O | SSTL | |
| 156 | DQ31 | I/O | SSTL | |
| 81 | DQ32 | I/O | SSTL | |
| 82 | DQ33 | I/O | SSTL | |
| 87 | DQ34 | I/O | SSTL | |
| 88 | DQ35 | I/O | SSTL | |
| 200 | DQ36 | I/O | SSTL | |
| 201 | DQ37 | I/O | SSTL | |
| 206 | DQ38 | I/O | SSTL | |
| 207 | DQ39 | I/O | SSTL | |
| 90 | DQ40 | I/O | SSTL | |
| 91 | DQ41 | I/O | SSTL | |
| 96 | DQ42 | I/O | SSTL | |
| 97 | DQ43 | I/O | SSTL | |
| 209 | DQ44 | I/O | SSTL | |
| 210 | DQ45 | I/O | SSTL | |
| 215 | DQ46 | I/O | SSTL | |
| 216 | DQ47 | I/O | SSTL | |
| 99 | DQ48 | I/O | SSTL | |

| Pin No. | Name | Pin Type | Buffer Type | Function |
|----------------------------|-------|----------|-------------|--|
| 100 | DQ49 | I/O | SSTL | Data Bus 63:0 Note: Data Input / Output pins |
| 105 | DQ50 | I/O | SSTL | |
| 106 | DQ51 | I/O | SSTL | |
| 218 | DQ52 | I/O | SSTL | |
| 219 | DQ53 | I/O | SSTL | |
| 224 | DQ54 | I/O | SSTL | |
| 225 | DQ55 | I/O | SSTL | |
| 108 | DQ56 | I/O | SSTL | |
| 109 | DQ57 | I/O | SSTL | |
| 114 | DQ58 | I/O | SSTL | |
| 115 | DQ59 | I/O | SSTL | |
| 227 | DQ60 | I/O | SSTL | |
| 228 | DQ61 | I/O | SSTL | |
| 233 | DQ62 | I/O | SSTL | |
| 234 | DQ63 | I/O | SSTL | |
| Check Bits | | | | |
| 39 | CB0 | I/O | SSTL | Check Bits 7:0 Check Bit Input/Output Note: NC on Non-ECC modules |
| 40 | CB1 | I/O | SSTL | |
| 45 | CB2 | I/O | SSTL | |
| 46 | CB3 | I/O | SSTL | |
| 158 | CB4 | I/O | SSTL | |
| 159 | CB5 | I/O | SSTL | |
| 164 | CB6 | I/O | SSTL | |
| 165 | CB7 | I/O | SSTL | |
| Data Strobe Signals | | | | |
| 7 | DQS0 | I/O | SSTL | Data Strobe Bus 7:0 and Complementary Data Strobe Bus 7:0 The data strobes, associated with one data byte, sourced with data transfers. In Write mode, the data strobe is sourced by the controller and is centered in the data window. In Read mode the data strobe is sourced by the DDR3 SDRAM and is sent at the leading edge of the data window. bDQS signals are complements, and timing is relative to the cross-point of respective DQS and bDQS. If the module is to be operated in single ended strobe mode, all bDQS signals must be tied on the system board to VSS and DDR3 SDRAM mode registers programmed appropriately |
| 6 | bDQS0 | I/O | SSTL | |
| 16 | DQS1 | I/O | SSTL | |
| 15 | bDQS1 | I/O | SSTL | |
| 25 | DQS2 | I/O | SSTL | |
| 24 | bDQS2 | I/O | SSTL | |
| 34 | DQS3 | I/O | SSTL | |
| 33 | bDQS3 | I/O | SSTL | |
| 85 | DQS4 | I/O | SSTL | |
| 84 | bDQS4 | I/O | SSTL | |
| 94 | DQS5 | I/O | SSTL | |
| 93 | bDQS5 | I/O | SSTL | |
| 103 | DQS6 | I/O | SSTL | |
| 102 | bDQS6 | I/O | SSTL | |
| 112 | DQS7 | I/O | SSTL | |
| 111 | bDQS7 | I/O | SSTL | |

| Pin No. | Name | Pin Type | Buffer Type | Function |
|------------------|--------|----------|-------------|---|
| 43 | DQS8 | I/O | SSTL | |
| 42 | bDQS8 | I/O | SSTL | |
| 125 | DQS9 | I/O | SSTL | |
| 126 | bDQS9 | I/O | SSTL | |
| 134 | DQS10 | I/O | SSTL | |
| 135 | bDQS10 | I/O | SSTL | |
| 143 | DQS11 | I/O | SSTL | |
| 144 | bDQS11 | I/O | SSTL | |
| 152 | DQS12 | I/O | SSTL | |
| 153 | bDQS12 | I/O | SSTL | |
| 203 | DQS13 | I/O | SSTL | |
| 204 | bDQS13 | I/O | SSTL | |
| 212 | DQS14 | I/O | SSTL | |
| 213 | bDQS14 | I/O | SSTL | |
| 221 | DQS15 | I/O | SSTL | |
| 222 | bDQS15 | I/O | SSTL | |
| 230 | DQS16 | I/O | SSTL | |
| 231 | bDQS16 | I/O | SSTL | |
| 161 | DQS17 | I/O | SSTL | |
| 162 | bDQS17 | I/O | SSTL | |
| Data Mask | | | | |
| 125 | DM0 | I/O | SSTL | Data Masks 7:0 The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is LOW but blocks the write operation if it is HIGH. In Read mode, DM lines have no effect. <i>Note:x8 based module</i> |
| 134 | DM1 | I/O | SSTL | |
| 143 | DM2 | I/O | SSTL | |
| 152 | DM3 | I/O | SSTL | |
| 203 | DM4 | I/O | SSTL | |
| 212 | DM5 | I/O | SSTL | |
| 221 | DM6 | I/O | SSTL | |
| 230 | DM7 | I/O | SSTL | |
| 161 | DM8 | I/O | SSTL | |

| Pin No. | Name | Pin Type | Buffer Type | Function |
|---|--------------|----------|-------------|---|
| EEPROM | | | | |
| 118 | SCL | I | CMOS | Serial Bus Clock This signal is used to clock data into and out of the SPD EEPROM and Thermal sensor. |
| 238 | SDA | I/O | OD | Serial Bus Data This is a bidirectional pin used to transfer data into and out of the SPD EEPROM and Thermal sensor. A resistor must be connected from SDA to V_{DDSPD} on the motherboard to act as a pull-up. |
| 117 | SA0 | I | CMOS | Serial Address Select Bus 1:0 Address pins used to select the SPD and Thermal sensor base address. |
| 237 | SA1 | I | CMOS | |
| 119 | SA2 | I | CMOS | |
| Parity | | | | |
| 53 | bERR_O UT | O | CMOS | Parity bits <i>Note: Only for modules with parity bit for address and control bus. Not connected on non-parity registered modules.</i> |
| 68 | PAR_IN | I | CMOS | |
| Power Supplies | | | | |
| 1 | V_{REFDQ} | AI | — | I/O Reference Voltage Reference voltage for the SSTL-18 inputs. |
| 48,49,120,240 | V_{tt} | PWR | — | Termination Voltage Termination voltage for command and address. |
| 236 | V_{DDSPD} | PWR | — | EEPROM Power Supply Power supplies for Serial Presence Detect, Thermal Sensor and ground for the module. |
| 51,54,57,60,62,65,66,69,72,75,78, 170,173,176,179,182,183,186,189, 191,194,197 | V_{DD} | PWR | — | Power Supply Power supplies for core, I/O and ground for the module. |
| 2,5,8,11,14,17,20,23,26,29,32,35, 38,41,44,47,80,83,86,89,92,95,98, 101,104,107,110,113,116,121,124, 127,130,133,136,139,142,145,148, 151,154,157,160,163,166,199, 202,205,208,211,214,217,220,223, 226,229,232,235,239 | V_{SS} | GND | — | Ground Plane Power supplies for core, I/O, Serial Presence Detect, Thermal Sensor and ground for the module. |
| Other pins | | | | |
| 195 | ODT0 | I | SSTL | On-Die Termination Control 1:0 |
| 77 | ODT1 | I | SSTL | On-Die Termination Control 1 Asserts on-die termination for DQ, DM, DQS, and bDQS signals if enabled via the DDR3 SDRAM mode register. <i>Note: 2 Rank modules</i> |
| 63,64,126,135,144,153,162,204,213, 222,231 | NC | NC | — | Not Connected |

Table 5 - Abbreviations for pin Type

| Abbreviation | Description |
|--------------|---|
| I | Standard input-only pin. Digital levels. |
| O | Output. Digital levels. |
| I/O | I/O is a bidirectional input/output signal. |
| AI | Input. Analog levels. |
| PWR | Power |
| GND | Ground |
| NC | Not Connected |

Table 6 - Abbreviations for Buffer Type

| Abbreviation | Description |
|--------------|--|
| SSTL | Serial Stub Terminated Logic (SSTL_15) |
| LV-CMOS | Low Voltage CMOS |
| CMOS | CMOS Levels |
| OD | Open Drain. The corresponding pin has 2 operational states, active low and tri-state, and allows multiple devices to share as a wire-OR. |

Table 7 - Pin Configuration RDIMM (240 pin)

| Pin | Front | Pin | Front | Pin | Front | Pin | Back | Pin | Back | Pin | Back |
|-----|--------|-----|----------|-----|-------|-----|------|-----|--------|-----|--------|
| 1 | VREFDQ | 41 | VSS | 81 | DQ32 | 121 | VSS | 161 | DM8 | 201 | DQ37 |
| 2 | VSS | 42 | /DQS8 | 82 | DQ33 | 122 | DQ4 | 162 | NC | 202 | VSS |
| 3 | DQ0 | 43 | DQS8 | 83 | VSS | 123 | DQ5 | 163 | VSS | 203 | DM4 |
| 4 | DQ1 | 44 | VSS | 84 | /DQS4 | 124 | VSS | 164 | CB6 | 204 | NC |
| 5 | VSS | 45 | CB2 | 85 | DQS4 | 125 | DM0 | 165 | CB7 | 205 | VSS |
| 6 | /DQS0 | 46 | CB3 | 86 | VSS | 126 | NC | 166 | VSS | 206 | DQ38 |
| 7 | DQS0 | 47 | VSS | 87 | DQ34 | 127 | VSS | 167 | NC | 207 | DQ39 |
| 8 | VSS | 48 | VTT | 88 | DQ35 | 128 | DQ6 | 168 | /RESET | 208 | VSS |
| 9 | DQ2 | 49 | VTT | 89 | VSS | 129 | DQ7 | 169 | CKE1 | 209 | DQ44 |
| 10 | DQ3 | 50 | CKE0 | 90 | DQ40 | 130 | VSS | 170 | VDD | 210 | DQ45 |
| 11 | VSS | 51 | VDD | 91 | DQ41 | 131 | DQ12 | 171 | A15 | 211 | VSS |
| 12 | DQ8 | 52 | BA2 | 92 | VSS | 132 | DQ13 | 172 | A14 | 212 | DM5 |
| 13 | DQ9 | 53 | /ERR_OUT | 93 | /DQS5 | 133 | VSS | 173 | VDD | 213 | NC |
| 14 | VSS | 54 | VDD | 94 | DQS5 | 134 | DM1 | 174 | A12 | 214 | VSS |
| 15 | /DQS1 | 55 | A11 | 95 | VSS | 135 | NC | 175 | A9 | 215 | DQ46 |
| 16 | DQS1 | 56 | A7 | 96 | DQ42 | 136 | VSS | 176 | VDD | 216 | DQ47 |
| 17 | VSS | 57 | VDD | 97 | DQ43 | 137 | DQ14 | 177 | A8 | 217 | VSS |
| 18 | DQ10 | 58 | A5 | 98 | VSS | 138 | DQ15 | 178 | A6 | 218 | DQ52 |
| 19 | DQ11 | 59 | A4 | 99 | DQ48 | 139 | VSS | 179 | VDD | 219 | DQ53 |
| 20 | VSS | 60 | VDD | 100 | DQ49 | 140 | DQ20 | 180 | A3 | 220 | VSS |
| 21 | DQ16 | 61 | A2 | 101 | VSS | 141 | DQ21 | 181 | A1 | 221 | DM6 |
| 22 | DQ17 | 62 | VDD | 102 | /DQS6 | 142 | VSS | 182 | VDD | 222 | NC |
| 23 | VSS | 63 | NC | 103 | DQS6 | 143 | DM2 | 183 | VDD | 223 | VSS |
| 24 | /DQS2 | 64 | NC | 104 | VSS | 144 | NC | 184 | CK0 | 224 | DQ54 |
| 25 | DQS2 | 65 | VDD | 105 | DQ50 | 145 | VSS | 185 | /CK0 | 225 | DQ55 |
| 26 | VSS | 66 | VDD | 106 | DQ51 | 146 | DQ22 | 186 | VDD | 226 | VSS |
| 27 | DQ18 | 67 | VREFCA | 107 | VSS | 147 | DQ23 | 187 | /EVENT | 227 | DQ60 |
| 28 | DQ19 | 68 | PAR_IN | 108 | DQ56 | 148 | VSS | 188 | A0 | 228 | DQ61 |
| 29 | VSS | 69 | VDD | 109 | DQ57 | 149 | DQ28 | 189 | VDD | 229 | VSS |
| 30 | DQ24 | 70 | A10/AP | 110 | VSS | 150 | DQ29 | 190 | BA1 | 230 | DM7 |
| 31 | DQ25 | 71 | BA0 | 111 | /DQS7 | 151 | VSS | 191 | VDD | 231 | NC |
| 32 | VSS | 72 | VDD | 112 | DQS7 | 152 | DM3 | 192 | /RAS | 232 | VSS |
| 33 | /DQS3 | 73 | /WE | 113 | VSS | 153 | NC | 193 | /S0 | 233 | DQ62 |
| 34 | DQS3 | 74 | /CAS | 114 | DQ58 | 154 | VSS | 194 | VDD | 234 | DQ63 |
| 35 | VSS | 75 | VDD | 115 | DQ59 | 155 | DQ30 | 195 | ODT0 | 235 | VSS |
| 36 | DQ26 | 76 | /S1 | 116 | VSS | 156 | DQ31 | 196 | A13 | 236 | VDDSPD |
| 37 | DQ27 | 77 | ODT1 | 117 | SA0 | 157 | VSS | 197 | VDD | 237 | SA1 |
| 38 | VSS | 78 | VDD | 118 | SCL | 158 | CB4 | 198 | /S3 | 238 | SDA |
| 39 | CB0 | 79 | /S2 | 119 | SA2 | 159 | CB5 | 199 | VSS | 239 | VSS |
| 40 | CB1 | 80 | VSS | 120 | VTT | 160 | VSS | 200 | DQ36 | 240 | VTT |

3 General Description

3.1 General Description

DDR3 SDRAM modules are high-speed, CMOS dynamic random access memory modules that use internally configured 4 or 8-bank DDR3 SDRAM devices. DDR3 SDRAM modules use DDR architecture to achieve high-speed operation. DDR3 architecture is essentially a $8n$ -prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR3 SDRAM module effectively consists of a single $8n$ -bit-wide, one-clock-cycle data transfer at the internal DRAM core and eight corresponding n -bit-wide, one-half-clock-cycle data transfers at the I/O pins.

DDR3 modules use two sets of differential signals: DQS, DQS# to capture data and CK and CK# to capture commands, addresses, and control signals. Differential clocks and data strobes ensure exceptional noise immunity for these signals and provide precise crossing points to capture input signals. A bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR3 SDRAM device during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

DDR3 SDRAM modules operate from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

3.2 Fly-by topology

DDR3 modules use faster clock speeds than earlier DDR technologies, making signal quality more important than ever. For improved signal quality, the clock, control, command, and address buses have been routed in a fly-by topology, where each clock, control, command, and address pin on each DRAM is connected to a single trace and terminated (rather than a tree structure, where the termination is off the module near the connector). Inherent to fly-by topology, the timing skew between the clock and DQS signals can be easily accounted for by using the write-leveling feature of DDR3.

3.3 Serial Presence-Detect EEPROM Operation

DDR3 SDRAM modules incorporate serial presence-detect. The SPD data is stored in a 256-byte EEPROM. The first 128 bytes are programmed by UnilC to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I2C bus using the DIMM's SCL (clock) SDA (data), and SA (address) pins. Write protect (WP) is connected to VSS, permanently disabling hardware write protection.

3.4 Register and PLL Operation

DDR3 SDRAM modules operate in registered mode, where the command/address input signals are latched in the registers on the rising clock edge and sent to the DDR3 SDRAM devices on the following rising clock edge (data access is delayed by one clock cycle). A phase-lock loop (PLL) on the module receives and redrives the differential clock signals (CK, CK#) to the DDR3 SDRAM devices. The registers and PLL minimize system and clock loading. PLL clock timing is defined by JEDEC specifications and ensured by use of the JEDEC clock reference board. Registered mode will add one clock cycle to CL.

4 Electrical Characteristics

This chapter contains speed grade definition, AC timing parameter and ODT tables.

4.1 Absolute Maximum Ratings

Attention: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 8 - Absolute Maximum Ratings

| Symbol | Parameter | Rating | | Unit | Note |
|-------------------|---|--------|--------|------|------|
| | | Min. | Max. | | |
| V_{DD} | Voltage on V_{DD} pin relative to V_{SS} | -0.4 | +1.975 | V | |
| V_{DDQ} | Voltage on V_{DDQ} pin relative to V_{SS} | -0.4 | +1.975 | V | |
| V_{IN}, V_{OUT} | Voltage on any pin relative to V_{SS} | -0.4 | +1.975 | V | |
| T_{STG} | Storage Temperature | - 50 | +100 | °C | |

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to integrated circuit.

Table 9 - DRAM Component Operating Temperature Range

| Symbol | Parameter | Rating | | Unit | Note |
|------------|-----------------------|--------|------|------|----------|
| | | Min. | Max. | | |
| T_{CASE} | Operating Temperature | 0 | 95 | °C | 1)2)3)4) |

- 1) Operating Temperature is the case surface temperature on the center / top side of the DRAM.
- 2) The operating temperature ranges are the temperatures where all DRAM specification will be supported. During operation, the DRAM case temperature must be maintained between 0 - 95 °C under all other specification parameters.
- 3) Above 85 °C the Auto-Refresh command interval has to be reduced to $t_{REFI} = 3.9 \mu s$
- 4) When operating this product in the 85 °C to 95 °C T_{CASE} temperature range, the High Temperature Self Refresh has to be enabled by setting EMR(2) bit A7 to “1”.

4.2 Operating Conditions

Table 10 - Supply Voltage Levels and AC / DC Operating Conditions

| Parameter | Symbol | Values | | | Unit | Note |
|-----------------------------|--------------|-----------------------|----------------------|-----------------------|---------|------|
| | | Min. | Typ. | Max. | | |
| Device Supply Voltage | V_{DD} | 1.283 | 1.35 | 1.45 | V | |
| Output Supply Voltage | V_{DDQ} | 1.283 | 1.35 | 1.45 | V | 1) |
| Device Supply Voltage | V_{DD} | 1.425 | 1.5 | 1.575 | V | |
| Output Supply Voltage | V_{DDQ} | 1.425 | 1.5 | 1.575 | V | 1) |
| Input Reference Voltage | V_{REF} | $0.49 \times V_{DDQ}$ | $0.5 \times V_{DDQ}$ | $0.51 \times V_{DDQ}$ | V | 2) |
| SPD Supply Voltage | V_{DDSPD} | 3 | — | 3.6 | V | |
| DC Input Logic High | $V_{IH(DC)}$ | $V_{REF} + 0.1$ | — | V_{DD} | V | |
| DC Input Logic Low | $V_{IL(DC)}$ | vss | — | $V_{REF} - 0.1$ | V | |
| AC Input Logic High | $V_{IH(AC)}$ | $V_{REF} + 0.175$ | — | | V | |
| AC Input Logic Low | $V_{IL(AC)}$ | | — | $V_{REF} - 0.175$ | V | |
| In / Output Leakage Current | I_L | - 5 | — | 5 | μA | 3) |

- 1) Under all conditions, V_{DDQ} must be less than or equal to V_{DD}
- 2) Peak to peak AC noise on V_{REF} may not exceed $\pm 2\% V_{REF}$ (DC). V_{REF} is also expected to track noise in V_{DDQ} .
- 3) Input voltage for any connector pin under test of $0 V \leq V_{IN} \leq V_{DDQ} + 0.3 V$; all other pins at 0 V. Current is per pin

4.3 Module and Component Speed Grades

DDR3 components may exceed the listed module speed grades; module may not be available in all listed speed grades

Table 11 - Module and Component Speed Grades

| Module Speed Grade | Component Speed Grade |
|---------------------------|------------------------------|
| -16K | 1600-11-11-11 |

4.4 AC Timing Requirements

This chapter describes the AC timing requirements.

Table 12 - AC Timing Requirements

| Symbol | AC Characteristics Parameter | Min | Max | Unit |
|---------------------|--|-----------------------------|----------------------------|----------|
| tCK(DLL_OFF) | Minimum Clock Cycle Time (DLL off mode) | 8 | - | ns |
| tCH(avg) | Average high pulse width | 0.47 | 0.53 | tCK(avg) |
| tCL(avg) | Average low pulse width | 0.47 | 0.53 | tCK(avg) |
| tDQSQ | DQS, DQS# to DQ skew, per group, per access | - | 100 | ps |
| tQH | DQ output hold time from DQS, DQS# | 0.38 | - | tCK(avg) |
| tDS(base) | Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels | 10 | - | ps |
| tDH(base) | Data hold time from DQS, DQS# referenced to Vih(dc) / Vil(dc) levels | 45 | - | ps |
| tDIPW | DQ and DM Input pulse width for each input | 360 | - | ps |
| tRPRE | DQS, DQS# differential READ Preamble | 0.9 | - | tCK(avg) |
| tRPST | DQS, DQS# differential READ Postamble | 0.3 | - | tCK(avg) |
| tQSH | DQS, DQS# differential output high time | 0.40 | - | tCK(avg) |
| tQSL | DQS, DQS# differential output low time | 0.40 | - | tCK(avg) |
| tWPRE | DQS, DQS# differential WRITE Preamble | 0.9 | - | tCK(avg) |
| tWPST | DQS, DQS# differential WRITE Postamble | 0.3 | - | tCK(avg) |
| tDQCK | DQS, DQS# rising edge output access time from rising CK, CK# | -225 | 225 | ps |
| tLZ | DQ, DQS and DQS# low-impedance time | -450 | 225 | ps |
| tHZ | DQ, DQS and DQS# high-impedance time | - | 225 | ps |
| tDQSL | DQS, DQS# differential input low pulse width | 0.45 | 0.55 | tCK(avg) |
| tDQSH | DQS, DQS# differential input high pulse width | 0.45 | 0.55 | tCK(avg) |
| tDQSS | DQS, DQS# rising edge to CK, CK# rising edge | -0.27 | 0.27 | tCK(avg) |
| tDSS | DQS, DQS# falling edge setup time to CK, CK# rising edge | 0.18 | - | tCK(avg) |
| tDSH | DQS, DQS# falling edge hold time from CK, CK# rising edge | 0.18 | - | tCK(avg) |
| tRTP | Internal READ Command to PRECHARGE Command delay | max(4nCK, 7.5ns) | - | - |
| tWTR | Delay from start of internal write transaction to internal read command | max(4nCK, 7.5ns) | - | - |
| tWR | WRITE recovery time | 15 | - | ns |
| tMRD | Mode Register Set command cycle time | 4 | - | nCK |
| tIS(base) | Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels | 45 | - | ps |
| tIH(base) | Command and Address hold time from CK, CK# referenced to Vih(dc) / Vil(dc) levels | 120 | - | ps |
| tXP | Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL | max(3nCK, 6ns) | - | - |
| tCKE | CKE minimum pulse width | max(3nCK, 5.625ns) | - | - |
| tREFI | Average Periodic Refresh interval | 85°C < TCASE < 95°C /3.9 | 0°C < TCASE < 85°C /7.8 | us |

4.5 I_{DD} Specifications and Conditions

List of tables defining I_{DD} Specifications and Conditions.

Table 13 - I_{DD} Measurement Conditions

| Parameter | Symbol | Note ¹⁾²⁾³⁾⁴⁾⁵⁾ |
|--|--------------------|----------------------------|
| Operating Current 0 One bank Active - Precharge; $t_{CK} = t_{CK.MIN}$, $t_{RC} = t_{RC.MIN}$, $t_{RAS} = t_{RAS.MIN}$; CKE is HIGH, \overline{CS} is HIGH between valid commands. Address and control inputs are SWITCHING, Databus inputs are SWITCHING. | I _{DD0} | |
| Operating Current 1 One bank Active - Read - Precharge; $I_{OUT} = 0$ mA, BL = 4, $t_{CK} = t_{CK.MIN}$, $t_{RC} = t_{RC.MIN}$, $t_{RAS} = t_{RAS.MIN}$, $t_{RCD} = t_{RCD.MIN}$; AL = 0, CL = CL _{MIN} ; CKE is HIGH, CS is HIGH between valid commands. Address and control inputs are SWITCHING, Databus inputs are SWITCHING. | I _{DD1} | 6) |
| Precharge Standby Current All banks idle; \overline{CS} is HIGH; CKE is HIGH; $t_{CK} = t_{CK.MIN}$; Other control and address inputs are SWITCHING, Databus inputs are SWITCHING. | I _{DD2N} | |
| Precharge Standby ODT Current All banks idle; CS is HIGH; CKE is HIGH; $t_{CK} = t_{CK.MIN}$; Other control and address inputs are SWITCHING, Databus inputs are SWITCHING. | I _{DD2NT} | |
| Precharge Power-Down Current: Slow Exit Other control and address inputs are STABLE, Data bus inputs are FLOATING. | I _{DD2P0} | |
| Precharge Power-Down Current: Fast Exit Other control and address inputs are STABLE, Data bus inputs are FLOATING. | I _{DD2P1} | |
| Precharge Quiet Standby Current All banks idle; CS is HIGH; CKE is HIGH; $t_{CK} = t_{CK.MIN}$; Other control and address inputs are STABLE, Data bus inputs are FLOATING. | I _{DD2Q} | |
| Active Standby Current Burst Read: All banks open; Continuous burst reads; BL = 4; AL = 0, CL = CL _{MIN} ; $t_{CK} = t_{CK.MIN}$; $t_{RAS} = t_{RAS.MAX}$, $t_{RP} = t_{RP.MIN}$; CKE is HIGH, CS is HIGH between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING; $I_{OUT} = 0$ mA. | I _{DD3N} | |
| Active Power-Down Current All banks open; $t_{CK} = t_{CK.MIN}$; CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are FLOATING. | I _{DD3P} | |
| Operating Current - Burst Read All banks open; Continuous burst reads; BL = 4; AL = 0, CL = CL _{MIN} ; $t_{CK} = t_{CK.MIN}$; $t_{RAS} = t_{RAS.MAX}$; $t_{RP} = t_{RP.MIN}$; CKE is HIGH, CS is HIGH between valid commands; Address inputs are SWITCHING; Data bus inputs are SWITCHING; $I_{OUT} = 0$ mA. | I _{DD4R} | 6) |
| Operating Current - Burst Write All banks open; Continuous burst writes; BL = 4; AL = 0, CL = CL _{MIN} ; $t_{CK} = t_{CK.MIN}$; $t_{RAS} = t_{RAS.MAX}$, $t_{RP} = t_{RP.MAX}$; CKE is HIGH, CS is HIGH between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING; | I _{DD4W} | |
| Burst Refresh Current $t_{CK} = t_{CK.MIN}$; Refresh command every $t_{RFC} = t_{RFC.MIN}$ interval, CKE is HIGH, CS is HIGH between valid commands, Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING. | I _{DD5B} | |

| Parameter | Symbol | Note ¹⁾²⁾³⁾⁴⁾⁵⁾ |
|---|-----------|----------------------------|
| Self-Refresh Current CKE ≤ 0.2 V; external clock off, CK and CK at 0 V; Other control and address inputs are FLOATING, Data bus inputs are FLOATING. I_{DD6} current values are guaranteed up to T_{CASE} of 85 °C max. | I_{DD6} | |
| All Bank Interleave Read Current All banks are being interleaved at minimum t_{RC} without violating t_{RRD} using a burst length of 4. Control and address bus inputs are STABLE during DESELECTS. $I_{out} = 0$ mA. | I_{DD7} | 6) |
| Reset Current | I_{DD8} | |

- 1) $V_{DDQ} = 1.5 V \pm 0.1 V$; $V_{DD} = 1.5 V \pm 0.1 V$
- 2) I_{DD} specifications are tested after the device is properly initialized and I_{DD} parameter is specified with ODT disabled.
- 3) Definitions for I_{DD} see [Table 14](#)
- 4) For two rank modules: All active current measurements in the same I_{DD} current mode. The other rank is in I_{DD2P} Precharge Power-Down Mode.
- 5) For details and notes see the relevant UnilC component data sheet.
- 6) I_{DD1} , I_{DD4R} and I_{DD7} current measurements are defined with the outputs disabled ($I_{OUT} = 0$ mA). To achieve this on module level the output buffers can be disabled using an EMRS(1) (Extended Mode Register Command) by setting A12 bit to HIGH.

Table 14 - Definitions for I_{DD}

| Parameter | Description |
|-----------|---|
| LOW | $V_{IN} \leq V_{IL(ac).MAX}$, HIGH is defined as $V_{IN} \geq V_{IH(ac).MIN}$ |
| STABLE | Inputs are stable at a HIGH or LOW level. |
| FLOATING | Inputs are $V_{REF} = V_{DDQ} / 2$ |
| SWITCHING | Inputs are changing between HIGH and LOW every other clock (once per 2 cycles) for address and control signals, and inputs changing between HIGH and LOW every other data transfer (once per cycle) for DQ signals not including mask or strobes. |

Table 15 - I_{DD} Specification for HXMSH16P13A2F2CL16K

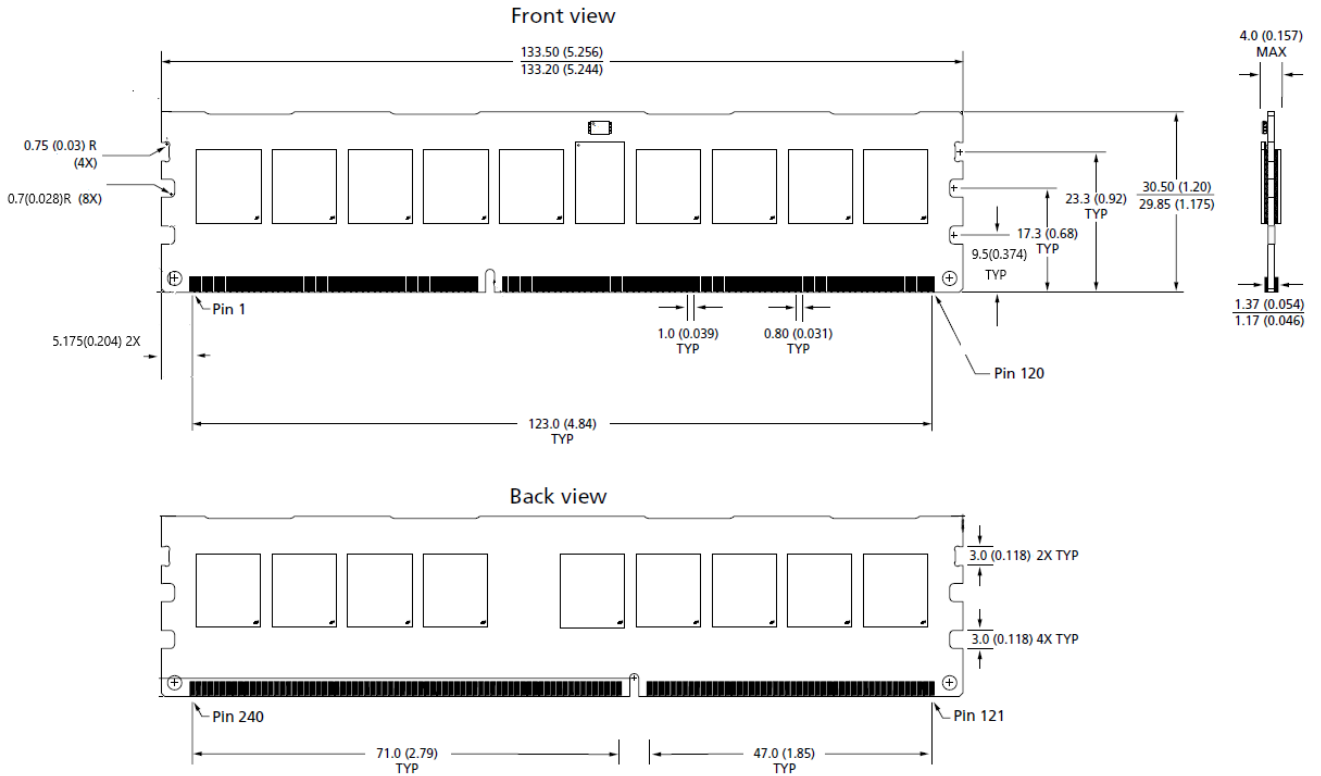
| Product Type | HXMSH16P13A2F2CL16K | | |
|--------------|---------------------|------|----------------------|
| Organization | 16 GB | Unit | Note ¹⁾²⁾ |
| | 2 Rank (×8) | | |
| | ×72 | | |
| | -16K | | |
| Symbol | Current | | |
| I_{DD0} | 810 | mA | 2) |
| I_{DD1} | 1017 | mA | 2) |
| I_{DD2N} | 864 | mA | 3) |
| I_{DD2P0} | 234 | mA | 3) |
| I_{DD2Q} | 846 | mA | 3) |
| I_{DD3N} | 1152 | mA | 3) |
| I_{DD3P} | 756 | mA | 3) |
| I_{DD4R} | 1620 | mA | 2) |
| I_{DD4W} | 1692 | mA | 2) |
| I_{DD5B} | 2457 | mA | 2) |
| I_{DD6} | 396 | mA | 3) |
| I_{DD7} | 2502 | mA | 2) |

Notes:

- 1) Calculated values from Device data.
- 2) One module rank in the active I_{DD} , the other rank in I_{DD2P}
- 3) All ranks in this I_{DD} condition

5 Package Dimensions

Figure 1 - Package Dimensions_HXMSH16P13A2F2CL16K



- Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
 2. The dimensional diagram is for reference only.

List of Figures

| | |
|--|----|
| Figure 1 - Package Dimensions_HXMSH16P13A2F2CL16K..... | 22 |
|--|----|

List of Tables

| | |
|---|----|
| Table 1 - Module Performance Table..... | 4 |
| Table 2 - Ordering Information..... | 5 |
| Table 3 - Address Format | 5 |
| Table 4 - Pin Configuration of DDR3 RDIMM | 6 |
| Table 5 - Abbreviations for pin Type | 12 |
| Table 6 - Abbreviations for Buffer Type..... | 12 |
| Table 7 - Pin Configuration RDIMM (240 pin)..... | 13 |
| Table 8 - Absolute Maximum Ratings | 15 |
| Table 9 - DRAM Component Operating Temperature Range | 15 |
| Table 10 - Supply Voltage Levels and AC / DC Operating Conditions | 16 |
| Table 11 - Module and Component Speed Grades..... | 17 |
| Table 12 - AC Timing Requirements | 18 |
| Table 13 - I _{DD} Measurement Conditions | 19 |
| Table 14 - Definitions for I _{DD} | 20 |
| Table 15 - I _{DD} Specification for HXMSH16P13A2F2CL16K | 21 |

Edition 2021-01
Published by
Xi'an UnilC Semiconductors Co., Ltd.

Xi'an: 4th Floor, Building A,
No. 38 Gaoxin 6th Road,
Xian High-tech Industries Development Zone
Xi'an, Shanxi 710075, P. R. China
Tel: +86-29-88318000
Fax: +86-29-88453299

info@unisemicon.com

© UnilC 2021.
All Rights Reserved.

Legal Disclaimer

THE INFORMATION GIVEN IN THIS INTERNET DATA SHEET SHALL IN NO EVENT BE REGARDED AS A GUARANTEE OF CONDITIONS OR CHARACTERISTICS. WITH RESPECT TO ANY EXAMPLES OR HINTS GIVEN HEREIN, ANY TYPICAL VALUES STATED HEREIN AND/OR ANY INFORMATION REGARDING THE APPLICATION OF THE DEVICE, UNILC HEREBY DISCLAIMS ANY AND ALL WARRANTIES AND LIABILITIES OF ANY KIND, INCLUDING WITHOUT LIMITATION WARRANTIES OF NON-INFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS OF ANY THIRD PARTY.

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest UnilC Office.

Warnings

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest UnilC Office.

UnilC Components may only be used in life-support devices or systems with the express written approval of UnilC, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

www.unisemicon.com