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SCB33S256320AF
SCB33S256160AF
SCB33S256800AF

256Mbit synchronous DRAM

EU RoHS Compliant Products

Data Sheet

Rev. D

Revision History		
Date	**version**	**Subjects(major changes since last revision)**
2016/07	A	Initial Release
2016/09	B	Add the “I”, “A2” grade component
2016/11	C	Update the “I” grade temperature and IDD specification
2017/03	D	1. Redefine the operating temperature 2. Add the X grade product

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1 Overview

This chapter gives an overview of the 256-Mbit Synchronous DRAM component product and describes its main characteristics.

1.1 Features

- Fully Synchronous to Positive Clock Edge
- Operating Temperature
  - – Commercial temperature range 0 °C to 70 °C
  - – Industrial temperature range -40 °C to 85 °C
  - – Automotive grade 2 temperature range -40°C to 105°C
  - –High-Rel, X (-55 ℃ to 125 ℃)
- Four Banks controlled by BA0 & BA1
- Programmable CAS Latency: 1 & 2 & 3
- Programmable Wrap Sequence: Sequential or Interleave
- Programmable Burst Length: 1, 2, 4, 8 and full page
- Multiple Burst Read with Single Write Operation
- Automatic and Controlled Precharge Command
- Data Mask for Read / Write control (x8, x16, x32)
- Data Mask for Byte Control (x16,x32)
- Auto Refresh (CBR) and Self Refresh
- Power Down Mode
- 8192 refresh cycles / 64 ms (7.8 µs) T≦105°C
  / 32 ms (3.9us) T>105°C
- Random Column Address every CLK (1-N Rule)
- Single 3.3 V ± 0.3 V Power Supply
- LVTTL Interface versions
- Chipsize Packages: P-FBGA54L 8*13*1.2mm (x8, x16) P-FBGA90L 8*13*1.2mm (x32)

Note: Self Refresh Mode available on temperature less than 105°C (Tcase) only.

TABLE 1
Performance

Part Number Speed Code			–6E	–6	-75	Unit
System Frequency (fCK)			167	167	133	MHz
Max. Clock Frequency	@CL3	t_{CK3}	6	6	7.5	ns
		t_{AC3}	5.4	5.4	5.4	ns
	@CL2	t_{CK2}	7.5	10	10	ns
		t_{AC2}	5.4	6	6	ns
	@CL1	t_{CK1}	20	20	20	ns
		t_{AC1}	17	17	17	ns

1.2 Description

The SCB33S256[320/160/800]AF-[6B/6EB/75B] are four bank Synchronous DRAMs organized as 4 banks x 2 MBit x32, 4 banks x 4 Mbit x16 and 4 banks x 8 MBit x8 respectively. These synchronous devices achieve high speed data transfer rates for CAS latencies by employing a chip architecture that prefetches multiple bits and then synchronizes the output data to a system clock.
The device is designed to comply with all industry standards set for synchronous DRAM products, both electrically and mechanically. All of the control, address, data input and output circuits are synchronized with the positive edge of an externally supplied clock.
Operating the four memory banks in an interleave fashion allows random access operation to occur at a higher rate than is possible with standard DRAMs. A sequential and gapless data rate is possible depending on burst length, CAS latency and speed grade of the device.
`Auto Refresh (CBR) and Self Refresh operation are supported. These devices operate with a single 3.3 V ± 0.3 V power supply. All 256-Mbit components are available in P–TFBGA–[90/54] packages.

TABLE 2
Ordering Information for RoHS Compliant Products

	Product Type[1)]	Package	Description
X8 P-FBGA54	SCB33S256800AF-6B	P-FBGA54	167MHz 32M x 8 SDRAM
	SCB33S256800AF-6BI	P-FBGA54	167MHz 32M x 8 SDRAM
	SCB33S256800AF-6BA2	P-FBGA54	167MHz 32M x 8 SDRAM
	SCB33S256800AF-6EBX	P-FBGA54	167MHz 32M x 8 SDRAM
	SCB33S256800AF-6EB	P-FBGA54	167MHz 32M x 8 SDRAM
	SCB33S256800AF-6EBI	P-FBGA54	167MHz 32M x 8 SDRAM
	SCB33S256800AF-6EBA2	P-FBGA54	167MHz 32M x 8 SDRAM
	SCB33S256800AF-6EBX	P-FBGA54	167MHz 32M x 8 SDRAM
	SCB33S256800AF-75B	P-FBGA54	133MHz 32M x 8 SDRAM
	SCB33S256800AF-75BI	P-FBGA54	133MHz 32M x 8 SDRAM
	SCB33S256800AF-75BA2	P-FBGA54	133MHz 32M x 8 SDRAM
	SCB33S256800AF-75BX	P-FBGA54	133MHz 32M x 8 SDRAM
X16 P-FBGA54	SCB33S256160AF-6B	P-FBGA54	167MHz 16M x 16 SDRAM
	SCB33S256160AF-6BI	P-FBGA54	167MHz 16M x 16 SDRAM
	SCB33S256160AF-6BA2	P-FBGA54	167MHz 16M x 16 SDRAM
	SCB33S256160AF-6BX	P-FBGA54	167MHz 16M x 16 SDRAM
	SCB33S256160AF-6EB	P-FBGA54	167MHz 16M x 16 SDRAM

	SCB33S256160AF-6EBI	P-FBGA54	167MHz 16M x 16 SDRAM
	SCB33S256160AF-6EBA2	P-FBGA54	167MHz 16M x 16 SDRAM
	SCB33S256160AF-6EBX	P-FBGA54	167MHz 16M x 16 SDRAM
	SCB33S256160AF-75B	P-FBGA54	133MHz 16M x 16 SDRAM
	SCB33S256160AF-75BI	P-FBGA54	133MHz 16M x 16 SDRAM
	SCB33S256160AF-75BA2	P-FBGA54	133MHz 16M x 16 SDRAM
	SCB33S256160AF-75BX	P-FBGA54	133MHz 16M x 16 SDRAM
X32 P-FBGA90	SCB33S256320AF-6B	P-FBGA90	167MHz 8M x 32 SDRAM
	SCB33S256320AF-6BI	P-FBGA90	167MHz 8M x 32 SDRAM
	SCB33S256320AF-6BA2	P-FBGA90	167MHz 8M x 32 SDRAM
	SCB33S256320AF-6BX	P-FBGA90	167MHz 8M x 32 SDRAM
	SCB33S256320AF-6EB	P-FBGA90	167MHz 8M x 32 SDRAM
	SCB33S256320AF-6EBI	P-FBGA90	167MHz 8M x 32 SDRAM
	SCB33S256320AF-6EBA2	P-FBGA90	167MHz 8M x 32 SDRAM
	SCB33S256320AF-6EBX	P-FBGA90	167MHz 8M x 32 SDRAM
	SCB33S256320AF-75B	P-FBGA90	133MHz 8M x 32 SDRAM
	SCB33S256320AF-75BI	P-FBGA90	133MHz 8M x 32 SDRAM
	SCB33S256320AF-75BA2	P-FBGA90	133MHz 8M x 32 SDRAM
	SCB33S256320AF-75BX	P-FBGA90	133MHz 8M x 32 SDRAM

1) RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers.

2 Configuration

This chapter contains the pin configuration table, the FBGA package drawing,

2.1 Pin Description

Listed below are the pin configurations sections for the various signals of the SDRAM

TABLE 3
Configuration FBGA-54/90

Name	Pin Type	Buffer Type	Function
Clock Signals			
CLK	I	LVTTL	**Clock Signal CK**
CKE	I	LVTTL	**Clock Enable** *Note: Activates the CLK signal when high and deactivates the CLK signal when low, thereby initiating either the Power Down mode, Suspend mode, or the Self Refresh mode.*
Control Signals			
$\overline{RAS}$	I	LVTTL	**Row Address Strobe**
$\overline{CAS}$	I	LVTTL	**Column Address Strobe**
$\overline{WE}$	I	LVTTL	**Write Enable**
$\overline{CS}$	I	LVTTL	**Chip Select**
Address Signals			
BA0~BA1	I	LVTTL	**Bank Address Signals 1:0** *Note: Bank Select Inputs. Bank address inputs selects which of the four banks a command applies to.*
A0~A12	I	LVTTL	**Address Signal 9:0, Address Signal 10/Auto precharge** *Note: During a Bank Activate command cycle, A0-A11/A12 define the row address (RA0-RA11/RA12) when sampled at the rising clock edge. During a Read or Write command cycle, A0-An define the column address (CA0-CAn) when sampled at the rising clock edge. CAn depends upon the SDRAM organization:* *32M x8SDRAM CAn = CA9 (Page Length = 1024 bits)* *16M x16SDRAM CAn = CA8 (Page Length = 512 bits)* *8M x32SDRAM CAn = CA8 (Page Length = 512 bits)* *In addition to the column address, A10 (= AP) is used to invoke the auto pre charge operation at the end of the burst read or write cycle. If A10 is high, auto pre charge is selected and BA0, BA1 defines the bank to be precharged. If A10 is low, auto pre charge is disabled. During a Precharge command cycle, A10 (= AP) is used in conjunction with BA0 and BA1 to control which bank(s) to precharge. If A10 is high, all four banks will be precharged regardless of the state of BA0 and BA1. If A10 is low, then BA0 and BA1 are used to define which bank to precharge.* *X32 row address : RA0-RA11* *X16 row address : RA0-RA12* *X8 row address : RA0-RA12*

Name	Pin Type	Buffer Type	Function
Data Signals			
DQ0~DQ31	I/O	LVTTL	**Data Signal 31:0**
DQM(x8)/ LDQM(x16)/ DQM0(x32)	I	LVTTL	**Data Mask for DQ0~DQ7**
UDQM(x16)/ DQM1(x32)	I	LVTTL	**Data Mask for DQ8~DQ15**
DQM2(x32)	I	LVTTL	**Data Mask for DQ16~DQ23**
DQM3(x32)	I	LVTTL	**Data Mask for DQ24~DQ31**
Power Supplies			
V_{DDQ}	PWR	–	**Power Supply for DQs**
V_{DD}	PWR	–	**Power Supply**
V_{SSQ}	PWR	–	**Power Supply Ground for DQs**
V_{SS}	PWR	–	**Power Supply Ground**
Not Connected			
NC	NC	—	**Not Connected**

TABLE 4
Abbreviations for Ball Type

Abbreviation	Description
I	Standard input-only pin. Digital levels
O	Output. Digital levels
I/O	I/O is a bidirectional input/output signal
AI	Input. Analog levels
PWR	Power
GND	Ground
NC	Not Connected

TABLE 5
Abbreviations for Buffer Type

Abbreviation	Description
LVTTL	Low Voltage Transistor-Transistor Logic (LVTTL-3.3)
LV-CMOS	Low Voltage CMOS
CMOS	CMOS Levels
OD	Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR

FIGURE 1

Configuration for x32 Organization, TFBGA-90, Top View

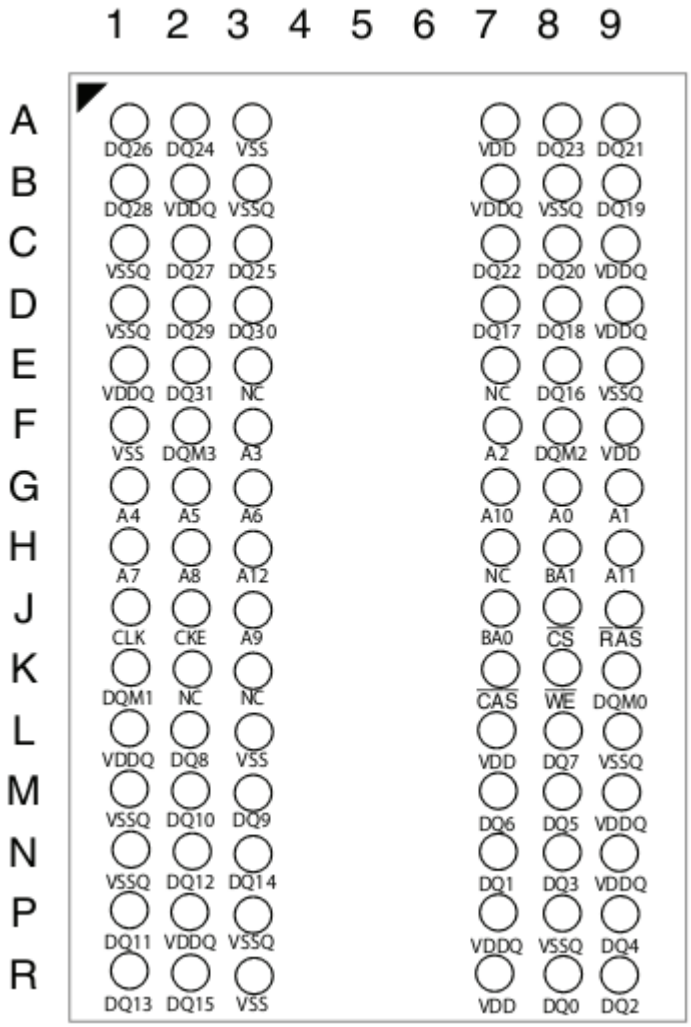


FIGURE 2
Configuration for x16 Organization, TFBGA-54, Top View

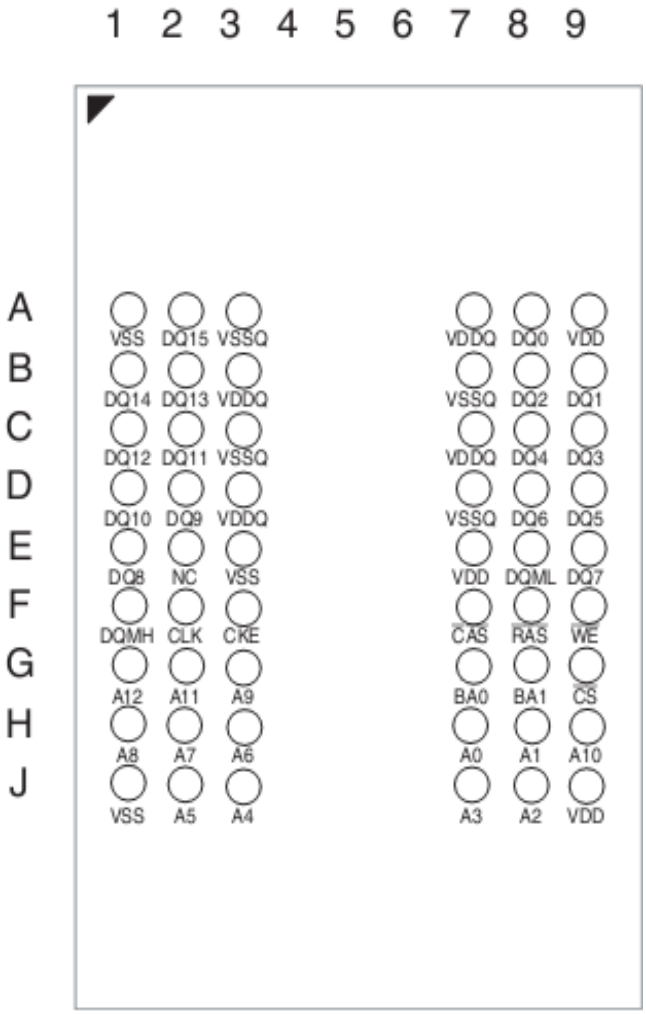
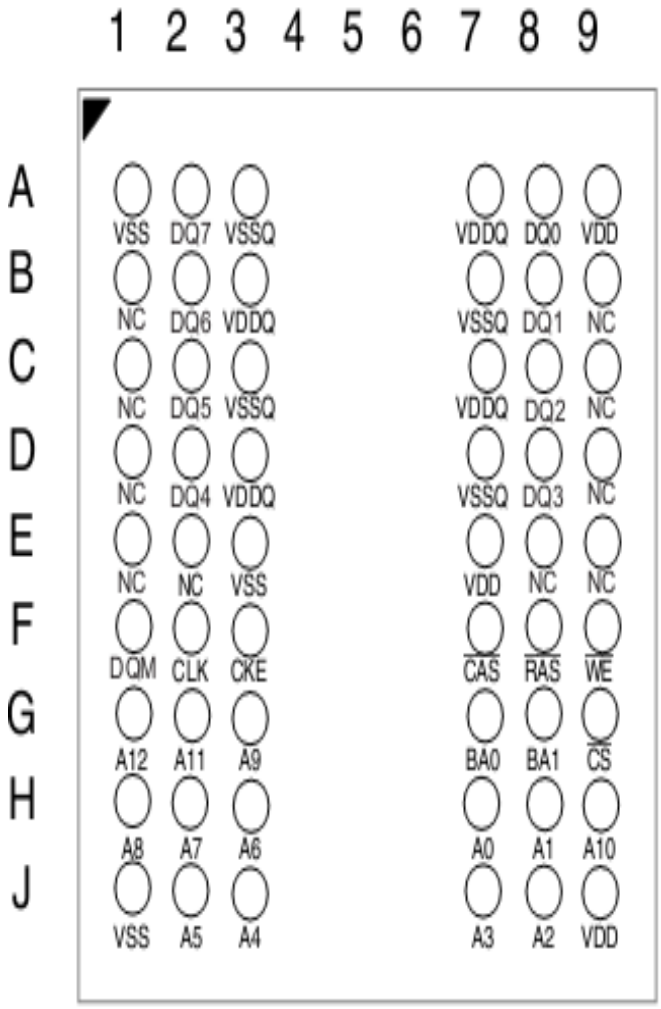


FIGURE 3
Configuration for x8 Organization, TFBGA-54, Top View



3 Functional Description

3.1 Operation Definition

All of SDRAM operations are defined by states of control signals $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, and DQM at the positive edge of the clock. The following list shows the truth table for the operation commands.

TABLE 6
Truth table

Operation	Device State	CKE n-1 1)2)	CKE n 1)2)	DQM 1)2)	BA0 BA1 1)2)	AP= A10 1)2)	Addr. 1)2)	$\overline{CS}$ 1)2)	$\overline{RAS}$ 1)2)	$\overline{CAS}$ 1)2)	$\overline{WE}$ 1)2)
Bank Active	Idle 3)	H	X	X	V	V	V	L	L	H	H
Bank Precharge	Any	H	X	X	V	L	X	L	L	H	L
Precharge All	Any	H	X	X	X	H	X	L	L	H	L
Write	Active 3)	H	X	X	V	L	V	L	H	L	L
Write with Auto pre charge	Active 3)	H	X	X	V	H	V	L	H	L	L
Read	Active 3)	H	X	X	V	L	V	L	H	L	H
Read with Auto pre charge	Active 3)	H	X	X	V	H	V	L	H	L	H
Mode Register Set	Idle	H	X	X	V	V	V	L	L	L	L
No Operation	Any	H	X	X	X	X	X	L	H	H	H
Burst Stop	Active	H	X	X	X	X	X	L	H	H	L
Device Deselect	Any	H	X	X	X	X	X	H	X	X	X
Auto Refresh	Idle	H	H	X	X	X	X	L	L	L	H
Self Refresh Entry	Idle	H	L	X	X	X	X	L	L	L	H
Self Refresh Exit	Idle (Self Refr.)	L	H	X	X	X	X	H	X	X	X
								L	H	H	X
Clock Suspend Entry	Active	H	L	X	X	X	X	X	X	X	X
Power Down Entry (Precharge or active standby)	Idle	H	L	X	X	X	X	H	X	X	X
	Active							L	H	H	H
Clock Suspend Exit	Active 4)	L	H	X	X	X	X	X	X	X	X
Power Down Exit	Any (Power Down)	L	H	X	X	X	X	H	X	X	X
								L	H	H	L
Data Write/Output Enable	Active	H	X	L	X	X	X	X	X	X	X
Data Write/Output Disable	Active	H	X	H	X	X	X	X	X	X	X

1) V = Valid, x = Don't Care, L = Low Level, H = High Level
2) CKEn signal is input level when commands are provided, CKEn-1 signal is input level one clock before the commands are Provided
3) This is the state of the banks designated by BA0, BA1 signals.
4) Power Down Mode can not be entered in a burst cycle. When this command asserted in the burst mode cycle device is in clock suspend mode.

3.2 Initialization

The default power on state of the mode register is supplier specific and may be undefined. The following power on and initialization sequence guarantees the device is preconditioned to each users specific needs. Like a conventional DRAM, the Synchronous DRAM must be powered up and initialized in a predefined manner. During power on, all VDD and VDDQ pins must be built up simultaneously to the specified voltage when the input signals are held in the “NOP” state. The power on voltage must not exceed VDD + 0.3 V on any of the input pins or VDD supplies. The CLK signal must be started at the same time. After power on, an initial pause of 200 µs is required followed by a precharge of all banks using the precharge command. To prevent data contention on the DQ bus during power on, it is required that the DQM and CKE pins be held high during the initial pause period. Once all banks have been precharged, the Mode Register Set Command must be issued to initialize the Mode Register. A minimum of eight Auto Refresh cycles (CBR) are also required. These may be done before or after programming the Mode Register. Failure to follow these steps may lead to unpredictable start-up modes.

3.3 Mode Register Definition

The Mode register designates the operation mode at the read or write cycle. This register is divided into four fields. First, a Burst Length field which sets the length of the burst. Second, an Addressing Selection bit which programs the column access sequence in a burst cycle (interleaved or sequential). Third, a CAS Latency field to set the access time at clock cycle. Fourth, an Operation mode field to differentiate between normal operation (Burst read and burst Write) and special Burst Read and Single Write mode. After the initial power up, the mode set operation must be done before any activate command. Any content of the mode register can be altered by re-executing the mode set command. All banks must be in precharged state and CKE must be high at least one clock before the mode set operation. After the mode register is set, a Standby or NOP command is required. Low signals of RAS, CAS, and WE at the positive edge of the clock activate the mode set operation. Address input data at this timing defines parameters to be set as shown in the previous table.

BA0	BA1	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	reserved		weak OCD	wrbst	reserved		CL			BT	BL		

TABLE 7
Mode Register Definition

Field	Bits	Type[1)]	Description
BL	[2:0]	W	**Burst Length** 000_B1, 001_B 2, 010_B 4, 011_B 8, 111_B Full Page (Sequential burst type only),
BT	[3]		**Burst Type** 0 Sequential 1 Interleaved
CL	[6:4]		**CAS Latency** *Note: All other bit combinations are RESERVED.* 010_B **2** 011_B **3**
MODE	[8:7]		**RESERVED**
wrbst	[9]		**Write Burst Mode** 0_BProgrammed Burst Length, 1_BSingle Location Access,
Weak OCD	[10]		**Weak OCD Mode** 0_Bnormal OCD, 1_Bweak OCD,
MODE	[12:11]		**RESERVED**

1) W = write only register bit

3.4 Burst Type

Accesses within a given burst may be programmed to be sequential or interleaved; as shown in **Table 8**.

TABLE 8
Burst Definition

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
	A2	A1	A0	Type = Sequential	Type = Interleaved
2			0	0-1	0-1
			1	1-0	1-0
4		0	0	0-1-2-3	0-1-2-3
		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
8	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
Full page	n			Cn, Cn+1, Cn+2	not supported

Notes

1. For a burst length of two, A1-Ai selects the two-data-element block; A0 selects the first access within the block.
2. For a burst length of four, A2-Ai selects the four-data-element block; A0-A1 selects the first access within the block.
3. For a burst length of eight, A3-Ai selects the eight-data- element block; A0-A2 selects the first access within the block.
4. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.

3.5 Commands

Refresh Mode

SDRAM has two refresh modes, Auto Refresh and Self Refresh. Auto Refresh is similar to the CAS -before-RAS refresh of conventional DRAMs. All banks must be precharged before applying any refresh mode. An on-chip address counter increments the word and the bank addresses and no bank information is required for both refresh modes.

The chip enters the Auto Refresh mode, when $\overline{RAS}$ and $\overline{CAS}$ are held low and CKE and $\overline{WE}$ are held high at a clock timing. The mode restores word line after the refresh and no external precharge command is necessary. A minimum tRC time is required between two automatic refreshes in a burst refresh mode. The same rule applies to any access command after the automatic refresh operation.

The chip has an on-chip timer and the Self Refresh mode is available. The mode restores the word lines after, $\overline{RAS}$ $\overline{CAS}$ and CKE are low and $\overline{WE}$ is high at a clock timing. All of external control signals including the clock are disabled. Returning CKE to high enables the clock and initiates the refresh exit operation. After the exit command, at least one tRC delay is required prior to any access command.

Auto Precharge

Two methods are available to precharge SDRAMs. In an automatic precharge mode, the CAS timing accepts one extra address, CA10, to determine whether the chip restores or not after the operation. If CA10 is high when a Read Command is issued, the Read with Auto-Precharge function is initiated. If CA10 is high when a Write Command is issued, the Write with Auto-Precharge function is initiated. The SDRAM automatically enters the precharge operation a time delay equal to tWR (“write recovery time”) after the last data in. A burst operation with Auto-Precharge may only be interrupted by a burst start to another bank. It must not be interrupted by a precharge or a burst stop command.

Precharge Command

There is also a separate precharge command available. When $\overline{RAS}$ and $\overline{WE}$ are low and $\overline{CAS}$ is high at a clock timing, it triggers the precharge operation. Three address bits, BA0, BA1 and A10 are used to define banks as shown in the following list. The precharge command can be imposed one clock before the last data out for CAS latency = 2 and two clocks before the last data out for CAS latency = 3. Writes require a time delay tWR (“write recovery time”) of 2 clocks minimum from the last data out to apply the precharge command.

TABLE 9
Bank Selection by Address Bits

A10	BA0	BA1	
0	0	0	Bank 0
0	0	1	Bank 1
0	1	0	Bank 2
0	1	1	Bank 3
1	X	X	All Banks

Burst Termination

Once a burst read or write operation has been initiated, there are several methods in which to terminate the burst operation prematurely. These methods include using another Read or Write Command to interrupt an existing burst operation, use a Precharge Command to interrupt a burst cycle and close the active bank, or using the Burst Stop Command to terminate the existing burst operation but leave the bank open for future Read or Write Commands to the same page of the active bank. When interrupting a burst with another Read or Write Command care must be taken to avoid DQ contention. The Burst Stop Command, however, has the fewest restrictions making it the easiest method to use when terminating a burst operation before it has been completed. If a Burst Stop command is issued during a burst write operation, then any residual data from the burst write cycle will be ignored. Data that is presented on the DQ pins before the Burst Stop Command is registered will be written to the memory.

3.6 Operations

Read and Write

When $\overline{RAS}$ is low and both $\overline{CAS}$ and $\overline{WE}$ are high at the positive edge of the clock, a $\overline{RAS}$ cycle starts. According to address data, a word line of the selected bank is activated and all of sense amplifiers associated to the wordline are set. A $\overline{CAS}$ cycle is triggered by $\overline{RAS}$ setting high and $\overline{CAS}$ low at a clock timing after a necessary delay, tRCD from the $\overline{RAS}$ timing. $\overline{WE}$ is used to define either a read(WE=H) or a write(WE=L) at this stage.

SDRAM provides a wide variety of fast access modes. In a single $\overline{CAS}$ cycle, serial data read or write operations are allowed at up to a 166 MHz data rate. The numbers of serial data bits are the burst length programmed at the mode set operation, i.e., one of 1, 2, 4 and 8 and full page. Column addresses are segmented by the burst length and serial data accesses are done within this boundary. The first column address to be accessed is supplied at the $\overline{CAS}$ timing and the subsequent addresses are generated automatically by the programmed burst length and its sequence. For example, in a burst length of 8 with interleave sequence, if the first address is '2', then the rest of the burst sequence is 3, 0, 1, 6, 7, 4, and 5.

Full page burst operation is only possible using the sequential burst type and page length is a function of the I/O organization and column addressing. Full page burst operation does not self terminate once the burst length has been reached. In other words, unlike burst lengths of 2, 4 and 8, full page burst continues until it is terminated using another command.

Similar to the page mode of conventional DRAMs, burst read or write accesses on any column address are possible once the $\overline{RAS}$ cycle latches the sense amplifiers. The maximum tRAS or the refresh interval time limits the number of random column accesses. A new burst access can be done even before the previous burst ends. The interrupt operation at every clock cycle is supported. When the previous burst is interrupted, the remaining addresses are overridden by the new address with the full burst length. An interrupt which accompanies an operation change from a read to a write is possible by exploiting DQM to avoid bus contention.

When two or more banks are activated sequentially, interleaved bank read or write operations are possible. With the programmed burst length, alternate access and precharge operations on two or more banks can realize fast serial data access modes among many different pages. Once two or more banks are activated, column to column interleave operation can be performed between different pages.

DQM Function

DQM has two functions for data I/O read and write operations. During reads, when it turns to "high" at a clock timing, data outputs are disabled and become high impedance after two clock delay (DQM Data Disable Latency tDQZ). It also provides a data mask function for writes. When DQM is activated, the write operation at the next clock is prohibited (DQM Write Mask Latency tDQW = zero clocks).

Power Down

In order to reduce standby power consumption, a power down mode is available. All banks must be precharged and the necessary Precharge delay (tRP) must occur before the SDRAM can enter the Power Down mode. Once the Power Down mode is initiated by holding CKE low, all of the receiver circuits except CLK and CKE are gated off. The Power Down mode does not perform any refresh operations, therefore the device can't remain in Power Down mode longer than the Refresh period (tREF) of the device. Exit from this mode is performed by taking CKE "high". One clock delay is required for Power Down mode entry and exit.

4 Electrical Characteristics

4.1 Operating Conditions

TABLE 10
Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Note/ Test Condition
		Min.	Max.		
Input / Output voltage relative to V_{SS}	V_{IN}, V_{OUT}	– 1.0	+4.6	V	–
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}	– 1.0	+4.6	V	–
Voltage on V_{DDQ} supply relative to V_{SS}	V_{DDQ}	– 1.0	+4.6	V	–
Storage temperature range	T_{STG}	-55	+150	℃	–
Power dissipation per SDRAM component	P_D	–	1	W	–
Data out current (short circuit)	I_{OUT}	–	50	mA	–

Attention: Stresses above the max. values listed here may cause permanent damage to the device.
Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

TABLE 11
Operating Temperature

Symbol	Parameter	Rating		Unit	Note/ Test Condition
		Min	Max		
Toper	Operating temperature	0	70	℃	Commercial temperature
		– 40	85	℃	Industrial temperature range
		– 40	105	℃	Automotive grade 2 temperature range
		– 55	125	℃	High-Rel temperature range

1) Operating Temperature is the operating ambient temperature surrounding the DRAM.
2) The operating temperature range are the temperatures where all DRAM specification will be supported.
3) When TCASE ⩾105℃ the Auto-Refresh command interval has to be reduced to t_{REFI}= 3.9 µs.

TABLE 12
DC Characteristics

Parameter	Symbol	Values		Unit	Note/ Test Condition
		Min.	Max.		
Supply Voltage	V_{DD}	3.0	3.6	V	2)
I/O Supply Voltage	V_{DDQ}	3.0	3.6	V	2)
Input high voltage	V_{IH}	2.0	V_{DDQ}+0.3	V	2)3)
Input low voltage	V_{IL}	– 0.3	+0.8	V	2)3)
Output high voltage (I_{OUT} = – 4.0 mA)	V_{OH}	2.4	–	V	2)
Output low voltage (I_{OUT} = 4.0 mA)	V_{OL}	–	0.4	V	2)
Input leakage current, any input (0 V < V_{IN} < V_{DD}, all other inputs = 0 V)	I_{IL}	– 10	+10	µA	–
Output leakage current (DQs are disabled, 0 V < V_{OUT} < V_{DDQ})	I_{OL}	– 10	+10	µA	–

1) All voltages are referenced to VSS
2) VIH may overshoot to VDDQ + 2.0 V for pulse width of < 4ns with 3.3 V. VIL may undershoot to -2.0 V for pulse width < 4.0 ns with 3.3 V. Pulse width measured at 50% points with amplitude measured peak to DC reference.

TABLE 13
Input and Output Capacitances

Parameter	Symbol	Values[2)]		Unit
		Min.	Max.	
Input Capacitances: CK, CK	C_{I1}	2.5	3.5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CKE, DQM)	C_{I2}	2.5	3.8	pF
Input/Output Capacitance (DQ)	C_{I0}	4.0	6.0	pF

1) VDD, VDDQ = 3.3 V ± 0.3 V, f = 1 MHz
2) Capacitance values are shown for TSOP-54 packages. Capacitance values for TFBGA packages are lower by 0.5 pF

TABLE 14
I_{DD} Conditions

Parameter	Symbol
Operating Current One bank active, Burst length = 1	I_{DD1}
Precharge Standby Current in Power Down Mode tCK = min.	I_{DD2P}
Recharge Standby Current in Non-Power Down Mode tCK = min.	I_{DD2N}
No Operating Current Active state (max. 4 banks)	I_{DD3N}
	I_{DD3P}
Burst Operating Current Read command cycling	I_{DD4}
Auto Refresh Current Auto Refresh command cycling	I_{DD5}
Self Refresh Current Self Refresh Mode, CKE=0.2V, t_{CK}=infinity	I_{DD6}

TABLE 15
X32/X16/X8 I_{DD} Specifications

Symbol	Parameter &Test Condition	Speed Gread	IDDmax			Unit	Notes
			X32	X16	X8		
I_{DD1}	tRC = tRCMIN., tRC = tCKMIN. 1 bank operation	–6/6E	90	90	90	mA	1,3
		-75	70	70	70		
I_{DD2P}	CS =VIH, CKE≤ VIL(max) tCK = min.	–6/6E	4	4	4	mA	1,3
		-75	4	4	4		
I_{DD2N}	CS =VIH, CKE≥ VIL(max) tCK = min.	–6/6E	15	15	15	mA	3
		-75	15	15	15		
I_{DD3P}	CS = $V_{IH(min)}$, CKE ≤ $V_{IL(max.)}$ tCK = min,	–6/6E	6	6	6	mA	3
		-75	6	6	6		
I_{DD3N}	CS = $V_{IH(min)}$, CKE ≥$V_{IH(min.)}$ tCK = min,	–6/6E	20	20	20	mA	3
		-75	20	20	20		
I_{DD4}	Burst Operating Current Read/Write command cycling tCK = min	–6/6E	120	110	100	mA	1,2,3
		-75	100	90	80		
I_{DD5}	t_{RC}= $t_{RC(min)}$ tCK = min	–6/6E	190	190	190	mA	1,3
		-75	190	190	190		
I_{DD6}	CKE≤ 0.2V Standard	–6/6E	5	5	5	mA	3
		-75	5	5	5		

Notes:
1. These parameters depend on the cycle rate and these values are measured by the cycle rate under the minimum value of tCK and tRC. Input signals are changed one time during tCK.
2. These parameter depend on output loading. Specified values are obtained with output open.
3. The temperature from -55°C~125°C

4.2 AC Characteristics

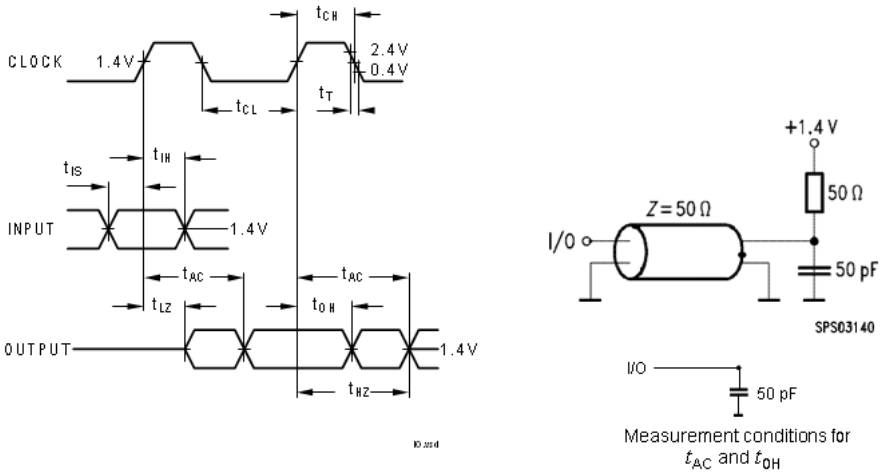
TABLE 16
AC Timing-Absolute Speccifications-6E/-6/75

Parameter	Symbol	–6E		–6		–75		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Clock Frequency	^tCK	–6 –7.5 –20	— — —	–6 –10 –20	— — —	–7.5 –10 –20	— — —	ns ns ns	CL3 CL2 CL1
Access Time from Clock	^tAC	— — —	5.4 5.4 17	— — —	5.4 6 17	— — —	5.4 6 17	ns ns ns	CL3 CL2 CL1 3)4)5)
Clock High Pulse Width	^tCH	2	—	2.5	—	2.5	—	ns	
Clock Low Pulse Width	^tCL	2	—	2.5	—	2.5	—	ns	
Transition time	^tT	0.3	1.2	0.3	1.2	0.3	1.2	ns	
Input Setup Time	^tIS	1.5	—	1.5	—	1.5	—	ns	6)
Input Hold Time	^tIH	0.8	—	0.8	—	0.8	—	ns	6)
CKE Setup Time	^tCK	1.5	—	1.5	—	1.5	—	ns	6)
CKE Hold Time	^tCKH	0.8	—	0.8	—	0.8	—	ns	6)
Mode Register Set-up to Command delay	^tMRD	2	—	2	—	2	—	^tCK	
Power Down Exit Setup Time	^tDDE	7	0	6	0	7.5	0	ns	
Row to Column Delay Time	^tRCD	15	—	18	—	15	—	ns	7)
Row Precharge Time	^tRP	15	—	15	—	15	—	ns	7)
Row Active Time	^tRAS	42	100k	42	100k	44	120k	ns	7)
Row Cycle Time	^tRC	60	—	60	—	66	—	ns	7)
Row Cycle Time during Auto Refresh	^tRFC	67	—	60	—	66	—	ns	
Activate(a) to Activate(b) Command period	^tRRD	14	—	12	—	15	—	ns	7)
CAS(a) to CAS(b) Command period	^tCCD	1	—	1	—	1	—	^tCK	
Refresh Period (8192 cycles)	^tREF	–	64	–	64	–	64	ms	
Self Refresh Exit Time	^tSREX	67	—	70	—	75	—	ns	
Data Out Hold Time	^tOH	2.5	—	2.7	—	2.7	—	ns	3)5)
Data Out to Low Impedance Time	^tLZ	1	—	1	—	1	—	ns	
Data Out to High Impedance Time	^tHZ		5.4 6 17		5.4 6 17		5.4 6 17	ns	CL3 CL2 CL1
DQM Data Out Disable Latency	^tDQZ	—	2	—	2	—	2	^tCK	
Last Data Input to Precharge (Write without Auto Precharge)	^tWR	14	—	12	—	15	—	ns	8)
Last Data Input to Activate (Write with Auto Precharge)	^tDAL(min.)	29		30		30		ns	9)
DQM Write Mask Latency	^tDQW	0	—	0	—	0	—	^tCK	

1) VSS = 0 V; VDD, VDDQ = 3.3 V ± 0.3 V, tT = 1 ns
2) For proper power-up see the operation section of this data sheet.
3) AC timing tests for LV-TTL versions have VIL = 0.4 V and VIH = 2.4 V with the timing referenced to the 1.4 V crossover point. The transition time is measured between VIH and VIL. All AC measurements assume tT = 1 ns with the AC output load circuit shown in figure below. Specified tAC and tOH parameters are measured with a 50 pF only, without any resistive termination and with an input signal of 1V /

ns edge rate between 0.8 V and 2.0 V.
4) If clock rising time is longer than 1 ns, a time (tT/2 - 0.5) ns has to be added to this parameter.
5) Access time from clock tac is 4.6 ns for PC133 components with no termination and 0 pF load, Data out hold time toh is 1.8 ns for PC133 components with no termination and 0 pF load.
6) If tT is longer than 1 ns, a time (tT - 1) ns has to be added to this parameter.
7) These parameter account for the number of clock cycles and depend on the operating frequency of the clock, as follows:
the number of clock cycles = specified value of timing period (counted in fractions as a whole number)
8) It is recommended to use two clock cycles between the last data-in and the precharge command in case of a write command without Auto-Precharge. One clock cycle between the last data-in and the precharge command is also supported, but restricted to cycle times tCK greater or equal the specified tWR value, where tck is equal to the actual system clock time.
9) When a Write command with Auto Precharge has been issued, a time of tDAL(min) has be fullfilled before the next Activate Command can be applied. For each of the terms, if not already an integer, round up to the next highest integer. tCK is equal to the actual system clock time.

FIGURE 4
AC Output Load Circuit Diagram / Timing Reference Load



Measurement conditions for t_{AC} and t_{OH}

5 Package Outlines

FIGURE 5
Package Outline FBGA54

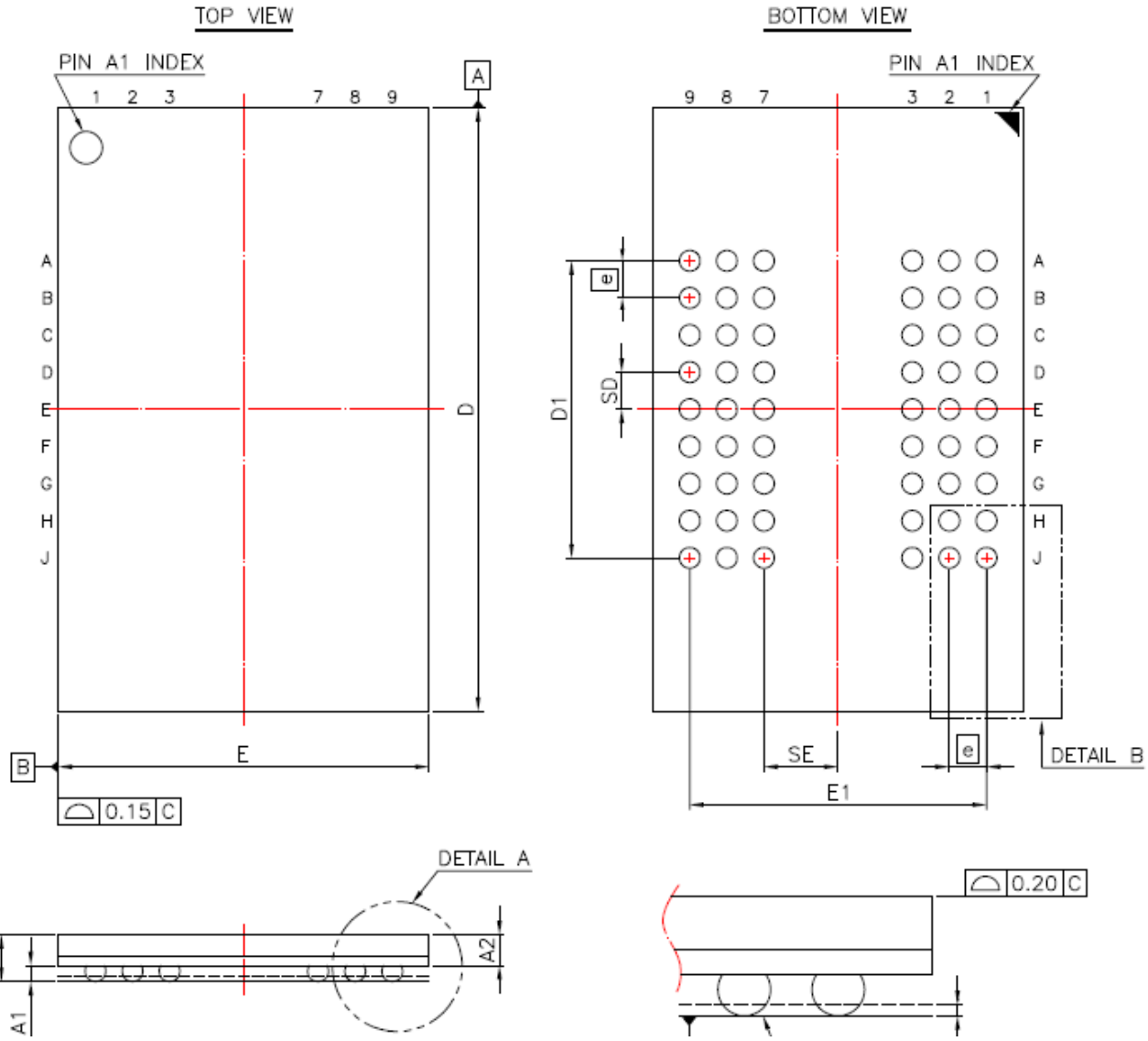


FIGURE 6
Package Outline FBGA54

SYM.	DIMENSION (mm)			DIMENSION (inch)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.25	—	0.40	0.010	—	0.016
A2	—	0.79	—	—	0.031	—
b	0.40	0.45	0.50	0.016	0.018	0.020
D	12.90	13.00	13.10	0.508	0.512	0.516
D1	6.400 BSC			0.252 BSC		
E	7.90	8.00	8.10	0.311	0.315	0.319
E1	6.400 BSC			0.252 BSC		
SE	1.600 TYP			0.063 TYP		
SD	0.800 TYP			0.031 TYP		
e	0.800 BSC			0.031 BSC		

NOTE:
1. CONTROLLING DIMENSION : MILLIMETER.
2. REFERENCE DOCUMENT : JEDEC MO-207.

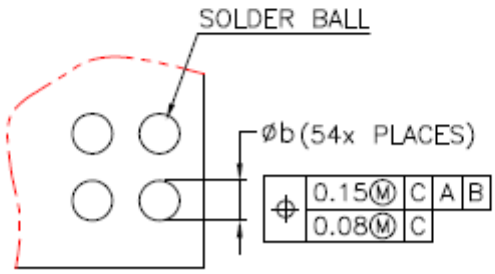


FIGURE 7
Package Outline FBGA90

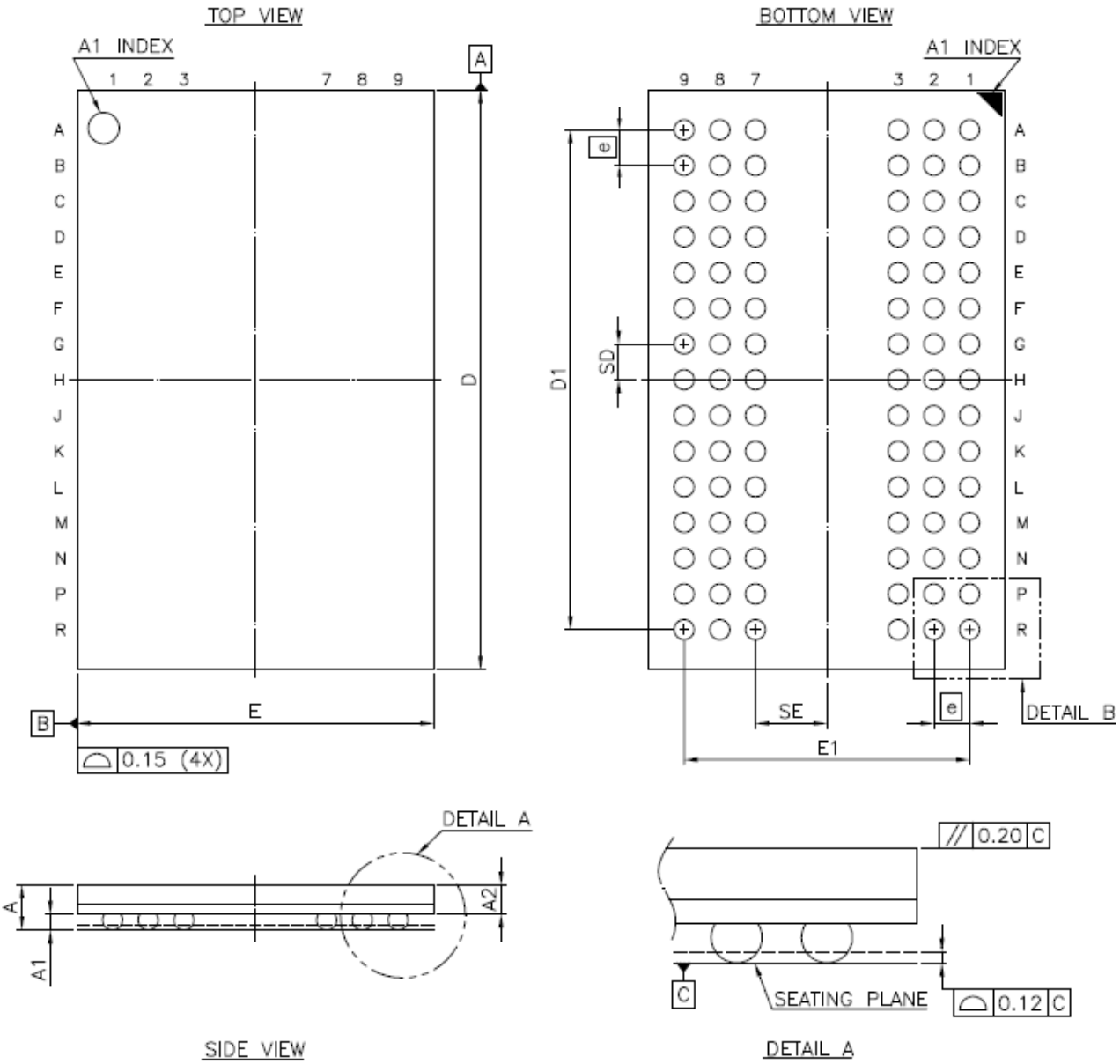
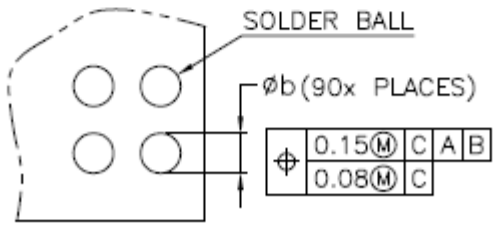


FIGURE 8
Package Outline FBGA90

SYM.	DIMENSION (mm)			DIMENSION (inch)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.25	—	0.40	0.010	—	0.016
A2	—	0.79	—	—	0.031	—
b	0.40	0.45	0.50	0.016	0.018	0.020
D	12.90	13.00	13.10	0.508	0.512	0.516
D1	11.200 BSC			0.441 BSC		
E	7.90	8.00	8.10	0.311	0.315	0.319
E1	6.400 BSC			0.252 BSC		
SE	1.600 TYP			0.063 TYP		
SD	0.800 TYP			0.031 TYP		
e	0.800 BSC			0.031 BSC		

NOTE:
1. CONTROLLING DIMENSION : MILLIMETER.
2. REFERENCE DOCUMENT : JEDEC MO-210.



DETAIL B

6 Product Nomenclature

For reference the UniIC SDRAM component nomenclature is enclosed in this chapter.

TABLE 17
Examples for Nomenclature Fields

Example for	Field Number									
	1	2	3	4	5	6	7	8	9	10
SDRAM	SCB	33	S	512	32/16/80	0	A	E	6B	I

TABLE 18
SDR Memory Components

Field	Description	Values	Coding
1	SCSemicon Component Prefix	SCB	Memory components
2	DRAM Volatge	33	33= 3.3V
3	DRAM generatio	S	S=SDRAM
4	Component Density [Mbit]	64	64 Mbit
		128	128 Mbit
		256	256 Mbit
		512	512 Mbit
5	Number of I/Os	32	× 32
		16	× 16
		80	× 8
6	Die numbers	0	monolithic
		2	2 die stack
		4	4 die stack
7	Die Revision	A	First
		B	Second
		C	Third
8	Package, Lead-Free Status	C	FBGA black
		T	TSOPII black
		E	TSOPII green
		F	FBGA green
		G	TSOP stack green
9	Speed Grade	75B	SDR–133 3–3–3
		6EB	SDR–166 3–3–3
		6B	SDR–166 3–3–3
		5B	SDR–200 3–3–3
10	Operating Temperature	Blank	Standard temperature range (0°C – +70 °C)
		I	Industrial temperature range (-40°C – +85 °C)
		A2	Automotive grade 2(-40°C – +105°C)
		X	High-Rel, temperature range (-55°C – +125 °C)

List of Illustrations

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