

2016-03



# **HXMSH4GP13A1F1C-13H**

**240-Pin PARITY RDIMM DDR3 SDRAM Modules**  
**EU RoHS Compliant**

## **Data Sheet**

**Rev. B**



| Revision History: |          |  |
|-------------------|----------|--|
| Date              | Revision | Subjects (major changes since last revision) |
| 2013/08/01        | A        | Initial Release                              |
| 2016/03/01        | B        | Change to UnilC Format                       |

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# Table of Contents

|     |   |    |
|-----|---|----|
| 1   | Overview .....                                | 3  |
| 1.1 | Features .....                                | 3  |
| 1.2 | Description .....                             | 4  |
| 2   | Pin Configurations .....                      | 5  |
| 2.1 | Pin Configurations.....                       | 5  |
| 3   | General Description.....                      | 13 |
| 3.1 | General Description .....                     | 13 |
| 3.2 | Fly-by topology.....                          | 13 |
| 3.3 | Serial Presence-Detect EEPROM Operation ..... | 13 |
| 3.4 | Register and PLL Operation .....              | 13 |
| 4   | Electrical Characteristics.....               | 14 |
| 4.1 | Absolute Maximum Ratings .....                | 14 |
| 4.2 | Operating Conditions.....                     | 15 |
| 4.3 | Module and Component Speed Grades.....        | 16 |
| 4.4 | AC Timing Requirements.....                   | 17 |
| 4.5 | $I_{DD}$ Specifications and Conditions .....  | 18 |
| 5   | Package Dimensions.....                       | 21 |

# 1 Overview

This chapter gives an overview of the 240-pin Register DDR3 SDRAM modules product family and describes its main characteristics.

## 1.1 Features

- 240-Pin PC3-10600 DDR3 SDRAM memory modules.
- Dual rank 512M x 72 module organization, by 18pcs 256M x 8 chips organization.
- 4GB Modules built with 2Gbit DDR3 SDRAMs in chip size package FBGA-78 ball.
- Standard Double-Data-Rate-Three Synchronous DRAMs (DDR3 SDRAM) with a single + 1.5 V ( $\pm 0.075V$ ) power supply.
- All speed grades faster than DDR3-1333 complies with DDR3-1333 timing specifications.
- Programmable CAS Latencies (6, 7, 8, 9), Burst Length 8, Burst Chop 4 (BC4) .
- Auto Refresh (CBR) and Self Refresh.
- Auto Refresh for temperatures above 85 °C  $t_{REFI} = 3.9 \mu s$ .
- Programmable self refresh rate via EMRS2 setting.
- Programmable partial array refresh via EMRS2 settings.
- DCC enabling via EMRS2 setting.
- All inputs and outputs SSTL\_1.5 compatible.
- Off-Chip Driver Impedance Adjustment (OCD) and On-Die Termination (ODT).
- Serial Presence Detect with E<sup>2</sup>PROM.
- VLP-RDIMM Dimensions (nominal): 30 mm high, 133.35 mm wide
- Based on standard reference layouts.

**TABLE 1**  
Module Performance Table

| UnilC Speed Code        |     |           | -13H   | Unit     | Note |
|-------------------------|-----|-----------|--------|----------|------|
| DRAM Speed Grade        |     | DDR3      | -1333  |          |      |
| Module Speed Grade      |     | PC3       | -10600 |          |      |
| CAS-RCD-RP latencies    |     |           | 9-9-9  | $t_{CK}$ |      |
| Max. Clock Frequency    | CL6 | $f_{CK6}$ | 400    | MHz      |      |
|                         | CL7 | $f_{CK7}$ | 533    | MHz      |      |
|                         | CL8 | $f_{CK8}$ | 533    | MHz      |      |
|                         | CL9 | $f_{CK9}$ | 667    | MHz      |      |
| Min. RAS-CAS-Delay      |     | $t_{RCD}$ | 13.5   | ns       |      |
| Min. Row Precharge Time |     | $t_{RP}$  | 13.5   | ns       |      |
| Min. Row Active Time    |     | $t_{RAS}$ | 36     | ns       |      |
| Min. Row Cycle Time     |     | $t_{RC}$  | 49.5   | ns       |      |

## 1.2 Description

The UniIC HXMSH4GP13A1F1C-13H module family are Register DIMM modules with 30 mm height based on DDR3 technology. DIMMs are available as ECC modules in 512M × 72 (4GB) in organization and density, intended for mounting into 240-pin connector sockets.

The memory array is designed with 2Gbit Double-Data-Rate-Three (DDR3) Synchronous DRAMs. Decoupling capacitors are mounted on the PCB board. The DIMMs feature serial presence detect based on a serial E<sup>2</sup>PROM device using the 2-pin I<sup>2</sup>C protocol. The first 128 bytes are programmed with configuration data and are write protected; the second 128 bytes are available to the customer.



**TABLE 2**  
Ordering Information

| Product Type <sup>1)</sup> | Compliance Code <sup>2)</sup> | Description  | SDRAM Technology |
|----------------------------|-------------------------------|--------------|------------------|
| <b>PC3-10600 (9-9-9)</b>   |                               |              |                  |
| HXMSH4GP13A1F1C-13H        | 4GB 2R×8 PC3-10600-999        | 2 Ranks, ECC | 2Gbit (×8)       |

- 1) For detailed information regarding Product Type of UniIC please see chapter "Product Type Nomenclature" of this data sheet.
- 2) The Compliance Code is printed on the module label and describes the speed grade, for example "PC3-10600-999" where 10600 means Register DIMM modules with 10.60 GB/sec Module Bandwidth and "999" means Column Address Strobe (CAS) latency=9, Row Column Delay (RCD) latency = 9 and Row Precharge (RP) latency = 9.

**TABLE 3**  
Address Format

| DIMM Density | Module Organization | Memory Ranks | ECC/ Non-ECC | # of SDRAMs | # of row/bank/column bits |
|--------------|---------------------|--------------|--------------|-------------|---------------------------|
| 4GB          | 512M × 72           | 2            | ECC          | 18          | 15/3/10                   |

**TABLE 4**  
Components on Modules

| DRAM Components <sup>1)2)</sup> | DRAM Density | DRAM Organization |
|---------------------------------|--------------|-------------------|
| HXB15H2G800AF-13K               | 2Gbit        | 256M × 8          |

- 1) Green Product
- 2) For a detailed description of all functionalities of the DRAM components on these modules see the component data sheet.

## 2 Pin Configurations

### 2.1 Pin Configurations

The pin configuration of the Register DDR3 SDRAM DIMM is listed by function in **Table 5** (240 pins). The abbreviations used in columns Pin Type and Buffer Type are explained in **Table 6** and **Table 7** respectively. The Pin numbering is depicted in **Figure 1**

| <b>TABLE 5</b>              |      |          |             |  |
|-----------------------------|------|----------|-------------|--|
| Pin Configuration of R-DIMM |      |          |             |  |
| Pin No.                     | Name | Pin Type | Buffer Type | Function   |
| <b>Clock Signals</b>        |      |          |             |  |
| 184                         | CK0  | I        | SSTL        | <b>Clock Signals CK0, Complement Clock Signals bCK0</b><br>The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and the falling edge of bCK. A Delay Locked Loop (DLL) circuit is driven from the clock inputs and output timing for read operations is synchronized to the input clock.   |
| 185                         | bCK0 | I        | SSTL        |  |
| 50                          | CKE0 | I        | SSTL        | <b>Clock Enable Rank 1:0</b><br>Activates the DDR3 SDRAM CK signal when HIGH and deactivates the CK signal when LOW. By deactivating the clocks, CKE LOW initiates the Power Down Mode or the Self Refresh Mode.<br><i>Note: 2 Ranks module</i>  |
| 169                         | CKE1 | I        | SSTL        |  |
|                             | NC   | NC       | —           | <b>Not Connected</b>   |
| <b>Control Signals</b>      |      |          |             |  |
| 193                         | bS0  | I        | SSTL        | <b>Chip Select Rank 1:0</b><br>Enables the associated DDR3 SDRAM command decoder when LOW and disables the command decoder when HIGH. When the command decoder is disabled, new commands are ignored but previous operations continue. Rank 0 is selected by bS0; Rank 1 is selected by bS1. Rank 2 is selected by Bs2; Rank 3 is selected by bS3. Ranks are also called "Physical banks". |
| 76                          | bS1  | I        | SSTL        |  |
| 79                          | bS2  | I        | SSTL        |  |
| 198                         | bS3  | I        | SSTL        |  |
| 192                         | bRAS | I        | SSTL        | <b>Row Address Strobe</b><br>When sampled at the cross point of the rising edge of CK, and falling edge of bCK, bRAS, bCAS and bWE define the operation to be executed by the SDRAM.   |
| 74                          | bCAS | I        | SSTL        | <b>Column Address Strobe</b>   |

| Pin No.                | Name   | Pin Type | Buffer Type | Function  |  |
|------------------------|--------|----------|-------------|---|--|
| 73                     | bWE    | I        | SSTL        | <b>Write Enable</b>   |  |
| 168                    | bRESET | I        | SSTL        | <b>Register Reset</b>   |  |
| <b>Address Signals</b> |        |          |             |   |  |
| 71                     | BA0    | I        | SSTL        | <b>Bank Address Bus 2:0</b><br>Selects which DDR3 SDRAM internal bank of four or eight is activated.  |  |
| 190                    | BA1    | I        | SSTL        |   |  |
| 52                     | BA2    | I        | SSTL        | <b>Bank Address Bus 2</b><br>Greater than 512Mb DDR3 SDRAMS   |  |
|                        | NC     | NC       | SSTL        | <b>Less than 1Gb DDR3 SDRAMS</b>  |  |
| 188                    | A0     | I        | SSTL        | <b>Address Bus 12:0</b><br>During a Bank Activate command cycle, defines the row address when sampled at the cross-point of the rising edge of CK and falling edge of bCK. During a Read or Write command cycle, defines the column address when sampled at the cross point of the rising edge of CK and falling edge of bCK. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is HIGH, autoprecharge is selected and BA0-BAn defines the bank to be precharged. If AP is LOW, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0-BAn to control which bank(s) to precharge. If AP is HIGH, all banks will be precharged regardless of the state of BA0-BAn inputs. If AP is LOW, then BA0-BAn are used to define which bank to precharge. |  |
| 181                    | A1     | I        | SSTL        |   |  |
| 61                     | A2     | I        | SSTL        |   |  |
| 180                    | A3     | I        | SSTL        |   |  |
| 59                     | A4     | I        | SSTL        |   |  |
| 58                     | A5     | I        | SSTL        |   |  |
| 178                    | A6     | I        | SSTL        |   |  |
| 56                     | A7     | I        | SSTL        |   |  |
| 177                    | A8     | I        | SSTL        |   |  |
| 175                    | A9     | I        | SSTL        |   |  |
| 70                     | A10    | I        | SSTL        |   |  |
|                        | AP     | I        | SSTL        |   |  |
| 55                     | A11    | I        | SSTL        |   |  |
| 174                    | A12    | I        | SSTL        |   | <b>Address Signal 12</b><br><i>Note: Module based on 256 Mbit or larger dies</i> |
| 196                    | A13    | I        | SSTL        |   | <b>Address Signal 13</b><br><i>Note: 1 Gbit based module</i>                     |
|                        | NC     | NC       | —           | <b>Not Connected</b><br><i>Note: Module based on 512 Mbit or smaller dies</i>   |  |
| 172                    | A14    | I        | SSTL        | <b>Address Signal 14</b><br><i>Note: 2 Gbit based module</i>  |  |
| 171                    | A15    | I        | SSTL        | <b>Address Signal 15</b><br><i>Note: 4 Gbit based module</i>  |  |
| <b>Data Signals</b>    |        |          |             |   |  |
| 3                      | DQ0    | I/O      | SSTL        | <b>Data Bus 63:0</b><br><i>Note: Data Input / Output pins</i>   |  |
| 4                      | DQ1    | I/O      | SSTL        |   |  |
| 9                      | DQ2    | I/O      | SSTL        |   |  |
| 10                     | DQ3    | I/O      | SSTL        |   |  |
| 122                    | DQ4    | I/O      | SSTL        |   |  |
| 123                    | DQ5    | I/O      | SSTL        |   |  |
| 128                    | DQ6    | I/O      | SSTL        |   |  |
| 129                    | DQ7    | I/O      | SSTL        |   |  |
| 12                     | DQ8    | I/O      | SSTL        |   |  |

| Pin No. | Name | Pin Type | Buffer Type | Function  |
|---------|------|----------|-------------|---|
| 13      | DQ9  | I/O      | SSTL        | <b>Data Bus 63:0</b><br><i>Note: Data Input / Output pins</i> |
| 18      | DQ10 | I/O      | SSTL        |   |
| 19      | DQ11 | I/O      | SSTL        |   |
| 131     | DQ12 | I/O      | SSTL        |   |
| 132     | DQ13 | I/O      | SSTL        |   |
| 137     | DQ14 | I/O      | SSTL        |   |
| 138     | DQ15 | I/O      | SSTL        |   |
| 21      | DQ16 | I/O      | SSTL        |   |
| 22      | DQ17 | I/O      | SSTL        |   |
| 27      | DQ18 | I/O      | SSTL        |   |
| 28      | DQ19 | I/O      | SSTL        |   |
| 140     | DQ20 | I/O      | SSTL        |   |
| 141     | DQ21 | I/O      | SSTL        |   |
| 146     | DQ22 | I/O      | SSTL        |   |
| 147     | DQ23 | I/O      | SSTL        |   |
| 30      | DQ24 | I/O      | SSTL        |   |
| 31      | DQ25 | I/O      | SSTL        |   |
| 36      | DQ26 | I/O      | SSTL        |   |
| 37      | DQ27 | I/O      | SSTL        |   |
| 149     | DQ28 | I/O      | SSTL        |   |
| 150     | DQ29 | I/O      | SSTL        |   |
| 155     | DQ30 | I/O      | SSTL        |   |
| 156     | DQ31 | I/O      | SSTL        |   |
| 81      | DQ32 | I/O      | SSTL        |   |
| 82      | DQ33 | I/O      | SSTL        |   |
| 87      | DQ34 | I/O      | SSTL        |   |
| 88      | DQ35 | I/O      | SSTL        |   |
| 200     | DQ36 | I/O      | SSTL        |   |
| 201     | DQ37 | I/O      | SSTL        |   |
| 206     | DQ38 | I/O      | SSTL        |   |
| 207     | DQ39 | I/O      | SSTL        |   |
| 90      | DQ40 | I/O      | SSTL        |   |
| 91      | DQ41 | I/O      | SSTL        |   |
| 96      | DQ42 | I/O      | SSTL        |   |
| 97      | DQ43 | I/O      | SSTL        |   |
| 209     | DQ44 | I/O      | SSTL        |   |
| 210     | DQ45 | I/O      | SSTL        |   |
| 215     | DQ46 | I/O      | SSTL        |   |
| 216     | DQ47 | I/O      | SSTL        |   |
| 99      | DQ48 | I/O      | SSTL        |   |



| Pin No.                    | Name  | Pin Type | Buffer Type | Function   |
|----------------------------|-------|----------|-------------|--|
| 100                        | DQ49  | I/O      | SSTL        | <b>Data Bus 63:0</b><br>Note: Data Input / Output pins   |
| 105                        | DQ50  | I/O      | SSTL        |  |
| 106                        | DQ51  | I/O      | SSTL        |  |
| 218                        | DQ52  | I/O      | SSTL        |  |
| 219                        | DQ53  | I/O      | SSTL        |  |
| 224                        | DQ54  | I/O      | SSTL        |  |
| 225                        | DQ55  | I/O      | SSTL        |  |
| 108                        | DQ56  | I/O      | SSTL        |  |
| 109                        | DQ57  | I/O      | SSTL        |  |
| 114                        | DQ58  | I/O      | SSTL        |  |
| 115                        | DQ59  | I/O      | SSTL        |  |
| 227                        | DQ60  | I/O      | SSTL        |  |
| 228                        | DQ61  | I/O      | SSTL        |  |
| 233                        | DQ62  | I/O      | SSTL        |  |
| 234                        | DQ63  | I/O      | SSTL        |  |
| <b>Check Bits</b>          |       |          |             |  |
| 39                         | CB0   | I/O      | SSTL        | <b>Check Bits 7:0</b><br>Check Bit Input/Output<br>Note: NC on Non-ECC modules   |
| 40                         | CB1   | I/O      | SSTL        |  |
| 45                         | CB2   | I/O      | SSTL        |  |
| 46                         | CB3   | I/O      | SSTL        |  |
| 158                        | CB4   | I/O      | SSTL        |  |
| 159                        | CB5   | I/O      | SSTL        |  |
| 164                        | CB6   | I/O      | SSTL        |  |
| 165                        | CB7   | I/O      | SSTL        |  |
| <b>Data Strobe Signals</b> |       |          |             |  |
| 7                          | DQS0  | I/O      | SSTL        | <b>Data Strobe Bus 7:0 and Complementary Data Strobe Bus 7:0</b><br>The data strobes, associated with one data byte, sourced with data transfers. In Write mode, the data strobe is sourced by the controller and is centered in the data window. In Read mode the data strobe is sourced by the DDR3 SDRAM and is sent at the leading edge of the data window. bDQS signals are complements, and timing is relative to the cross-point of respective DQS and bDQS. If the module is to be operated in single ended strobe mode, all bDQS signals must be tied on the system board to VSS and DDR3 SDRAM mode registers programmed appropriately |
| 6                          | bDQS0 | I/O      | SSTL        |  |
| 16                         | DQS1  | I/O      | SSTL        |  |
| 15                         | bDQS1 | I/O      | SSTL        |  |
| 25                         | DQS2  | I/O      | SSTL        |  |
| 24                         | bDQS2 | I/O      | SSTL        |  |
| 34                         | DQS3  | I/O      | SSTL        |  |
| 33                         | bDQS3 | I/O      | SSTL        |  |
| 85                         | DQS4  | I/O      | SSTL        |  |
| 84                         | bDQS4 | I/O      | SSTL        |  |
| 94                         | DQS5  | I/O      | SSTL        |  |
| 93                         | bDQS5 | I/O      | SSTL        |  |
| 103                        | DQS6  | I/O      | SSTL        |  |
| 102                        | bDQS6 | I/O      | SSTL        |  |
| 112                        | DQS7  | I/O      | SSTL        |  |
| 111                        | bDQS7 | I/O      | SSTL        |  |

| Pin No.          | Name   | Pin Type | Buffer Type | Function   |
|------------------|--------|----------|-------------|--|
| 43               | DQS8   | I/O      | SSTL        |  |
| 42               | bDQS8  | I/O      | SSTL        |  |
| 125              | DQS9   | I/O      | SSTL        |  |
| 126              | bDQS9  | I/O      | SSTL        |  |
| 134              | DQS10  | I/O      | SSTL        |  |
| 135              | bDQS10 | I/O      | SSTL        |  |
| 143              | DQS11  | I/O      | SSTL        |  |
| 144              | bDQS11 | I/O      | SSTL        |  |
| 152              | DQS12  | I/O      | SSTL        |  |
| 153              | bDQS12 | I/O      | SSTL        |  |
| 203              | DQS13  | I/O      | SSTL        |  |
| 204              | bDQS13 | I/O      | SSTL        |  |
| 212              | DQS14  | I/O      | SSTL        |  |
| 213              | bDQS14 | I/O      | SSTL        |  |
| 221              | DQS15  | I/O      | SSTL        |  |
| 222              | bDQS15 | I/O      | SSTL        |  |
| 230              | DQS16  | I/O      | SSTL        |  |
| 231              | bDQS16 | I/O      | SSTL        |  |
| 161              | DQS17  | I/O      | SSTL        |  |
| 162              | bDQS17 | I/O      | SSTL        |  |
| <b>Data Mask</b> |        |          |             |  |
| 125              | DM0    | I/O      | SSTL        | <b>Data Masks 7:0</b><br>The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is LOW but blocks the write operation if it is HIGH. In Read mode, DM lines have no effect.<br><i>Note: x8 based module</i> |
| 134              | DM1    | I/O      | SSTL        |  |
| 143              | DM2    | I/O      | SSTL        |  |
| 152              | DM3    | I/O      | SSTL        |  |
| 203              | DM4    | I/O      | SSTL        |  |
| 212              | DM5    | I/O      | SSTL        |  |
| 221              | DM6    | I/O      | SSTL        |  |
| 230              | DM7    | I/O      | SSTL        |  |
| 161              | DM8    | I/O      | SSTL        |  |

| Pin No.   | Name         | Pin Type | Buffer Type | Function  |
|---|--------------|----------|-------------|---|
| <b>EEPROM</b>   |              |          |             |   |
| 118   | SCL          | I        | CMOS        | <b>Serial Bus Clock</b><br>This signal is used to clock data into and out of the SPD EEPROM and Thermal sensor.   |
| 238   | SDA          | I/O      | OD          | <b>Serial Bus Data</b><br>This is a bidirectional pin used to transfer data into and out of the SPD EEPROM and Thermal sensor. A resistor must be connected from SDA to $V_{DDSPD}$ on the motherboard to act as a pull-up. |
| 117   | SA0          | I        | CMOS        | <b>Serial Address Select Bus 1:0</b><br>Address pins used to select the SPD and Thermal sensor base address.  |
| 237   | SA1          | I        | CMOS        |   |
| 119   | SA2          | I        | CMOS        |   |
| <b>Parity</b>   |              |          |             |   |
| 53  | bERR_O<br>UT | O        | CMOS        | <b>Parity bits</b><br><i>Note: Only for modules with parity bit for address and control bus. Not connected on non-parity registered modules.</i>  |
| 68  | PAR_IN       | I        | CMOS        |   |
| <b>Power Supplies</b>   |              |          |             |   |
| 1   | $V_{REFDQ}$  | AI       | —           | <b>I/O Reference Voltage</b><br>Reference voltage for the SSTL-18 inputs.   |
| 48,49,120,240   | $V_{tt}$     | PWR      | —           | <b>Termination Voltage</b><br>Termination voltage for command and address.  |
| 236   | $V_{DDSPD}$  | PWR      | —           | <b>EEPROM Power Supply</b><br>Power supplies for Serial Presence Detect, Thermal Sensor and ground for the module.  |
| 51,54,57,60,62,65,66,69,72,75,78,170,173,176,179,182,183,186,189,191,194,197  | $V_{DD}$     | PWR      | —           | <b>Power Supply</b><br>Power supplies for core, I/O and ground for the module.  |
| 2,5,8,11,14,17,20,23,26,29,32,35,38,41,44,47,80,83,86,89,92,95,98,101,104,107,110,113,116,121,124,127,130,133,136,139,142,145,148,151,154,157,160,163,166,199,202,205,208,211,214,217,220,223,226,229,232,235,239 | $V_{SS}$     | GND      | —           | <b>Ground Plane</b><br>Power supplies for core, I/O, Serial Presence Detect, Thermal Sensor and ground for the module.  |
| <b>Other pins</b>   |              |          |             |   |
| 195   | ODT0         | I        | SSTL        | <b>On-Die Termination Control 1:0</b>   |
| 77  | ODT1         | I        | SSTL        | <b>On-Die Termination Control 1</b><br>Asserts on-die termination for DQ, DM, DQS, and bDQS signals if enabled via the DDR3 SDRAM mode register.<br><i>Note: 2 Rank modules</i>   |
| 63,64,126,135,144,153,162,204,213,222,231   | NC           | NC       | —           | <b>Not Connected</b>  |

**TABLE 6**  
Abbreviations for pin Type

| Abbreviation | Description                                 |
|--------------|---|
| I            | Standard input-only pin. Digital levels.    |
| O            | Output. Digital levels.                     |
| I/O          | I/O is a bidirectional input/output signal. |
| AI           | Input. Analog levels.                       |
| PWR          | Power                                       |
| GND          | Ground                                      |
| NC           | Not Connected                               |

**TABLE 7**  
Abbreviations for Buffer Type

| Abbreviation | Description  |
|--------------|--|
| SSTL         | Serial Stub Terminated Logic (SSTL_15)   |
| LV-CMOS      | Low Voltage CMOS   |
| CMOS         | CMOS Levels  |
| OD           | Open Drain. The corresponding pin has 2 operational states, active low and tri-state, and allows multiple devices to share as a wire-OR. |

**FIGURE 1**  
Pin Configuration Parity DIMM (240 pin)

| Pin | Front  | Pin | Front    | Pin | Front | Pin | Back | Pin | Back   | Pin | Back   |
|-----|--------|-----|----------|-----|-------|-----|------|-----|--------|-----|--------|
| 1   | VREFDQ | 41  | VSS      | 81  | DQ32  | 121 | VSS  | 161 | DM8    | 201 | DQ37   |
| 2   | VSS    | 42  | /DQS8    | 82  | DQ33  | 122 | DQ4  | 162 | NC     | 202 | VSS    |
| 3   | DQ0    | 43  | DQS8     | 83  | VSS   | 123 | DQ5  | 163 | VSS    | 203 | DM4    |
| 4   | DQ1    | 44  | VSS      | 84  | /DQS4 | 124 | VSS  | 164 | CB6    | 204 | NC     |
| 5   | VSS    | 45  | CB2      | 85  | DQS4  | 125 | DM0  | 165 | CB7    | 205 | VSS    |
| 6   | /DQS0  | 46  | CB3      | 86  | VSS   | 126 | NC   | 166 | VSS    | 206 | DQ38   |
| 7   | DQS0   | 47  | VSS      | 87  | DQ34  | 127 | VSS  | 167 | NC     | 207 | DQ39   |
| 8   | VSS    | 48  | VTT      | 88  | DQ35  | 128 | DQ6  | 168 | /RESET | 208 | VSS    |
| 9   | DQ2    | 49  | VTT      | 89  | VSS   | 129 | DQ7  | 169 | CKE1   | 209 | DQ44   |
| 10  | DQ3    | 50  | CKE0     | 90  | DQ40  | 130 | VSS  | 170 | VDD    | 210 | DQ45   |
| 11  | VSS    | 51  | VDD      | 91  | DQ41  | 131 | DQ12 | 171 | A15    | 211 | VSS    |
| 12  | DQ8    | 52  | BA2      | 92  | VSS   | 132 | DQ13 | 172 | A14    | 212 | DM5    |
| 13  | DQ9    | 53  | /ERR_OUT | 93  | /DQS5 | 133 | VSS  | 173 | VDD    | 213 | NC     |
| 14  | VSS    | 54  | VDD      | 94  | DQS5  | 134 | DM1  | 174 | A12    | 214 | VSS    |
| 15  | /DQS1  | 55  | A11      | 95  | VSS   | 135 | NC   | 175 | A9     | 215 | DQ46   |
| 16  | DQS1   | 56  | A7       | 96  | DQ42  | 136 | VSS  | 176 | VDD    | 216 | DQ47   |
| 17  | VSS    | 57  | VDD      | 97  | DQ43  | 137 | DQ14 | 177 | A8     | 217 | VSS    |
| 18  | DQ10   | 58  | A5       | 98  | VSS   | 138 | DQ15 | 178 | A6     | 218 | DQ52   |
| 19  | DQ11   | 59  | A4       | 99  | DQ48  | 139 | VSS  | 179 | VDD    | 219 | DQ53   |
| 20  | VSS    | 60  | VDD      | 100 | DQ49  | 140 | DQ20 | 180 | A3     | 220 | VSS    |
| 21  | DQ16   | 61  | A2       | 101 | VSS   | 141 | DQ21 | 181 | A1     | 221 | DM6    |
| 22  | DQ17   | 62  | VDD      | 102 | /DQS6 | 142 | VSS  | 182 | VDD    | 222 | NC     |
| 23  | VSS    | 63  | NC       | 103 | DQS6  | 143 | DM2  | 183 | VDD    | 223 | VSS    |
| 24  | /DQS2  | 64  | NC       | 104 | VSS   | 144 | NC   | 184 | CK0    | 224 | DQ54   |
| 25  | DQS2   | 65  | VDD      | 105 | DQ50  | 145 | VSS  | 185 | /CK0   | 225 | DQ55   |
| 26  | VSS    | 66  | VDD      | 106 | DQ51  | 146 | DQ22 | 186 | VDD    | 226 | VSS    |
| 27  | DQ18   | 67  | VREFCA   | 107 | VSS   | 147 | DQ23 | 187 | /EVENT | 227 | DQ60   |
| 28  | DQ19   | 68  | PAR_IN   | 108 | DQ56  | 148 | VSS  | 188 | A0     | 228 | DQ61   |
| 29  | VSS    | 69  | VDD      | 109 | DQ57  | 149 | DQ28 | 189 | VDD    | 229 | VSS    |
| 30  | DQ24   | 70  | A10/AP   | 110 | VSS   | 150 | DQ29 | 190 | BA1    | 230 | DM7    |
| 31  | DQ25   | 71  | BA0      | 111 | /DQS7 | 151 | VSS  | 191 | VDD    | 231 | NC     |
| 32  | VSS    | 72  | VDD      | 112 | DQS7  | 152 | DM3  | 192 | /RAS   | 232 | VSS    |
| 33  | /DQS3  | 73  | /WE      | 113 | VSS   | 153 | NC   | 193 | /S0    | 233 | DQ62   |
| 34  | DQS3   | 74  | /CAS     | 114 | DQ58  | 154 | VSS  | 194 | VDD    | 234 | DQ63   |
| 35  | VSS    | 75  | VDD      | 115 | DQ59  | 155 | DQ30 | 195 | ODT0   | 235 | VSS    |
| 36  | DQ26   | 76  | /S1      | 116 | VSS   | 156 | DQ31 | 196 | A13    | 236 | VDDSPD |
| 37  | DQ27   | 77  | ODT1     | 117 | SA0   | 157 | VSS  | 197 | VDD    | 237 | SA1    |
| 38  | VSS    | 78  | VDD      | 118 | SCL   | 158 | CB4  | 198 | /S3    | 238 | SDA    |
| 39  | CB0    | 79  | /S2      | 119 | SA2   | 159 | CB5  | 199 | VSS    | 239 | VSS    |
| 40  | CB1    | 80  | VSS      | 120 | VTT   | 160 | VSS  | 200 | DQ36   | 240 | VTT    |

## 3 General Description

### 3.1 General Description

DDR3 SDRAM modules are high-speed, CMOS dynamic random access memory modules that use internally configured 4 or 8-bank DDR3 SDRAM devices. DDR3 SDRAM modules use DDR architecture to achieve high-speed operation. DDR3 architecture is essentially a  $8n$ -prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR3 SDRAM module effectively consists of a single  $8n$ -bit-wide, one-clock-cycle data transfer at the internal DRAM core and eight corresponding  $n$ -bit-wide, one-half-clock-cycle data transfers at the I/O pins.

DDR3 modules use two sets of differential signals: DQS, DQS# to capture data and CK and CK# to capture commands, addresses, and control signals. Differential clocks and data strobes ensure exceptional noise immunity for these signals and provide precise crossing points to capture input signals. A bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR3 SDRAM device during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

DDR3 SDRAM modules operate from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

### 3.2 Fly-by topology

DDR3 modules use faster clock speeds than earlier DDR technologies, making signal quality more important than ever. For improved signal quality, the clock, control, command, and address buses have been routed in a fly-by topology, where each clock, control, command, and address pin on each DRAM is connected to a single trace and terminated (rather than a tree structure, where the termination is off the module near the connector). Inherent to fly-by topology, the timing skew between the clock and DQS signals can be easily accounted for by using the write-leveling feature of DDR3.

### 3.3 Serial Presence-Detect EEPROM Operation

DDR3 SDRAM modules incorporate serial presence-detect. The SPD data is stored in a 256-byte EEPROM. The first 128 bytes are programmed by UniIC to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I2C bus using the DIMM's SCL (clock) SDA (data), and SA (address) pins. Write protect (WP) is connected to VSS, permanently disabling hardware write protection.

### 3.4 Register and PLL Operation

DDR3 SDRAM modules operate in registered mode, where the command/address input signals are latched in the registers on the rising clock edge and sent to the DDR3 SDRAM devices on the following rising clock edge (data access is delayed by one clock cycle). A phase-lock loop (PLL) on the module receives and redrives the differential clock signals (CK, CK#) to the DDR3 SDRAM devices. The registers and PLL minimize system and clock loading. PLL clock timing is defined by JEDEC specifications and ensured by use of the JEDEC clock reference board. Registered mode will add one clock cycle to CL.

## 4 Electrical Characteristics

This chapter contains speed grade definition, AC timing parameter and ODT tables.

### 4.1 Absolute Maximum Ratings

**Attention: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.**

**TABLE 8**  
Absolute Maximum Ratings

| Symbol            | Parameter                                     | Rating |        | Unit | Note |
|-------------------|---|--------|--------|------|------|
|                   |   | Min.   | Max.   |      |      |
| $V_{DD}$          | Voltage on $V_{DD}$ pin relative to $V_{SS}$  | -0.4   | +1.975 | V    |      |
| $V_{DDQ}$         | Voltage on $V_{DDQ}$ pin relative to $V_{SS}$ | -0.4   | +1.975 | V    |      |
| $V_{IN}, V_{OUT}$ | Voltage on any pin relative to $V_{SS}$       | -0.4   | +1.975 | V    |      |

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to integrated circuit.

**TABLE 9**  
Module Environmental Requirements

| Parameter                                 | Symbol    | Values |      | Unit | Note |
|---|-----------|--------|------|------|------|
|   |           | Min.   | Max. |      |      |
| Operating temperature (ambient)           | $T_{OPR}$ | 0      | +65  | °C   |      |
| Storage Temperature                       | $T_{STG}$ | - 50   | +100 | °C   |      |
| Barometric Pressure (operating & storage) | PBar      | +69    | +105 | kPa  | 1)   |

1) Up to 3000m.

**TABLE 10**
**DRAM Component Operating Temperature Range**

| Symbol     | Parameter             | Rating |      | Unit | Note     |
|------------|-----------------------|--------|------|------|----------|
|            |                       | Min.   | Max. |      |          |
| $T_{CASE}$ | Operating Temperature | 0      | 95   | °C   | 1)2)3)4) |

- 1) Operating Temperature is the case surface temperature on the center / top side of the DRAM.
- 2) The operating temperature ranges are the temperatures where all DRAM specification will be supported. During operation, the DRAM case temperature must be maintained between 0 - 95 °C under all other specification parameters.
- 3) Above 85 °C the Auto-Refresh command interval has to be reduced to  $t_{REFI} = 3.9 \mu s$
- 4) When operating this product in the 85 °C to 95 °C  $T_{CASE}$  temperature range, the High Temperature Self Refresh has to be enabled by setting EMR(2) bit A7 to "1". When the High Temperature Self Refresh is enabled there is an increase of  $I_{DD6}$  by approximately 50%

## 4.2 Operating Conditions

**TABLE 11**
**Supply Voltage Levels and AC / DC Operating Conditions**

| Parameter                   | Symbol       | Values                |                      |                       | Unit | Note |
|-----------------------------|--------------|-----------------------|----------------------|-----------------------|------|------|
|                             |              | Min.                  | Typ.                 | Max.                  |      |      |
| Device Supply Voltage       | $V_{DD}$     | 1.425                 | 1.5                  | 1.575                 | V    |      |
| Output Supply Voltage       | $V_{DDQ}$    | 1.425                 | 1.5                  | 1.575                 | V    | 1)   |
| Input Reference Voltage     | $V_{REF}$    | $0.49 \times V_{DDQ}$ | $0.5 \times V_{DDQ}$ | $0.51 \times V_{DDQ}$ | V    | 2)   |
| SPD Supply Voltage          | $V_{DDSPD}$  | 3                     | —                    | 3.6                   | V    |      |
| DC Input Logic High         | $V_{IH(DC)}$ | $V_{REF} + 0.1$       | —                    | $V_{DD}$              | V    |      |
| DC Input Logic Low          | $V_{IL(DC)}$ | vss                   | —                    | $V_{REF} - 0.1$       | V    |      |
| AC Input Logic High         | $V_{IH(AC)}$ | $V_{REF} + 0.175$     | —                    |                       | V    |      |
| AC Input Logic Low          | $V_{IL(AC)}$ |                       | —                    | $V_{REF} - 0.175$     | V    |      |
| In / Output Leakage Current | $I_L$        | - 5                   | —                    | 5                     | μA   | 3)   |

- 1) Under all conditions,  $V_{DDQ}$  must be less than or equal to  $V_{DD}$ .
- 2) Peak to peak AC noise on  $V_{REF}$  may not exceed  $\pm 2\% V_{REF(DC)}$ .  $V_{REF}$  is also expected to track noise in  $V_{DDQ}$ .
- 3) Input voltage for any connector pin under test of  $0 V \leq V_{IN} \leq V_{DDQ} + 0.3 V$ ; all other pins at 0 V. Current is per pin



### 4.3 Module and Component Speed Grades

DDR3 components may exceed the listed module speed grades; module may not be available in all listed speed grades

| <b>TABLE 12</b>                          |                              |
|--|------------------------------|
| <b>Module and Component Speed Grades</b> |                              |
| <b>Module Speed Grade</b>                | <b>Component Speed Grade</b> |
| -13H                                     | 1333MHz                      |

## 4.4 AC Timing Requirements

This chapter describes the AC timing requirements.

**TABLE 13**  
AC Timing Requirements

| Symbol              | AC Characteristics Parameter   | Min                       | Max                      | Unit     |
|---------------------|--|---------------------------|--------------------------|----------|
| <b>tCK(DLL_OFF)</b> | Minimum Clock Cycle Time (DLL off mode)  | 8                         | -                        | ns       |
| <b>tCH(avg)</b>     | Average high pulse width   | 0.47                      | 0.53                     | tCK(avg) |
| <b>tCL(avg)</b>     | Average low pulse width  | 0.47                      | 0.53                     | tCK(avg) |
| <b>tDQSQ</b>        | DQS, DQS# to DQ skew, per group, per access  | -                         | 100                      | ps       |
| <b>tQH</b>          | DQ output hold time from DQS, DQS#   | 0.38                      | -                        | tCK(avg) |
| <b>tDS(base)</b>    | Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels  | 10                        | -                        | ps       |
| <b>tDH(base)</b>    | Data hold time from DQS, DQS# referenced to Vih(dc) / Vil(dc) levels   | 45                        | -                        | ps       |
| <b>tDIPW</b>        | DQ and DM Input pulse width for each input   | 360                       | -                        | ps       |
| <b>tRPRE</b>        | DQS, DQS# differential READ Preamble   | 0.9                       | -                        | tCK(avg) |
| <b>tRPST</b>        | DQS, DQS# differential READ Postamble  | 0.3                       | -                        | tCK(avg) |
| <b>tQSH</b>         | DQS, DQS# differential output high time  | 0.40                      | -                        | tCK(avg) |
| <b>tQSL</b>         | DQS, DQS# differential output low time   | 0.40                      | -                        | tCK(avg) |
| <b>tWPRE</b>        | DQS, DQS# differential WRITE Preamble  | 0.9                       | -                        | tCK(avg) |
| <b>tWPST</b>        | DQS, DQS# differential WRITE Postamble   | 0.3                       | -                        | tCK(avg) |
| <b>tDQSCK</b>       | DQS, DQS# rising edge output access time from rising CK, CK#   | -255                      | 255                      | ps       |
| <b>tLZ</b>          | DQ, DQS and DQS# low-impedance time  | -450                      | 250                      | ps       |
| <b>tHZ</b>          | DQ, DQS and DQS# high-impedance time   | -                         | 250                      | ps       |
| <b>tDQSL</b>        | DQS, DQS# differential input low pulse width   | 0.45                      | 0.55                     | tCK(avg) |
| <b>tDQSH</b>        | DQS, DQS# differential input high pulse width  | 0.45                      | 0.55                     | tCK(avg) |
| <b>tDQSS</b>        | DQS, DQS# rising edge to CK, CK# rising edge   | -0.25                     | 0.25                     | tCK(avg) |
| <b>tDSS</b>         | DQS, DQS# falling edge setup time to CK, CK# rising edge   | 0.18                      | -                        | tCK(avg) |
| <b>tDSH</b>         | DQS, DQS# falling edge hold time from CK, CK# rising edge  | 0.18                      | -                        | tCK(avg) |
| <b>tRTP</b>         | Internal READ Command to PRECHARGE Command delay   | max(4nCK, 7.5ns)          | -                        | -        |
| <b>tWTR</b>         | Delay from start of internal write transaction to internal read command  | max(4nCK, 7.5ns)          | -                        | -        |
| <b>tWR</b>          | WRITE recovery time  | 15                        | -                        | ns       |
| <b>tMRD</b>         | Mode Register Set command cycle time   | 4                         | -                        | nCK      |
| <b>tIS(base)</b>    | Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels   | 65                        | -                        | ps       |
| <b>tIH(base)</b>    | Command and Address hold time from CK, CK# referenced to Vih(dc) / Vil(dc) levels  | 140                       | -                        | ps       |
| <b>tXP</b>          | Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL | max(3nCK, 6ns)            | -                        | -        |
| <b>tCKE</b>         | CKE minimum pulse width  | max(3nCK, 5.625ns)        | -                        | -        |
| <b>tREFI</b>        | Average Periodic Refresh interval  | 85°C < TCASE < 95°C / 3.9 | 0°C < TCASE < 85°C / 7.8 | us       |

## 4.5 $I_{DD}$ Specifications and Conditions

List of tables defining  $I_{DD}$  Specifications and Conditions.

**TABLE 14**  
 $I_{DD}$  Measurement Conditions

| Parameter  | Symbol      | Note <sup>1)2)3)4)5)</sup> |
|--|-------------|----------------------------|
| <b>Operating Current 0</b><br>One bank Active - Precharge; $t_{CK} = t_{CK.MIN}$ , $t_{RC} = t_{RC.MIN}$ , $t_{RAS} = t_{RAS.MIN}$ , CKE is HIGH, CS is HIGH between valid commands. Address and control inputs are SWITCHING, Databus inputs are SWITCHING.   | $I_{DD0}$   |                            |
| <b>Operating Current 1</b><br>One bank Active - Read - Precharge; $I_{OUT} = 0$ mA, BL = 4, $t_{CK} = t_{CK.MIN}$ , $t_{RC} = t_{RC.MIN}$ , $t_{RAS} = t_{RAS.MIN}$ , $t_{RCD} = t_{RCD.MIN}$ , AL = 0, CL = CL <sub>MIN</sub> ; CKE is HIGH, CS is HIGH between valid commands. Address and control inputs are SWITCHING, Databus inputs are SWITCHING. | $I_{DD1}$   | 6)                         |
| <b>Precharge Standby Current</b><br>All banks idle; CS is HIGH; CKE is HIGH; $t_{CK} = t_{CK.MIN}$ ; Other control and address inputs are SWITCHING, Databus inputs are SWITCHING.   | $I_{DD2N}$  |                            |
| <b>Precharge Standby ODT Current</b><br>All banks idle; CS is HIGH; CKE is HIGH; $t_{CK} = t_{CK.MIN}$ ; Other control and address inputs are SWITCHING, Databus inputs are SWITCHING.   | $I_{DD2NT}$ |                            |
| <b>Precharge Power-Down Current: Slow Exit</b><br>Other control and address inputs are STABLE, Data bus inputs are FLOATING.   | $I_{DD2P0}$ |                            |
| <b>Precharge Power-Down Current: Fast Exit</b><br>Other control and address inputs are STABLE, Data bus inputs are FLOATING.   | $I_{DD2P1}$ |                            |
| <b>Precharge Quiet Standby Current</b><br>All banks idle; CS is HIGH; CKE is HIGH; $t_{CK} = t_{CK.MIN}$ ; Other control and address inputs are STABLE, Data bus inputs are FLOATING.  | $I_{DD2Q}$  |                            |
| <b>Active Standby Current</b><br>Burst Read: All banks open; Continuous burst reads; BL = 4; AL = 0, CL = CL <sub>MIN</sub> ; $t_{CK} = t_{CK.MIN}$ ; $t_{RAS} = t_{RAS.MAX}$ , $t_{RP} = t_{RP.MIN}$ ; CKE is HIGH, CS is HIGH between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING; $I_{OUT} = 0$ mA.                   | $I_{DD3N}$  |                            |
| <b>Active Power-Down Current</b><br>All banks open; $t_{CK} = t_{CK.MIN}$ , CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are FLOATING.   | $I_{DD3P}$  |                            |
| <b>Operating Current - Burst Read</b><br>All banks open; Continuous burst reads; BL = 4; AL = 0, CL = CL <sub>MIN</sub> ; $t_{CK} = t_{CKMIN}$ ; $t_{RAS} = t_{RASMAX}$ ; $t_{RP} = t_{RPMIN}$ ; CKE is HIGH, CS is HIGH between valid commands; Address inputs are SWITCHING; Data bus inputs are SWITCHING; $I_{OUT} = 0$ mA.                          | $I_{DD4R}$  | 6)                         |
| <b>Operating Current - Burst Write</b><br>All banks open; Continuous burst writes; BL = 4; AL = 0, CL = CL <sub>MIN</sub> ; $t_{CK} = t_{CK.MIN}$ ; $t_{RAS} = t_{RAS.MAX}$ , $t_{RP} = t_{RP.MAX}$ ; CKE is HIGH, CS is HIGH between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING;                                       | $I_{DD4W}$  |                            |
| <b>Burst Refresh Current</b><br>$t_{CK} = t_{CK.MIN}$ , Refresh command every $t_{RFC} = t_{RFC.MIN}$ interval, CKE is HIGH, CS is HIGH between valid commands, Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.   | $I_{DD5B}$  |                            |

| Parameter  | Symbol    | Note <sup>1)2)3)4)5)</sup> |
|--|-----------|----------------------------|
| <b>Self-Refresh Current</b><br>CKE $\leq 0.2$ V; external clock off, CK and CK at 0 V; Other control and address inputs are FLOATING, Data bus inputs are FLOATING. $I_{DD6}$ current values are guaranteed up to $T_{CASE}$ of 85 °C max. | $I_{DD6}$ |                            |
| <b>All Bank Interleave Read Current</b><br>All banks are being interleaved at minimum tRC without violating $t_{RRD}$ using a burst length of 4. Control and address bus inputs are STABLE during DESELECTS. $I_{out} = 0$ mA.             | $I_{DD7}$ | 6)                         |
| <b>Reset Current</b>   | $I_{DD8}$ |                            |

- 1)  $V_{DDQ} = 1.5\text{ V} \pm 0.1\text{ V}$ ;  $V_{DD} = 1.5\text{ V} \pm 0.1\text{ V}$
- 2)  $I_{DD}$  specifications are tested after the device is properly initialized and  $I_{DD}$  parameter are specified with ODT disabled.
- 3) Definitions for  $I_{DD}$  see [Table 16](#)
- 4) For two rank modules: All active current measurements in the same  $I_{DD}$  current mode. The other rank is in  $I_{DD2P}$  Precharge Power-Down Mode.
- 5) For details and notes see the relevant UniIC component data sheet.
- 6)  $I_{DD1}$ ,  $I_{DD4R}$  and  $I_{DD7}$  current measurements are defined with the outputs disabled ( $I_{OUT} = 0$  mA). To achieve this on module level the output buffers can be disabled using an EMRS(1) (Extended Mode Register Command) by setting A12 bit to HIGH.

**TABLE 16**

*I*<sub>DD</sub> Specification for HXMSH4GP13A1F1C-13H

| Product Type              | HXMSH4GP13A1F1C-13H | Unit | Note <sup>1)2)</sup> |
|---------------------------|---------------------|------|----------------------|
| Organization              | 4 GB                |      |                      |
|                           | 2 Rank (×8)         |      |                      |
|                           | ×72                 |      |                      |
|                           | -13H                |      |                      |
| Symbol                    | Max.                |      |                      |
| <i>I</i> <sub>DD0</sub>   | 981                 | mA   | 3)                   |
| <i>I</i> <sub>DD1</sub>   | 1161                | mA   | 3)                   |
| <i>I</i> <sub>DD2N</sub>  | 1080                | mA   | 4)                   |
| <i>I</i> <sub>DD2P0</sub> | 342                 | mA   | 4)                   |
| <i>I</i> <sub>DD2Q</sub>  | 1080                | mA   | 4)                   |
| <i>I</i> <sub>DD3N</sub>  | 1170                | mA   | 4)                   |
| <i>I</i> <sub>DD3P</sub>  | 900                 | mA   | 4)                   |
| <i>I</i> <sub>DD4R</sub>  | 2016                | mA   | 3)                   |
| <i>I</i> <sub>DD4W</sub>  | 1791                | mA   | 3)                   |
| <i>I</i> <sub>DD5B</sub>  | 1386                | mA   | 3)                   |
| <i>I</i> <sub>DD6</sub>   | 342                 | mA   | 4)                   |
| <i>I</i> <sub>DD7</sub>   | 3141                | mA   | 3)                   |

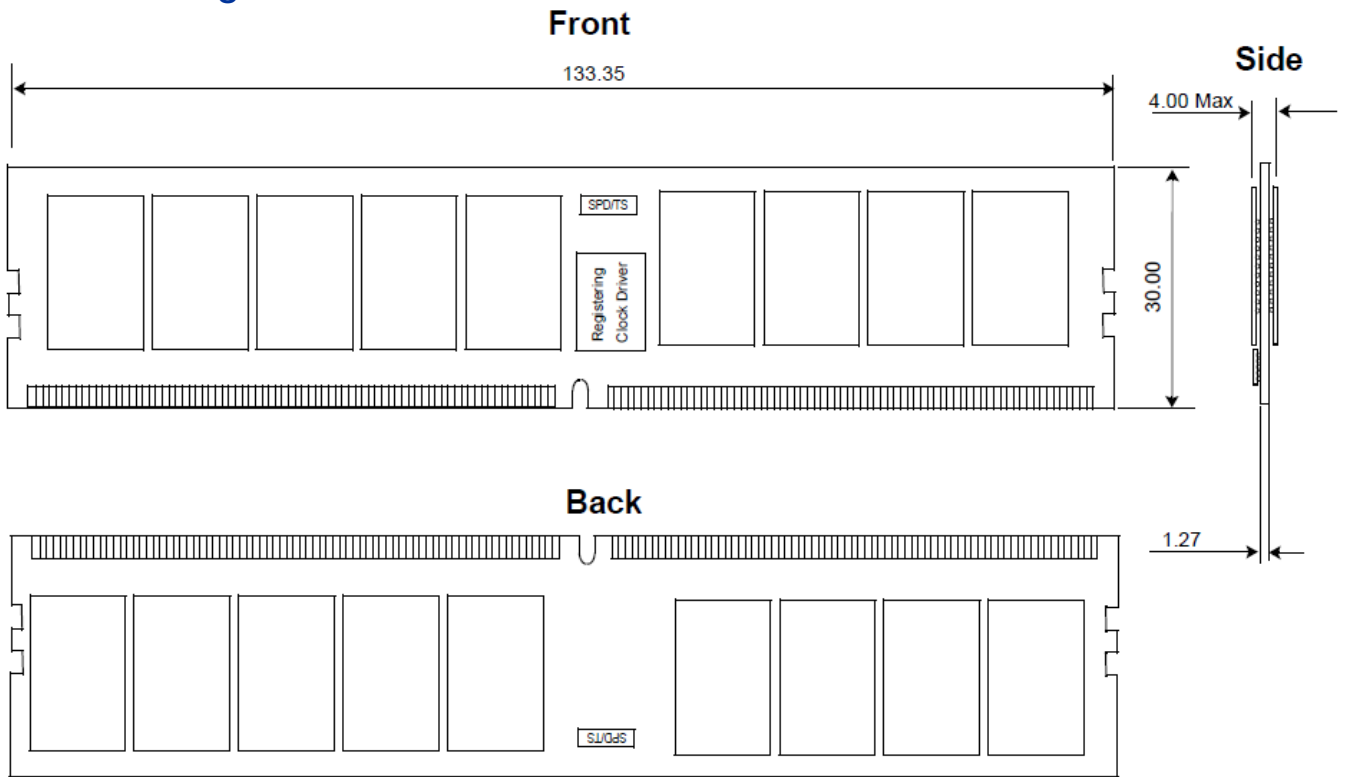
1) Calculated values from component data. ODT disabled. *I*<sub>DD1</sub>, *I*<sub>DD4R</sub> and *I*<sub>DD7</sub> are defined with the outputs disabled.

2)  $I_{DDX (rank)} = \text{Number of components} \times I_{DDX (component)}$

3)  $I_{DDX} = I_{DDX (rank)} + (\text{Rank}-1) \times I_{DD2P0 (rank)}$

4)  $I_{DDX} = \text{Rank} \times I_{DDX (rank)}$

## 5. Package Dimensions



- Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
  2. The dimensional diagram is for reference only.

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