2016-03

# HXMSH1GS03A3F1C-16KI

## 204-Pin Industrial Small Outline DDR3 SDRAM Modules EU RoHS Compliant

# Data Sheet

**Rev. A**

**Revision History:**

| Date | Revision | Subjects (major changes since last revision) |
|---|---|---|
| 2016/03/01 | A | Initial Release |

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# Table of Contents

1 Overview ........ 3
1.1 Features ........ 3
1.2 Description ........ 4
2 Pin Configurations ........ 5
2.1 Pin Configurations ........ 5
3 General Description ........ 9
3.1 General Description ........ 9
3.2 Serial Presence-Detect EEPROM Operation ........ 9
4 Electrical Characteristics ........ 10
4.1 Absolute Maximum Ratings ........ 10
4.2 Operating Conditions ........ 11
4.3 Module and Component Speed Grades ........ 12
4.4 AC Timing Requirements ........ 13
4.5 IDD Specifications and Conditions ........ 14
5 Package Dimensions ........ 20

# 1 Overview

This chapter gives an overview of the 204-pin Industrial Small Outline DDR3 SDRAM modules product family and describes its main characteristics.

## 1.1 Features

- 204-Pin PC3-12800 Industrial Small Outline DDR3 SDRAM memory modules.
- Single rank 128M x 64 module organization, by 8pcs 128M x 8 chips organization.
- 1GB Modules built with 1Gbit DDR3 SDRAMs in chipsize package FBGA-78 ball.
- Standard Double-Data-Rate-Three Synchronous DRAMs (DDR3 SDRAM) with a single + 1.5 V (± 0.075 V) power supply.
- All speed grades faster than DDR3-1600 complies with DDR3-1600 timing specifications.
- Programmable CAS Latencies (5, 6, 7, 8, 9,10,11), Burst Length 8 (BL8),Burst Chop 4（BC4）.
- Auto Refresh (CBR) and Self Refresh.
- Auto Refresh for temperatures above 85 °C $t_{REFI}$ = 3.9 μs.
- Programmable self refresh rate via MR2 setting.
- Programmable partial array refresh via MR2 settings.
- Off-Chip Driver Impedance Adjustment (OCD) and On-Die Termination (ODT).
- Serial Presence Detect with $E^2$PROM.
- Small Outline DIMM Dimensions (nominal): 30 mm high, 67.6 mm wide
- Based on standard reference layouts.

**TABLE 1**
**Module Performance Table**

| UnIC Speed Code | | | –16K | Unit | Note |
|---|---|---|---|---|---|
| **DRAM Speed Grade** | | **DDR3** | **–1600** | | |
| **Module Speed Grade** | | **PC3** | **–12800** | | |
| **CAS-RCD-RP latencies** | | | **11–11–11** | $t_{CK}$ | |
| Max. Clock Frequency | CL8 | $f_{CK8}$ | 533 | MHz | |
| | CL9 | $f_{CK9}$ | 667 | MHz | |
| | CL10 | $f_{CK10}$ | 667 | MHz | |
| | CL11 | $f_{CK11}$ | 800 | MHz | |
| Min. RAS-CAS-Delay | | $t_{RCD}$ | 13.75 | ns | |
| Min. Row Precharge Time | | $t_{RP}$ | 13.75 | ns | |
| Min. Row Active Time | | $t_{RAS}$ | 35 | ns | |
| Min. Row Cycle Time | | $t_{RC}$ | 48.75 | ns | |

## 1.2 Description

The UnilC HXMSH1GS03A3F1C-16KI module family are Low Power Small Outline DIMM modules with 30 mm height based on DDR3 technology. DIMMs are available in 128M × 64 (1GB) in organization and density, intended for mounting into 204-pin connector sockets.

The memory array is designed with 1 Gbit Double-Data-Rate-Three (DDR3) Synchronous DRAMs. Decoupling capacitors are mounted on the PCB board. The DIMMs feature serial presence detect based on a serial $E^2$PROM device using the 2-pin $I^2C$ protocol. The first 128 bytes are programmed with configuration data and are write-protected; the second 128 bytes are available to the customer.

**TABLE 2**
**Ordering Information**

| Product Type[1)] | Compliance Code[2)] | Description | SDRAM Technology |
|---|---|---|---|
| **PC3-12800 (11-11-11)** | | | |
| HXMSH1GS03A3F1C-16KI | 1GB 1R×8 PC3–12800–11-11-11 | 1 Rank | 1Gbit (×8) |

1) For detailed information regarding Product Type of UnilC please see chapter "Product Type Nomenclature" of this data sheet.
2) The Compliance Code is printed on the module label and describes the speed grade, for example "PC3–12800–11-11-11" where 12800 means DIMM modules with 12.80 GB/sec Module Bandwidth and "11-11-11" means Column Address Strobe (CAS) latency=11, Row Column Delay (RCD) latency = 11 and Row Precharge (RP) latency = 11.

**TABLE 3**
**Address Format**

| DIMM Density | Module Organization | Memory Ranks | ECC/ Non-ECC | # of SDRAMs | # of row/bank/column bits |
|---|---|---|---|---|---|
| 1GB | 128M × 64 | 1 | Non | 8 | 14/3/10 |

**TABLE 4**
**Components on Modules**

| DRAM Components[1)2)] | DRAM Density | DRAM Organization |
|---|---|---|
| SCB15H1G800AF-13KI | 1Gbit | 128M × 8 |

1) Green Product
2) For a detailed description of all functionalities of the DRAM components on these modules see the component data sheet.

# 2 Pin Configurations

## 2.1 Pin Configurations

The pin configuration of the 204-Pin Small Outline DDR3 SDRAM DIMM is listed by function in **Table 5** (204 pins). The abbreviations used in columns Pin Type and Buffer Type are explained in **Table 6** and **Table 7** respectively. The Pin numbering is depicted in **Figure 1**

**TABLE 5**
**Pin Configuration of SO-DIMM**

| Symbol | Type | Description |
|---|---|---|
| Ax | Input | **Address inputs:** Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BAx) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. See the Pin Assignments Table for density-specific addressing information. |
| BAx | Input | **Bank address inputs:** Define the device bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command. |
| CKx,<br>CKx# | Input | **Clock:** Differential clock inputs. All control, command, and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. |
| CKEx | Input | **Clock enable:** Enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM. |
| DMx | Input | **Data mask (x8 devices only):** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with that input data, during a write access. Although DM pins are input-only, DM loading is designed to match that of the DQ and DQS pins. |
| ODTx | Input | **On-die termination:** Enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to the following pins: DQ, DQS, DQS#, DM, and CB. The ODT input will be ignored if disabled via the LOAD MODE command. |
| Par_In | Input | **Parity input:** Parity bit for Ax, RAS#, CAS#, and WE#. |
| RAS#, CAS#, WE# | Input | **Command inputs:** RAS#, CAS#, and WE# (along with S#) define the command being entered. |
| RESET# | Input<br>(LVCMOS) | **Reset:** RESET# is an active LOW asychronous input that is connected to each DRAM and the registering clock driver. After RESET# goes HIGH, the DRAM must be reinitialized as though a normal power-up was executed. |
| Sx# | Input | **Chip select:** Enables (registered LOW) and disables (registered HIGH) the command decoder. |
| SAx | Input | **Serial address inputs:** Used to configure the temperature sensor/SPD EEPROM address range on the $I^2C$ bus. |

| | | |
|---|---|---|
| SCL | Input | **Serial clock for temperature sensor/SPD EEPROM:** Used to synchronize communication to and from the temperature sensor/SPD EEPROM on the $I^2C$ bus. |
| CBx | I/O | **Check bits:** Used for system error detection and correction. |
| DQx | I/O | **Data input/output:** Bidirectional data bus. |
| DQSx, DQSx# | I/O | **Data strobe:** Differential data strobes. Output with read data; edge-aligned with read data; input with write data; center-aligned with write data. |

| Symbol | Type | Description |
|---|---|---|
| SDA | I/O | **Serial data:** Used to transfer addresses and data into and out of the temperature sensor/SPD EEPROM on the $I^2C$ bus. |
| TDQSx, TDQSx# | Output | **Redundant data strobe (x8 devices only):** TDQS is enabled/disabled via the LOAD MODE command to the extended mode register (EMR). When TDQS is enabled, DM is disabled and TDQS and TDQS# provide termination resistance; otherwise, TDQS# are no function. |
| Err_Out# | Output (open drain) | **Parity error output:** Parity error found on the command and address bus. |
| EVENT# | Output (open drain) | **Temperature event:**The EVENT# pin is asserted by the temperature sensor when critical temperature thresholds have been exceeded. |
| $V_{DD}$ | Supply | **Power supply:** 1.5V ±0.075V. The component $V_{DD}$ and $V_{DDQ}$ are connected to the module $V_{DD}$. |
| $V_{DDSPD}$ | Supply | **Temperature sensor/SPD EEPROM power supply:** 3.0–3.6V. |
| $V_{REFCA}$ | Supply | **Reference voltage:** Control, command, and address $V_{DD}/2$. |
| $V_{REFDQ}$ | Supply | **Reference voltage:** DQ, DM $V_{DD}/2$. |
| $V_{SS}$ | Supply | Ground. |
| $V_{TT}$ | Supply | **Termination voltage:** Used for control, command, and address $V_{DD}/2$. |
| NC | – | **No connect:** These pins are not connected on the module. |
| NF | – | **No function:** These pins are connected within the module, but provide no functionality. |

## TABLE 6
### Abbreviations for pin Type

| Abbreviation | Description |
|---|---|
| I | Standard input-only pin. Digital levels. |
| O | Output. Digital levels. |
| I/O | I/O is a bidirectional input/output signal. |
| AI | Input. Analog levels. |
| PWR | Power |
| GND | Ground |
| NC | Not Connected |

**TABLE 7**
**Abbreviations for Buffer Type**

| Abbreviation | Description |
|---|---|
| SSTL | Serial Stub Terminated Logic |
| LV-CMOS | Low Voltage CMOS |
| CMOS | CMOS Levels |
| OD | Open Drain. The corresponding pin has 2 operational states, active low and tri-state, and allows multiple devices to share as a wire-OR. |

UniIC

**FIGURE 1**
**Pin Configuration SO-DIMM (204 pin)**

| Pin | Signal | Pin | Signal | Pin | Signal | | Pin | Signal | Pin | Signal | Pin | Signal |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | VREFDQ | 41 | DQ17 | 81 | VDD | | 121 | /S1 | 161 | VSS | 201 | SA1 |
| 2 | VSS | 42 | DQ21 | 82 | VDD | | 122 | NC | 162 | VSS | 202 | SCL |
| 3 | VSS | 43 | VSS | 83 | A12 | | 123 | VDD | 163 | DQ48 | 203 | VTT |
| 4 | DQ4 | 44 | VSS | 84 | A11 | | 124 | VDD | 164 | DQ52 | 204 | VTT |
| 5 | DQ0 | 45 | /DQS2 | 85 | A9 | | 125 | TEST | 165 | DQ49 | | |
| 6 | DQ5 | 46 | DM2 | 86 | A7 | | 126 | VREFCA | 166 | DQ53 | | |
| 7 | DQ1 | 47 | DQS2 | 87 | VDD | | 127 | VSS | 167 | VSS | | |
| 8 | VSS | 48 | VSS | 88 | VDD | | 128 | VSS | 168 | VSS | | |
| 9 | VSS | 49 | VSS | 89 | A8 | | 129 | DQ32 | 169 | /DQS6 | | |
| 10 | /DQS0 | 50 | DQ22 | 90 | A6 | | 130 | DQ36 | 170 | DM6 | | |
| 11 | DM0 | 51 | DQ18 | 91 | A5 | | 131 | DQ33 | 171 | DQS6 | | |
| 12 | DQS0 | 52 | DQ23 | 92 | A4 | | 132 | DQ37 | 172 | VSS | | |
| 13 | VSS | 53 | DQ19 | 93 | VDD | | 133 | VSS | 173 | VSS | | |
| 14 | VSS | 54 | VSS | 94 | VDD | | 134 | VSS | 174 | DQ54 | | |
| 15 | DQ2 | 55 | VSS | 95 | A3 | | 135 | /DQS4 | 175 | DQ50 | | |
| 16 | DQ6 | 56 | DQ28 | 96 | A2 | | 136 | DM4 | 176 | DQ55 | | |
| 17 | DQ3 | 57 | DQ24 | 97 | A1 | | 137 | DQS4 | 177 | DQ51 | | |
| 18 | DQ7 | 58 | DQ29 | 98 | A0 | | 138 | VSS | 178 | VSS | | |
| 19 | VSS | 59 | DQ25 | 99 | VDD | | 139 | VSS | 179 | VSS | | |
| 20 | VSS | 60 | VSS | 100 | VDD | | 140 | DQ38 | 180 | DQ60 | | |
| 21 | DQ8 | 61 | VSS | 101 | CK0 | | 141 | DQ34 | 181 | DQ56 | | |
| 22 | DQ12 | 62 | /DQS3 | 102 | CK1 | | 142 | DQ39 | 182 | DQ61 | | |
| 23 | DQ9 | 63 | DM3 | 103 | /CK0 | | 143 | DQ35 | 183 | DQ57 | | |
| 24 | DQ13 | 64 | DQS3 | 104 | /CK1 | | 144 | VSS | 184 | VSS | | |
| 25 | VSS | 65 | VSS | 105 | VDD | | 145 | VSS | 185 | VSS | | |
| 26 | VSS | 66 | VSS | 106 | VDD | | 146 | DQ44 | 186 | /DQS7 | | |
| 27 | /DQS1 | 67 | DQ26 | 107 | A10/AP | | 147 | DQ40 | 187 | DM7 | | |
| 28 | DM1 | 68 | DQ30 | 108 | BA1 | | 148 | DQ45 | 188 | DQS7 | | |
| 29 | DQS1 | 69 | DQ27 | 109 | BA0 | | 149 | DQ41 | 189 | VSS | | |
| 30 | /RESET | 70 | DQ31 | 110 | /RAS | | 150 | VSS | 190 | VSS | | |
| 31 | VSS | 71 | VSS | 111 | VDD | | 151 | VSS | 191 | DQ58 | | |
| 32 | VSS | 72 | VSS | 112 | VDD | | 152 | /DQS5 | 192 | DQ62 | | |
| 33 | DQ10 | 73 | CKE0 | 113 | /WE | | 153 | DM5 | 193 | DQ59 | | |
| 34 | DQ14 | 74 | CKE1 | 114 | /S0 | | 154 | DQS5 | 194 | DQ63 | | |
| 35 | DQ11 | 75 | VDD | 115 | /CAS | | 155 | VSS | 195 | VSS | | |
| 36 | DQ15 | 76 | VDD | 116 | ODT0 | | 156 | VSS | 196 | VSS | | |
| 37 | VSS | 77 | NC | 117 | VDD | | 157 | DQ42 | 197 | SA0 | | |
| 38 | VSS | 78 | A15 | 118 | VDD | | 158 | DQ46 | 198 | NC | | |
| 39 | DQ16 | 79 | BA2 | 119 | A13 | | 159 | DQ43 | 199 | VDDSPD | | |
| 40 | DQ20 | 80 | A14 | 120 | ODT1 | | 160 | DQ47 | 200 | SDA | | |

# 3 General Description

## 3.1 General Description

DDR3 SDRAM modules are high-speed, CMOS dynamic random access memory modules that use internally configured 4 or 8-bank DDR3 SDRAM devices. DDR3 SDRAM modules use DDR architecture to achieve high-speed operation. DDR3 architecture is essentially a 8*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR3 SDRAM module effectively consists of a single 8*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and eight corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

DDR3 modules use two sets of differential signals: DQS, DQS# to capture data and CK and CK# to capture commands, addresses, and control signals. Differential clocks and data strobes ensure exceptional noise immunity for these signals and provide precise crossing points to capture input signals. A bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR3 SDRAM device during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

DDR3 SDRAM modules operate from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

## 3.2 Serial Presence-Detect EEPROM Operation

DDR3 SDRAM modules incorporate serial presence-detect. The SPD data is stored in a 256-byte EEPROM. The first 128 bytes are programmed by UniIC to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I2C bus using the DIMM’s SCL (clock) SDA (data), and SA (address) pins. Write protect (WP) is connected to VSS, permanently disabling hardware write protection.

# 4 Electrical Characteristics

This chapter contains speed grade definition, AC timing parameter and ODT tables.

## 4.1 Absolute Maximum Ratings

***Attention: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.***

**TABLE 8**
**Absolute Maximum Ratings**

| Symbol | Parameter | Rating | | Unit | Note |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| $V_{DD}$ | Voltage on $V_{DD}$ pin relative to $V_{SS}$ | –0.4 | +1.975 | V | |
| $V_{DDQ}$ | Voltage on $V_{DDQ}$ pin relative to $V_{SS}$ | –0.4 | +1.975 | V | |
| $V_{IN}$, $V_{OUT}$ | Voltage on any pin relative to $V_{SS}$ | –0.4 | +1.975 | V | |

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to integrated circuit.

**TABLE 9**
**Module Environmental Requirements**

| Parameter | Symbol | Values | | Unit | Note |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| Operating temperature (ambient) | $T_{OPR}$ | 0 | +65 | ℃ | |
| Storage Temperature | $T_{STG}$ | – 50 | +100 | ℃ | |
| Barometric Pressure (operating & storage) | PBar | +69 | +105 | kPa | 1) |

1) Up to 3000m.

**TABLE 10**
**DRAM Component Operating Temperature Range**

| Symbol | Parameter | Rating | | Unit | Note |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| $T_{CASE}$ | Operating Temperature | -40 | 95 | °C | 1)2)3)4) |

1) Operating Temperature is the case surface temperature on the center / top side of the DRAM.
2) The operating temperature ranges are the temperatures where all DRAM specification will be supported. During operation, the DRAM case temperature must be maintained between -40~ 95 °C under all other specification parameters.
3) Above 85 ℃ the Auto-Refresh command interval has to be reduced to $t_{REFI}$= 3.9 µs
4) When operating this product in the 85 °C to 95 °C $T_{CASE}$ temperature range, the High Temperature Self Refresh has to be enabled by setting EMR(2) bit A7 to "1". When the High Temperature Self Refresh is enabled there is an increase of $I_{DD6}$ by approximately 50%

## 4.2 Operating Conditions

**TABLE 11**
**Supply Voltage Levels and AC / DC Operating Conditions**

| Parameter | Symbol | Values | | | Unit | Note |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Device Supply Voltage | $V_{DD}$ | 1.425 | 1.5 | 1.575 | V | |
| Output Supply Voltage | $V_{DDQ}$ | 1.425 | 1.5 | 1.575 | V | 1) |
| Input Reference Voltage | $V_{REF}$ | $0.49 \times V_{DDQ}$ | $0.5 \times V_{DDQ}$ | $0.51 \times V_{DDQ}$ | V | 2) |
| SPD Supply Voltage | $V_{DDSPD}$ | 3 | — | 3.6 | V | |
| DC Input Logic High | $V_{IH(DC)}$ | $V_{REF}$ + 0.1 | — | $V_{DDQ}$ | V | |
| DC Input Logic Low | $V_{IL\ (DC)}$ | vss | — | $V_{REF}$ – 0.1 | V | |
| AC Input Logic High | $V_{IH(AC)}$ | $V_{REF}$ + 0.175 | — | | V | |
| AC Input Logic Low | $V_{IL\ (AC)}$ | | — | $V_{REF}$ –0.175 | V | |
| In / Output Leakage Current | $I_L$ | – 5 | — | 5 | µA | 3) |

1) Under all conditions, $V_{DDQ}$ must be less than or equal to $V_{DD}$
2) Peak to peak AC noise on $V_{REF}$ may not exceed ± 2% $V_{REF}$ (DC). $V_{REF}$ is also expected to track noise in $V_{DDQ}$.
3) Input voltage for any connector pin under test of 0 V ≤ $V_{IN}$ ≤ $V_{DDQ}$ + 0.3 V; all other pins at 0 V. Current is per pin

## 4.3 Module and Component Speed Grades

DDR3 components may exceed the listed module speed grades; module may not be available in all listed speed grades

**TABLE 12**
**Module and Component Speed Grades**

| Module Speed Grade | Component Speed Grade |
| --- | --- |
| -16K | 1600MHz |

## 4.4 AC Timing Requirements

This chapter describes the AC timing requirements.

**TABLE 13**
**AC Timing Requirements**

| Symbol | AC Characteristics Parameter | Min | Max | Unit |
|---|---|---|---|---|
| **tCK(DLL_OFF)** | Minimum Clock Cycle Time (DLL off mode) | 8 | - | ns |
| **tCH(avg)** | Average high pulse width | 0.47 | 0.53 | tCK(avg) |
| **tCL(avg)** | Average low pulse width | 0.47 | 0.53 | tCK(avg) |
| **tDQSQ** | DQS, DQS# to DQ skew, per group, per access | - | 100 | ps |
| **tQH** | DQ output hold time from DQS, DQS# | 0.38 | - | tCK(avg) |
| **tDS(base)** | Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels | 10 | - | ps |
| **tDH(base)** | Data hold time from DQS, DQS# referenced to Vih(dc) / Vil(dc) levels | 45 | - | ps |
| **tDIPW** | DQ and DM Input pulse width for each input | 360 | - | ps |
| **tRPRE** | DQS,DQS# differential READ Preamble | 0.9 | - | tCK(avg) |
| **tRPST** | DQS, DQS# differential READ Postamble | 0.3 | - | tCK(avg) |
| **tQSH** | DQS, DQS# differential output high time | 0.40 | - | tCK(avg) |
| **tQSL** | DQS, DQS# differential output low time | 0.40 | - | tCK(avg) |
| **tWPRE** | DQS, DQS# differential WRITE Preamble | 0.9 | - | tCK(avg) |
| **tWPST** | DQS, DQS# differential WRITE Postamble | 0.3 | - | tCK(avg) |
| **tDQSCK** | DQS, DQS# rising edge output access time from rising CK, CK# | -225 | 225 | ps |
| **tLZ** | DQ, DQS and DQS# low-impedance time | -450 | 225 | ps |
| **tHZ** | DQ, DQS and DQS# high-impedance time | - | 225 | ps |
| **tDQSL** | DQS, DQS# differential input low pulse width | 0.45 | 0.55 | tCK(avg) |
| **tDQSH** | DQS, DQS# differential input high pulse width | 0.45 | 0.55 | tCK(avg) |
| **tDQSS** | DQS, DQS# rising edge to CK, CK# rising edge | -0.27 | 0.27 | tCK(avg) |
| **tDSS** | DQS, DQS# falling edge setup time to CK, CK# rising edge | 0.18 | - | tCK(avg) |
| **tDSH** | DQS, DQS# falling edge hold time from CK, CK# rising edge | 0.18 | - | tCK(avg) |
| **tRTP** | Internal READ Command to PRECHARGE Command delay | max(4nCK,7.5ns) | - | - |
| **tWTR** | Delay from start of internal write transaction to internal read command | max(4nCK,7.5ns) | - | - |
| **tWR** | WRITE recovery time | 15 | - | ns |
| **tMRD** | Mode Register Set command cycle time | 4 | - | nCK |
| **tIS(base)** | Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels | 45 | - | ps |
| **tIH(base)** | Command and Address hold time from CK, CK# referenced to Vih(dc) / Vil(dc) levels | 120 | - | ps |
| **tXP** | Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL | max(3nCK,6ns) | - | - |
| **tCKE** | CKE minimum pulse width | max(3nCK,5.625ns) | - | - |
| **tREFI** | Average Periodic Refresh interval | 85℃<TCASE <95℃ /3.9 | 0℃<TCASE <85℃ /7.8 | us |

## 4.5 $I_{DD}$ Specifications and Conditions

List of tables defining $I_{DD}$ Specifications and Conditions.

**TABLE 14**
**IDD Measurement Conditions**

| Parameter | Symbol | Note[1)2)3)4)5)] |
|---|---|---|
| **Operating Current 0**<br>One bank Active - Precharge; $t_{CK} = t_{CK.MIN}$, $t_{RC} = t_{RC.MIN}$, $t_{RAS} = t_{RAS.MIN}$, CKE is HIGH, CS is HIGH between valid commands. Address and control inputs are SWITCHING, Databus inputs are SWITCHING. | $I_{DD0}$ | |
| **Operating Current 1**<br>One bank Active - Read - Precharge; $I_{OUT}$ = 0 mA, BL = 4, $t_{CK} = t_{CK.MIN}$, $t_{RC} = t_{RC.MIN}$, $t_{RAS} = t_{RAS.MIN}$, $t_{RCD} = t_{RCD.MIN}$, AL = 0, CL = $CL_{MIN}$; CKE is HIGH, CS is HIGH between valid commands. Address and control inputs are SWITCHING, Databus inputs are SWITCHING. | $I_{DD1}$ | 6) |
| **Precharge Standby Current**<br>All banks idle; CS is HIGH; CKE is HIGH; $t_{CK} = t_{CK.MIN}$; Other control and address inputs are SWITCHING, Databus inputs are SWITCHING. | $I_{DD2N}$ | |
| **Precharge Power-Down Current**<br>Other control and address inputs are STABLE, Data bus inputs are FLOATING. | $I_{DD2P}$ | |
| **Precharge Quiet Standby Current**<br>All banks idle; CS is HIGH; CKE is HIGH; $t_{CK} = t_{CK.MIN}$; Other control and address inputs are STABLE, Data bus inputs are FLOATING. | $I_{DD2Q}$ | |
| **Active Standby Current**<br>Burst Read: All banks open; Continuous burst reads; BL = 4; AL = 0, CL = $CL_{MIN}$; $t_{CK} = t_{CK.MIN}$; $t_{RAS} = t_{RAS.MAX}$, $t_{RP} = t_{RP.MIN}$; CKE is HIGH, CS is HIGH between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING; $I_{OUT}$ = 0 mA. | $I_{DD3N}$ | |
| **Active Power-Down Current**<br>All banks open; $t_{CK} = t_{CK.MIN}$, CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are FLOATING. | $I_{DD3P}$ | |
| **Operating Current - Burst Read**<br>All banks open; Continuous burst reads; BL = 4; AL = 0, CL = $CL_{MIN}$; $t_{CK} = t_{CKMIN}$; $t_{RAS} = t_{RASMAX}$; $t_{RP} = t_{RPMIN}$; CKE is HIGH, CS is HIGH between valid commands; Address inputs are SWITCHING; Data bus inputs are SWITCHING; $I_{OUT}$ = 0mA. | $I_{DD4R}$ | 6) |
| **Operating Current - Burst Write**<br>All banks open; Continuous burst writes; BL = 4; AL = 0, CL = $CL_{MIN}$; $t_{CK} = t_{CK.MIN}$; $t_{RAS} = t_{RAS.MAX.}$, $t_{RP} = t_{RP.MAX}$; CKE is HIGH, CS is HIGH between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING; | $I_{DD4W}$ | |
| **Burst Refresh Current**<br>$t_{CK} = t_{CK.MIN.}$, Refresh command every $t_{RFC} = t_{RFC.MIN}$ interval, CKE is HIGH, CS is HIGH between valid commands, Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING. | $I_{DD5B}$ | |

| Parameter | Symbol | Note[1)2)3)4)5)] |
|---|---|---|
| **Self-Refresh Current**<br>CKE ≤ 0.2 V; external clock off, CK and $\overline{CK}$ at 0 V; Other control and address inputs are FLOATING, Data bus inputs are FLOATING. $I_{DD6}$ current values are guaranteed up to $T_{CASE}$ of 85 °C max. | $I_{DD6}$ | |
| **All Bank Interleave Read Current**<br>All banks are being interleaved at minimum $t_{RC}$ without violating $t_{RRD}$ using a burst length of 4. Control and address bus inputs are STABLE during DESELECTS. $I_{out}$ = 0 mA. | $I_{DD7}$ | 6) |

1) $V_{DDQ}$ = 1.35 V ±0.1 V; $V_{DD}$ = 1.35 V ±0.1 V
2) $I_{DD}$ specifications are tested after the device is properly initialized and $I_{DD}$ parameter are specified with ODT disabled.
3) Definitions for $I_{DD}$ see **Table 16**
4) For two rank modules: All active current measurements in the same $I_{DD}$ current mode. The other rank is in $I_{DD2P}$ Precharge Power-Down Mode.
5) For details and notes see the relevant UniIC component data sheet.
6) $I_{DD1}$, $I_{DD4R}$ and $I_{DD7}$ current measurements are defined with the outputs disabled ($I_{OUT}$ = 0 mA). To achieve this on module level the output buffers can be disabled using an EMRS(1) (Extended Mode Register Command) by setting A12 bit to HIGH.

## TABLE 15
### Definitions for $I_{DD}$

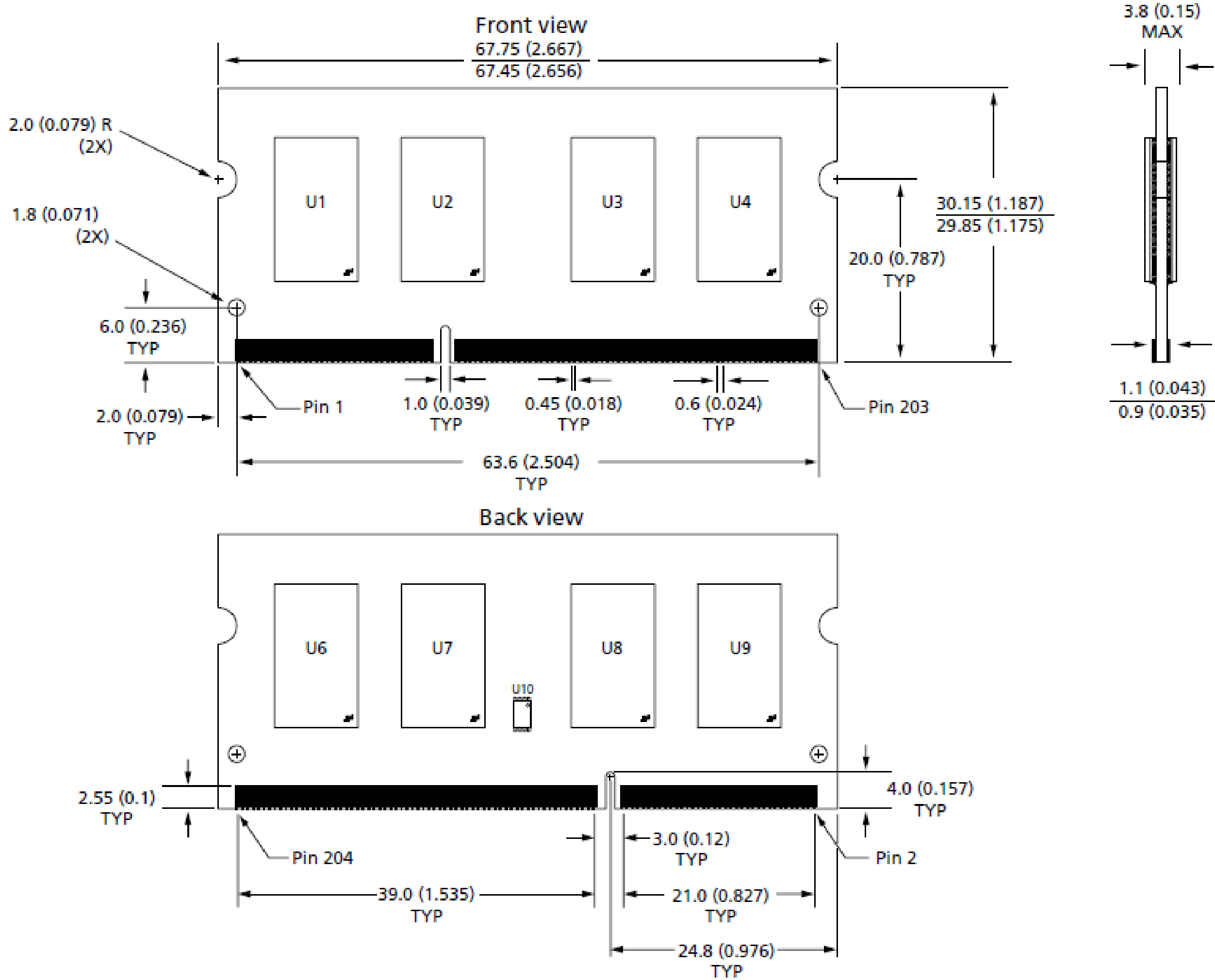
| Parameter | Description |
|---|---|
| LOW | $V_{IN} \leq V_{IL(ac).MAX}$, HIGH is defined as $V_{IN} \geq V_{IH(ac).MIN}$ |
| STABLE | Inputs are stable at a HIGH or LOW level. |
| FLOATING | Inputs are $V_{REF} = V_{DDQ}/2$ |
| SWITCHING | Inputs are changing between HIGH and LOW every other clock (once per 2 cycles) for address and control signals, and inputs changing between HIGH and LOW every other data transfer (once per cycle) for DQ signals not including mask or strobes. |

**TABLE 16**
**IDD Specification for HXMSH1GS03A3F1C-16KI**

| **Product Type** | HXMSH1GS03A3F1C-16KI | **Unit** | **Note**[1)2)] |
|---|---|---|---|
| **Organization** | **1 GB** | | |
| | **1 Rank (×8)** | | |
| | **×64** | | |
| | **-16KI** | | |
| **Symbol** | **Max.** | | |
| $I_{DD0}$ | 640 | mA | 3) |
| $I_{DD1}$ | 760 | mA | 3) |
| $I_{DD2N}$ | 480 | mA | 4) |
| $I_{DD2P0}$ | 96 | mA | 4) |
| $I_{DD2Q}$ | 480 | mA | 4) |
| $I_{DD3N}$ | 520 | mA | 4) |
| $I_{DD3P}$ | 400 | mA | 4) |
| $I_{DD4R}$ | 1440 | mA | 3) |
| $I_{DD4W}$ | 1600 | mA | 3) |
| $I_{DD5B}$ | 1360 | mA | 3) |
| $I_{DD6}$ | 112 | mA | 4) |
| $I_{DD7}$ | 2080 | mA | 3) |

1) Calculated values from component data. ODT disabled. $I_{DD1}$, $I_{DD4R}$ and $I_{DD7}$ are defined with the outputs disabled.
2) $I_{DDX\,(rank)}$ = Number of components x $I_{DDX\,(component)}$
3) $I_{DDX} = I_{DDX\,(rank)}$ +(Rank-1)* $I_{DD2P\,(rank)}$
4) $I_{DDX}$ = Rank * $I_{DDX\,(rank)}$

# 5. Package Dimensions




Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only.

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