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HXMSH4GX03A1F1C-16K

204-Pin ECC Small Outline DDR3 SDRAM Modules
EU RoHS Compliant

Data Sheet

Rev. A

Revision History:		
Date	**Revision**	**Subjects (major changes since last revision)**
2016/03/01	A	Initial Release

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1 Overview

This chapter gives an overview of the 204-pin Small Outline DDR3 SDRAM modules with ECC product family and describes its main characteristics.

1.1 Features

- 204-Pin PC3-12800 Small Outline DDR3 SDRAM memory modules with ECC.
- Single rank 512M x 72 module organization, by 9pcs 512M x 8 chips organization.
- 4GB Modules built with 4Gbit DDR3 SDRAMs in chipsize package FBGA-78 ball.
- Standard Double-Data-Rate-Three Synchronous DRAMs (DDR3 SDRAM) with a single + 1.5 V (± 0.075 V) power supply.
- All speed grades faster than DDR3-1600 complies with DDR3-1600 timing specifications.
- Programmable CAS Latencies (6, 7, 8, 9, 10,11), Burst Length 8 (BL8),Burst Chop 4（BC4）.
- Auto Refresh (CBR) and Self Refresh.
- Auto Refresh for temperatures above 85 °C t_{REFI} = 3.9 µs.
- Programmable self refresh rate via MR2 setting.
- Programmable partial array refresh via MR2 settings.
- All inputs and outputs SSTL_1.5 compatible.
- Off-Chip Driver Impedance Adjustment (OCD) and On-Die Termination (ODT).
- Serial Presence Detect with E^2PROM.
- Small Outline DIMM Dimensions (nominal): 30 mm high, 67.6 mm wide
- Based on standard reference layouts.

TABLE 1
Module Performance Table

UniIC Speed Code			**–16K**	**Unit**	**Note**
DRAM Speed Grade		**DDR3**	**–1600**		
Module Speed Grade		**PC3**	**–12800**		
CAS-RCD-RP latencies			**11-11-11**	**t_{CK}**	
Max. Clock Frequency	CL8	f_{CK8}	533	MHz	
	CL9	f_{CK9}	667	MHz	
	CL10	f_{CK10}	667	MHz	
	CL11	f_{CK11}	800	MHz	
Min. RAS-CAS-Delay		t_{RCD}	13.75	ns	
Min. Row Precharge Time		t_{RP}	13.75	ns	
Min. Row Active Time		t_{RAS}	35	ns	
Min. Row Cycle Time		t_{RC}	48.75	ns	

1.2 Description

The UniIC HXMSH4GX03A1F1C-16K module family are Small Outline DIMM modules with ECC and 30 mm height based on DDR3 technology. DIMMs are available in 512M × 72 (4GB) in organization and density, intended for mounting into 204-pin connector sockets.

The memory array is designed with 4 Gbit Double-Data-Rate-Three (DDR3) Synchronous DRAMs. Decoupling capacitors are mounted on the PCB board. The DIMMs feature serial presence detect based on a serial E^2PROM device using the 2-pin I^2C protocol. The first 128 bytes are programmed with configuration data and are write-protected; the second 128 bytes are available to the customer.

green Product

TABLE 2
Ordering Information

Product Type[1)]	Compliance Code[2)]	Description	SDRAM Technology
PC3-12800 (11-11-11)			
HXMSH4GX03A1F1C-16K	4GB 1R×8 PC3-12800-11-11-11	1 Ranks	4Gbit (×8)

1) For detailed information regarding Product Type of UniIC please see chapter "Product Type Nomenclature" of this data sheet.
2) The Compliance Code is printed on the module label and describes the speed grade, for example "PC3–12800-11-11-11" where 12800 means DIMM modules with 12.8 GB/sec Module Bandwidth and "11-11-11" means Column Address Strobe (CAS) latency=11, Row Column Delay (RCD) latency = 11 and Row Precharge (RP) latency = 11.

TABLE 3
Address Format

DIMM Density	Module Organization	Memory Ranks	ECC/ Non-ECC	# of SDRAMs	# of row/bank/column bits
4GB	512M × 72	1	ECC	9	16/3/10

TABLE 4
Components on Modules

DRAM Components[1)2)]	DRAM Density	DRAM Organization
HXB15H4G800AF-13K	4Gbit	512M × 8

1) Green Product
2) For a detailed description of all functionalities of the DRAM components on these modules see the component data sheet.

2 Pin Configurations

2.1 Pin Configurations

The pin configuration of the 204-Pin Small Outline DDR3 SDRAM DIMM is listed by function in **Table 5** (204 pins). The abbreviations used in columns Pin Type and Buffer Type are explained in **Table 6** and **Table 7** respectively. The Pin numbering is depicted in **Figure 1**

TABLE 5
Pin Configuration of SO-DIMM

Symbol	Type	Description
Ax	Input	**Address inputs:** Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BAx) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. See the Pin Assignments Table for density-specific addressing information.
BAx	Input	**Bank address inputs:** Define the device bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command.
CKx, CKx#	Input	**Clock:** Differential clock inputs. All control, command, and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#.
CKEx	Input	**Clock enable:** Enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM.
DMx	Input	**Data mask (x8 devices only):** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with that input data, during a write access. Although DM pins are input-only, DM loading is designed to match that of the DQ and DQS pins.
ODTx	Input	**On-die termination:** Enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to the following pins: DQ, DQS, DQS#, DM, and CB. The ODT input will be ignored if disabled via the LOAD MODE command.
Par_In	Input	**Parity input:** Parity bit for Ax, RAS#, CAS#, and WE#.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with S#) define the command being entered.
RESET#	Input (LVCMOS)	**Reset:** RESET# is an active LOW asychronous input that is connected to each DRAM and the registering clock driver. After RESET# goes HIGH, the DRAM must be reinitialized as though a normal power-up was executed.
Sx#	Input	**Chip select:** Enables (registered LOW) and disables (registered HIGH) the command decoder.
SAx	Input	**Serial address inputs:** Used to configure the temperature sensor/SPD EEPROM address range on the I^2C bus.

SCL	Input	**Serial clock for temperature sensor/SPD EEPROM:** Used to synchronize communication to and from the temperature sensor/SPD EEPROM on the I^2C bus.
CBx	I/O	**Check bits:** Used for system error detection and correction.
DQx	I/O	**Data input/output:** Bidirectional data bus.
DQSx, DQSx#	I/O	**Data strobe:** Differential data strobes. Output with read data; edge-aligned with read data; input with write data; center-aligned with write data.

Symbol	Type	Description
SDA	I/O	**Serial data:** Used to transfer addresses and data into and out of the temperature sensor/SPD EEPROM on the I^2C bus.
TDQSx, TDQSx#	Output	**Redundant data strobe (x8 devices only):** TDQS is enabled/disabled via the LOAD MODE command to the extended mode register (EMR). When TDQS is enabled, DM is disabled and TDQS and TDQS# provide termination resistance; otherwise, TDQS# are no function.
Err_Out#	Output (open drain)	**Parity error output:** Parity error found on the command and address bus.
EVENT#	Output (open drain)	**Temperature event:**The EVENT# pin is asserted by the temperature sensor when critical temperature thresholds have been exceeded.
V_{DD}	Supply	**Power supply:** 1.5V ±0.075V. The component V_{DD} and V_{DDQ} are connected to the module V_{DD}.
V_{DDSPD}	Supply	**Temperature sensor/SPD EEPROM power supply:** 3.0–3.6V.
V_{REFCA}	Supply	**Reference voltage:** Control, command, and address $V_{DD}/2$.
V_{REFDQ}	Supply	**Reference voltage:** DQ, DM $V_{DD}/2$.
V_{SS}	Supply	Ground.
V_{TT}	Supply	**Termination voltage:** Used for control, command, and address $V_{DD}/2$.
NC	–	**No connect:** These pins are not connected on the module.
NF	–	**No function:** These pins are connected within the module, but provide no functionality.

TABLE 6
Abbreviations for pin Type

Abbreviation	Description
I	Standard input-only pin. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
PWR	Power
GND	Ground
NC	Not Connected

TABLE 7
Abbreviations for Buffer Type

Abbreviation	Description
SSTL	Serial Stub Terminated Logic (SSTL_15)
LV-CMOS	Low Voltage CMOS
CMOS	CMOS Levels
OD	Open Drain. The corresponding pin has 2 operational states, active low and tri-state, and allows multiple devices to share as a wire-OR.

FIGURE 1
Pin Configuration SO-DIMM (204 pin) with ECC

204-Pin DDR3 SODIMM Front							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{REFDQ}	53	V_{SS}	105	A1	157	DM5
3	V_{SS}	55	DQ24	107	A0	159	DQ42
5	DQ0	57	DQ25	109	V_{DD}	161	DQ43
7	DQ1	59	DM3	111	CK0	163	V_{SS}
9	V_{SS}	61	V_{SS}	113	CK0#	165	DQ48
11	DM0	63	DQ26	115	V_{DD}	167	DQ49
13	DQ2	65	DQ27	117	A10/AP	169	V_{SS}
15	DQ3	67	V_{SS}	119	BA0	171	DQS6#
17	V_{SS}	69	CB0	121	WE#	173	DQS6
19	DQ8	71	CB1	123	V_{DD}	175	V_{SS}
21	DQ9	73	V_{SS}	125	CAS#	177	DQ50
23	V_{SS}	75	DQS8#	127	S0#	179	DQ51
25	DQS1#	77	DQS8	129	S1#	181	V_{SS}
27	DQS1	79	V_{SS}	131	V_{DD}	183	DQ56
29	V_{SS}	81	CB2	133	DQ32	185	DQ57
31	DQ10	83	CB3	135	DQ33	187	V_{SS}
33	DQ11	85	V_{DD}	137	V_{SS}	189	DM7
35	V_{SS}	87	CKE0	139	DQS4#	191	DQ58
37	DQ16	89	CKE1	141	DQS4	193	DQ59
39	DQ17	91	BA2	143	V_{SS}	195	V_{SS}
41	V_{SS}	93	V_{DD}	145	DQ34	197	SA0
43	DQS2#	95	A12	147	DQ35	199	V_{DDSPD}
45	DQS2	97	A8	149	V_{SS}	201	SA1
47	V_{SS}	99	A5	151	DQ40	203	V_{TT}
49	DQ18	101	V_{DD}	153	DQ41	–	–
51	DQ19	103	A3	155	V_{SS}	–	–

204-Pin DDR3 SODIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
2	V_{SS}	54	DQ28	106	A2	158	V_{SS}
4	DQ4	56	DQ29	108	BA1	160	DQ46
6	DQ5	58	V_{SS}	110	V_{DD}	162	DQ47
8	V_{SS}	60	DQS3#	112	CK1	164	V_{SS}
10	DQS0#	62	DQS3	114	CK1#	166	DQ52
12	DQS0	64	V_{SS}	116	V_{DD}	168	DQ53
14	V_{SS}	66	DQ30	118	NC	170	V_{SS}
16	DQ6	68	DQ31	120	NC	172	DM6
18	DQ7	70	V_{SS}	122	RAS#	174	DQ54
20	V_{SS}	72	CB4	124	V_{DD}	176	DQ55
22	DQ12	74	CB5	126	ODT0	178	V_{SS}
24	DQ13	76	DM8	128	ODT1	180	DQ60
26	V_{SS}	78	V_{SS}	130	A13	182	DQ61
28	DM1	80	CB6	132	V_{DD}	184	V_{SS}
30	RESET#	82	CB7	134	DQ36	186	DQS7#
32	V_{SS}	84	V_{REFCA}	136	DQ37	188	DQS7
34	DQ14	86	V_{DD}	138	V_{SS}	190	V_{SS}
36	DQ15	88	A15	140	DM4	192	DQ62
38	V_{SS}	90	A14	142	DQ38	194	DQ63
40	DQ20	92	A9	144	DQ39	196	V_{SS}
42	DQ21	94	V_{DD}	146	V_{SS}	198	EVENT#
44	DM2	96	A11	148	DQ44	200	SDA
46	V_{SS}	98	A7	150	DQ45	202	SCL
48	DQ22	100	A6	152	V_{SS}	204	V_{TT}
50	DQ23	102	V_{DD}	154	DQS5#	–	–
52	V_{SS}	104	A4	156	DQS5	–	–

3 General Description

3.1 General Description

DDR3 SDRAM modules are high-speed, CMOS dynamic random access memory modules that use internally configured 4 or 8-bank DDR3 SDRAM devices. DDR3 SDRAM modules use DDR architecture to achieve high-speed operation. DDR3 architecture is essentially a 8*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR3 SDRAM module effectively consists of a single 8*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and eight corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

DDR3 modules use two sets of differential signals: DQS, DQS# to capture data and CK and CK# to capture commands, addresses, and control signals. Differential clocks and data strobes ensure exceptional noise immunity for these signals and provide precise crossing points to capture input signals. A bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR3 SDRAM device during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

DDR3 SDRAM modules operate from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

3.2 Serial Presence-Detect EEPROM Operation

DDR3 SDRAM modules incorporate serial presence-detect. The SPD data is stored in a 256-byte EEPROM. The first 128 bytes are programmed by UniIC to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I2C bus using the DIMM's SCL (clock) SDA (data), and SA (address) pins. Write protect (WP) is connected to VSS, permanently disabling hardware write protection.

4 Electrical Characteristics

This chapter contains speed grade definition, AC timing parameter and ODT tables.

4.1 Absolute Maximum Ratings

Attention: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TABLE 8
Absolute Maximum Ratings

Symbol	Parameter	Rating		Unit	Note
		Min.	Max.		
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}	–0.4	+1.975	V	
V_{DDQ}	Voltage on V_{DDQ} pin relative to V_{SS}	–0.4	+1.975	V	
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	–0.4	+1.975	V	

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to integrated circuit.

TABLE 9
Module Environmental Requirements

Parameter	Symbol	Values		Unit	Note
		Min.	Max.		
Operating temperature (ambient)	T_{OPR}	0	+65	℃	
Storage Temperature	T_{STG}	– 50	+100	℃	
Barometric Pressure (operating & storage)	PBar	+69	+105	kPa	1)

1) Up to 3000m.

TABLE 10
DRAM Component Operating Temperature Range

Symbol	Parameter	Rating		Unit	Note
		Min.	Max.		
T_{CASE}	Operating Temperature	0	95	°C	1)2)3)4)

1) Operating Temperature is the case surface temperature on the center / top side of the DRAM.
2) The operating temperature ranges are the temperatures where all DRAM specification will be supported. During operation, the DRAM case temperature must be maintained between 0 - 95 °C under all other specification parameters.
3) Above 85 ℃ the Auto-Refresh command interval has to be reduced to t_{REFI}= 3.9 µs
4) When operating this product in the 85 °C to 95 °C T_{CASE} temperature range, the High Temperature Self Refresh has to be enabled by setting EMR(2) bit A7 to “1”. When the High Temperature Self Refresh is enabled there is an increase of I_{DD6} by approximately 50%

4.2 Operating Conditions

TABLE 11
Supply Voltage Levels and AC / DC Operating Conditions

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Device Supply Voltage	V_{DD}	1.425	1.5	1.575	V	
Output Supply Voltage	V_{DDQ}	1.425	1.5	1.575	V	1)
Input Reference Voltage	V_{REF}	0.49 × V_{DDQ}	0.5 × V_{DDQ}	0.51 × V_{DDQ}	V	2)
SPD Supply Voltage	V_{DDSPD}	3	—	3.6	V	
DC Input Logic High	$V_{IH(DC)}$	V_{REF} + 0.1	—	V_{DDQ}	V	
DC Input Logic Low	$V_{IL\ (DC)}$)	vss	—	V_{REF} – 0.1	V	
AC Input Logic High	$V_{IH(AC)}$	V_{REF} + 0.175	—		V	
AC Input Logic Low	$V_{IL\ (AC)}$)		—	V_{REF} –0.175	V	
In / Output Leakage Current	I_L	– 5	—	5	µA	3)

1) Under all conditions, V_{DDQ} must be less than or equal to V_{DD}
2) Peak to peak AC noise on V_{REF} may not exceed ± 2% V_{REF} (DC). V_{REF} is also expected to track noise in V_{DDQ}.
3) Input voltage for any connector pin under test of 0 V ≤ V_{IN} ≤ V_{DDQ} + 0.3 V; all other pins at 0 V. Current is per pin

4.3 Module and Component Speed Grades

DDR3 components may exceed the listed module speed grades; module may not be available in all listed speed grades

TABLE 12
Module and Component Speed Grades

Module Speed Grade	Component Speed Grade
-16K	1600MHz

4.4 AC Timing Requirements

This chapter describes the AC timing requirements.

TABLE 13
AC Timing Requirements

Symbol	AC Characteristics Parameter	Min	Max	Unit
tCK(DLL_OFF)	Minimum Clock Cycle Time (DLL off mode)	8	-	ns
tCH(avg)	Average high pulse width	0.47	0.53	tCK(avg)
tCL(avg)	Average low pulse width	0.47	0.53	tCK(avg)
tDQSQ	DQS, DQS# to DQ skew, per group, per access	-	100	ps
tQH	DQ output hold time from DQS, DQS#	0.38	-	tCK(avg)
tDS(base)	Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels	10	-	ps
tDH(base)	Data hold time from DQS, DQS# referenced to Vih(dc) / Vil(dc) levels	45	-	ps
tDIPW	DQ and DM Input pulse width for each input	360	-	ps
tRPRE	DQS,DQS# differential READ Preamble	0.9	-	tCK(avg)
tRPST	DQS, DQS# differential READ Postamble	0.3	-	tCK(avg)
tQSH	DQS, DQS# differential output high time	0.40	-	tCK(avg)
tQSL	DQS, DQS# differential output low time	0.40	-	tCK(avg)
tWPRE	DQS, DQS# differential WRITE Preamble	0.9	-	tCK(avg)
tWPST	DQS, DQS# differential WRITE Postamble	0.3	-	tCK(avg)
tDQSCK	DQS, DQS# rising edge output access time from rising CK, CK#	-255	255	ps
tLZ	DQ, DQS and DQS# low-impedance time	-450	250	ps
tHZ	DQ, DQS and DQS# high-impedance time	-	250	ps
tDQSL	DQS, DQS# differential input low pulse width	0.45	0.55	tCK(avg)
tDQSH	DQS, DQS# differential input high pulse width	0.45	0.55	tCK(avg)
tDQSS	DQS, DQS# rising edge to CK, CK# rising edge	-0.27	0.27	tCK(avg)
tDSS	DQS, DQS# falling edge setup time to CK, CK# rising edge	0.18	-	tCK(avg)
tDSH	DQS, DQS# falling edge hold time from CK, CK# rising edge	0.18	-	tCK(avg)
tRTP	Internal READ Command to PRECHARGE Command delay	max(4nCK,7.5ns)	-	-
tWTR	Delay from start of internal write transaction to internal read command	max(4nCK,7.5ns)	-	-
tWR	WRITE recovery time	15	-	ns
tMRD	Mode Register Set command cycle time	4	-	nCK
tIS(base)	Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels	45	-	ps
tIH(base)	Command and Address hold time from CK, CK# referenced to Vih(dc) / Vil(dc) levels	120	-	ps
tXP	Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	max(3nCK,6ns)	-	-
tCKE	CKE minimum pulse width	max(3nCK,5.625ns)	-	-
tREFI	Average Periodic Refresh interval	85℃<TCASE <95℃ /3.9	0℃<TCASE <85℃ /7.8	us

4.5 I_{DD} Specifications and Conditions

List of tables defining I_{DD} Specifications and Conditions.

TABLE 14
I_{DD} Measurement Conditions

Parameter	Symbol	Note[1)2)3)4)5)]
Operating Current 0 One bank Active - Precharge; $t_{CK} = t_{CK.MIN}$, $t_{RC} = t_{RC.MIN}$, $t_{RAS} = t_{RAS.MIN}$, CKE is HIGH, CS is HIGH between valid commands. Address and control inputs are SWITCHING, Databus inputs are SWITCHING.	I_{DD0}	
Operating Current 1 One bank Active - Read - Precharge; I_{OUT} = 0 mA, BL = 4, $t_{CK} = t_{CK.MIN}$, $t_{RC} = t_{RC.MIN}$, $t_{RAS} = t_{RAS.MIN}$, $t_{RCD} = t_{RCD.MIN}$, AL = 0, CL = CL_{MIN}; CKE is HIGH, CS is HIGH between valid commands. Address and control inputs are SWITCHING, Databus inputs are SWITCHING.	I_{DD1}	6)
Precharge Standby Current All banks idle; CS is HIGH; CKE is HIGH; $t_{CK} = t_{CK.MIN}$; Other control and address inputs are SWITCHING, Databus inputs are SWITCHING.	I_{DD2N}	
Precharge Power-Down Current Other control and address inputs are STABLE, Data bus inputs are FLOATING.	I_{DD2P}	
Precharge Quiet Standby Current All banks idle; CS is HIGH; CKE is HIGH; $t_{CK} = t_{CK.MIN}$; Other control and address inputs are STABLE, Data bus inputs are FLOATING.	I_{DD2Q}	
Active Standby Current Burst Read: All banks open; Continuous burst reads; BL = 4; AL = 0, CL = CL_{MIN}; $t_{CK} = t_{CK.MIN}$; $t_{RAS} = t_{RAS.MAX}$, $t_{RP} = t_{RP.MIN}$; CKE is HIGH, CS is HIGH between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING; I_{OUT} = 0 mA.	I_{DD3N}	
Active Power-Down Current All banks open; $t_{CK} = t_{CK.MIN}$, CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are FLOATING.	I_{DD3P}	
Operating Current - Burst Read All banks open; Continuous burst reads; BL = 4; AL = 0, CL = CL_{MIN}; $t_{CK} = t_{CKMIN}$; $t_{RAS} = t_{RASMAX}$; $t_{RP} = t_{RPMIN}$; CKE is HIGH, CS is HIGH between valid commands; Address inputs are SWITCHING; Data bus inputs are SWITCHING; I_{OUT} = 0mA.	I_{DD4R}	6)
Operating Current - Burst Write All banks open; Continuous burst writes; BL = 4; AL = 0, CL = CL_{MIN}; $t_{CK} = t_{CK.MIN}$; $t_{RAS} = t_{RAS.MAX.}$, $t_{RP} = t_{RP.MAX}$; CKE is HIGH, CS is HIGH between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING;	I_{DD4W}	
Burst Refresh Current $t_{CK} = t_{CK.MIN.}$, Refresh command every $t_{RFC} = t_{RFC.MIN}$ interval, CKE is HIGH, CS is HIGH between valid commands, Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.	I_{DD5B}	

Parameter	Symbol	Note[1)2) 3)4)5)]
Self-Refresh Current CKE ≤ 0.2 V; external clock off, CK and $\overline{CK}$ at 0 V; Other control and address inputs are FLOATING, Data bus inputs are FLOATING. I_{DD6} current values are guaranteed up to T_{CASE} of 85 ℃ max.	I_{DD6}	
All Bank Interleave Read Current All banks are being interleaved at minimum t_{RC} without violating t_{RRD} using a burst length of 4. Control and address bus inputs are STABLE during DESELECTS. I_{out} = 0 mA.	I_{DD7}	6)

1) V_{DDQ} = 1.5 V ±0.1 V; V_{DD} = 1.5 V ±0.1 V
2) I_{DD} specifications are tested after the device is properly initialized and I_{DD} parameter are specified with ODT disabled.
3) Definitions for I_{DD} see **Table 16**
4) For two rank modules: All active current measurements in the same I_{DD} current mode. The other rank is in I_{DD2P} Precharge Power-Down Mode.
5) For details and notes see the relevant UniIC component data sheet.
6) I_{DD1}, I_{DD4R} and I_{DD7} current measurements are defined with the outputs disabled (I_{OUT} = 0 mA). To achieve this on module level the output buffers can be disabled using an EMRS(1) (Extended Mode Register Command) by setting A12 bit to HIGH.

TABLE 15
Definitions for I_{DD}

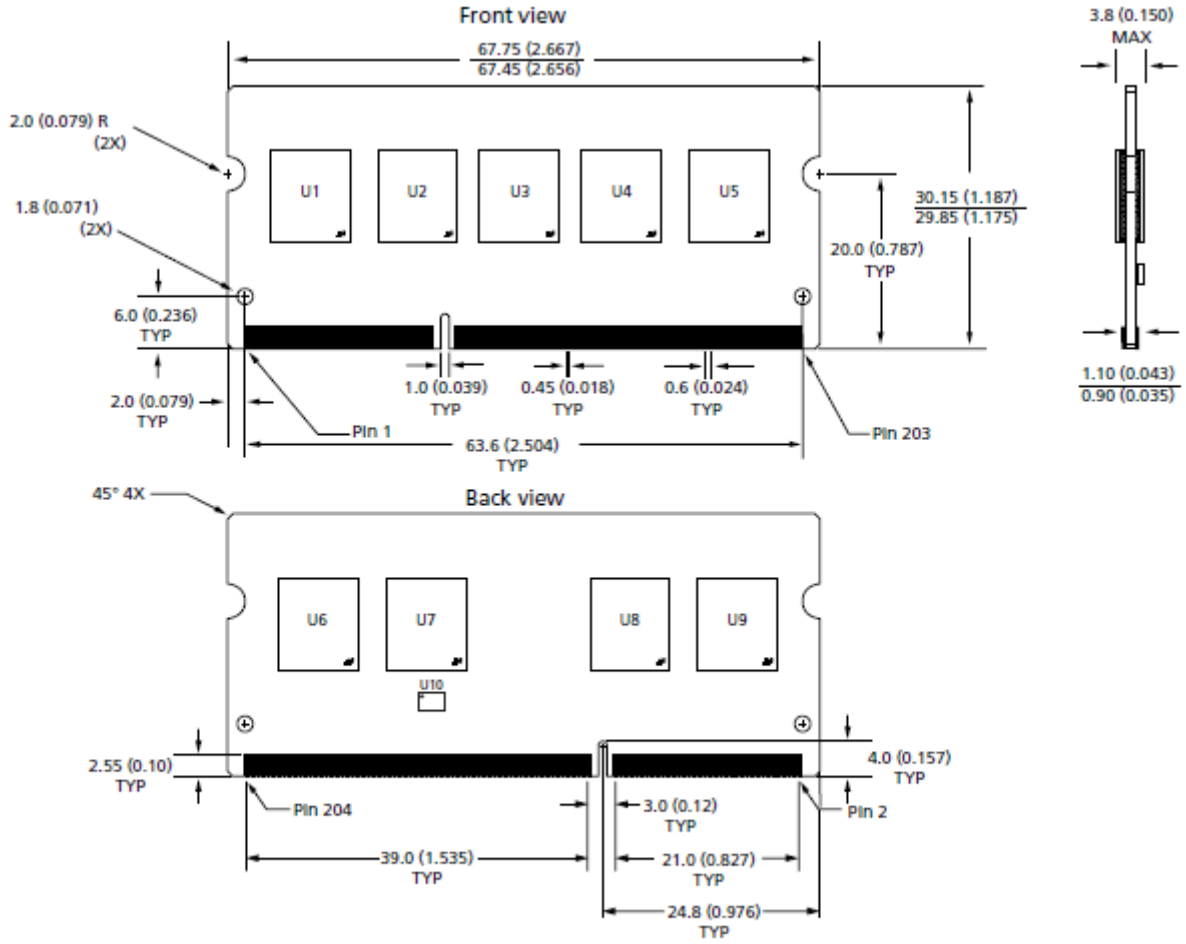
Parameter	Description
LOW	$V_{IN} \leq V_{IL(ac).MAX}$, HIGH is defined as $V_{IN} \geq V_{IH(ac).MIN}$
STABLE	Inputs are stable at a HIGH or LOW level.
FLOATING	Inputs are V_{REF} = V_{DDQ} /2
SWITCHING	Inputs are changing between HIGH and LOW every other clock (once per 2 cycles) for address and control signals, and inputs changing between HIGH and LOW every other data transfer (once per cycle) for DQ signals not including mask or strobes.

TABLE 16
IDD Specification for HXMSH4GX03A1F1C-16K

Product Type	HXMSH4GX03A1F1C-16K	**Unit**	**Note[1)2)]**
Organization	**4GB**		
	1Rank (×8)		
	×72		
	-16K		
Symbol	**Max.**		
I_{DD0}	585	mA	3)
I_{DD1}	720	mA	3)
I_{DD2N}	405	mA	4)
I_{DD2P0}	180	mA	4)
I_{DD2Q}	405	mA	4)
I_{DD3N}	495	mA	4)
I_{DD3P}	351	mA	4)
I_{DD4R}	1125	mA	3)
I_{DD4W}	1170	mA	3)
I_{DD5B}	2250	mA	3)
I_{DD6}	198	mA	4)
I_{DD7}	1890	mA	3)

1) Calculated values from component data. ODT disabled. $I_{DD1,}$ I_{DD4R} and I_{DD7} are defined with the outputs disabled.
2) $I_{DDX\ (rank)}$ = Number of components x $I_{DDX\ (component)}$
3) I_{DDX} = $I_{DDX\ (rank)}$ +(Rank-1)* $I_{DD2P\ (rank)}$
4) I_{DDX} = Rank * $I_{DDX\ (rank)}$

5. Package Dimensions



Notes: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only.

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