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SCE25D1G800AE(T/F)
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1Gbit DDR ECC SDRAM
EU RoHS Compliant Products

Data Sheet

Rev. H

Revision History		
Date	**Revision**	**Subjects (major changes since last revision)**
2014-07	A	Initial Release
2015-01	B	Updated tRFC and tXSNR timing
2015-06	C	1. Updated Power-up and initialization sequence 2. Add ECC description 3. Updated IDD's ,Include Automotive and High-Rel grade product.
2015-12	D	1. Updated Power-up and initialization sequence 2. Updated IOH value 3. Add AC timing parameter for DDR-266
2016-03	F	Change to UniIC Format
2016-04	G	1.Updated list of table and figure 2.Updated document format
2017-03	H	Modify the mistaken page header Format review (2020-05)

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Contents

1 Overview

This chapter gives an overview of the 1Gbit Double-Data-Rate ECC SDRAM product and describes its main characteristics.

1.1 Features

The 1-Gbit Double-Data-Rate ECC SDRAM offers the following key features:

- Double data rate architecture: two data transfers per clock cycle
- DDR ECC SDRAM special architecture:
  – 2 bits Error Detect and 1 bit Correct for all DQs
  – Long retention time for high reliability application
- Bidirectional data strobe (DQS) is transmitted and received with data, to be used in capturing data at the receiver
- DQS is edge-aligned with data for reads and is center-aligned with data for writes
- Differential clock inputs (CK and $\overline{CK}$)
- Four internal banks for concurrent operation
- Data mask (DM) for write data
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Programmable CAS latency: 2, 2.5, 3, 4
- Programmable burst lengths: 2, 4, or 8
- Programmable drive strength: normal, weak
- Auto Precharge option for each burst access
- Auto Refresh and Self Refresh Modes
- RAS-lockout supported
- 7.8 µs Maximum Average Periodic Refresh Interval
- 2.5 V (SSTL_2 compatible) I/O, All Functions Comply with JEDEC DDR SDRAM Standard
- V_{DD} = 2.5 V ±0.2 V
- V_{DDQ} = 2.5 V ±0.2 V
- Packages: TFBGA-60, TSOPII-66

Table 1 - Performance

Part Number Speed Code			–5B	–6B	-7A	Unit
Speed Grade			DDR400	DDR333	DDR266	—
Max. Clock Frequency	@CL3	f_{CK3}	200	—	—	MHz
	@CL2.5	$f_{CK2.5}$	166	166	—	MHz
	@CL2	f_{CK2}	133	133	133	MHz

1.2 Description

The 1Gbit Double-Data-Rate SDRAM is a high-speed CMOS, dynamic random-access memory containing 1,073,741,824 bits. It is internally configured as a eight-bank DRAM.

The 1Gbit Double-Data-Rate SDRAM uses a double- data-rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2n prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the 1Gbit Double-Data-Rate SDRAM effectively consists of a single 2n-bit wide, one clock cycle data transfer at the internal DRAM core and two corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR SDRAM during Reads and by the memory controller during Writes. DQS is edge-aligned with data for Reads and center-aligned with data for Writes.

The 1Gbit Double-Data-Rate SDRAM operates from a differential clock (CK and $\overline{CK}$; the crossing of CK going HIGH and $\overline{CK}$ going LOW is referred to as the positive edge of CK). Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the Active command are used to select the bank and row to be accessed. The address bits registered coincident with the Read or Write command are used to select the bank and the starting column location for the burst access.

The DDR SDRAM provides for programmable Read or Write burst lengths of 2, 4 or 8 locations. An Auto Precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access. As with standard SDRAMs, the pipelined, multibank architecture of DDR SDRAMs allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto refresh mode is provided along with a power-saving power-down mode. All inputs are compatible with the Industry Standard for SSTL_2. All outputs are SSTL_2, Class II compatible.

Note: The functionality described and the timing specifications included in this data sheet are for the DLL Enabled mode of operation.

Table 2 - Ordering Information for RoHS Compliant Products

Product Type[1]	Org.	Speed	CAS-RCD-RP Latencies[2][3][4]	Clock (MHz)	Package	Note[5]
Commercial Temperature Range (0 °C ~ +70 °C)						
DDR400B(3-3-3)						
SCE25D1G160AF-5B	×16	DDR400	3-3-3	200	TFBGA-60	
SCE25D1G800AF-5B	×8	DDR400	3-3-3	200	TFBGA-60	
SCE25D1G160AE-5B	×16	DDR400	3-3-3	200	TSOPII-66	
SCE25D1G800AE-5B	×8	DDR400	3-3-3	200	TSOPII-66	
DDR333B(2.5-3-3)						
SCE25D1G160AF-6B	×16	DDR333	2.5-3-3	166	TFBGA-60	
SCE25D1G800AF-6B	×8	DDR333	2.5-3-3	166	TFBGA-60	
SCE25D1G160AE-6B	×16	DDR333	2.5-3-3	166	TSOPII-66	
SCE25D1G800AE-6B	×8	DDR333	2.5-3-3	166	TSOPII-66	
DDR266A(2-2-2)						
SCE25D1G160AF-7A	×16	DDR266	2-2-2	133	TFBGA-60	
SCE25D1G800AF-7A	×8	DDR266	2-2-2	133	TFBGA-60	
SCE25D1G160AE-7A	×16	DDR266	2-2-2	133	TSOPII-66	
SCE25D1G800AE-7A	×8	DDR266	2-2-2	133	TSOPII-66	
Industrial Temperature Range (-40 °C ~ +85 °C)						
DDR400B(3-3-3)						
SCE25D1G160AF-5BI	×16	DDR400	3-3-3	200	TFBGA-60	
SCE25D1G800AF-5BI	×8	DDR400	3-3-3	200	TFBGA-60	
SCE25D1G160AE-5BI	×16	DDR400	3-3-3	200	TSOPII-66	
SCE25D1G800AE-5BI	×8	DDR400	3-3-3	200	TSOPII-66	
DDR333B(2.5-3-3)						
SCE25D1G160AF-6BI	×16	DDR333	2.5-3-3	166	TFBGA-60	
SCE25D1G800AF-6BI	×8	DDR333	2.5-3-3	166	TFBGA-60	
SCE25D1G160AE-6BI	×16	DDR333	2.5-3-3	166	TSOPII-66	
SCE25D1G800AE-6BI	×8	DDR333	2.5-3-3	166	TSOPII-66	
DDR266A(2-2-2)						
SCE25D1G160AF-7AI	×16	DDR266	2-2-2	133	TFBGA-60	
SCE25D1G800AF-7AI	×8	DDR266	2-2-2	133	TFBGA-60	
SCE25D1G160AE-7AI	×16	DDR266	2-2-2	133	TSOPII-66	
SCE25D1G800AE-7AI	×8	DDR266	2-2-2	133	TSOPII-66	

1) For detailed information regarding product type of UniIC please see chapter "Product Nomenclature" of this data sheet.
2) CAS: Column Address Strobe
3) RCD: Row Column Delay
4) RP: Row Precharge
5) RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers.

2 Configuration

This chapter contains the chip configuration and block diagrams.

2.1 Configuration for TFBGA-60

The ball configuration of a DDR SDRAM is listed by function in **Table 3**. The abbreviations used in the Ball#/Buffer Type column are explained in **Table 4** and **Table 5** respectively.

Table 3 - Configuration for TFBGA-60

Ball#	Name	Pin Type	Buffer Type	Function
Clock Signals				
G2	CK	I	SSTL	**Clock Signal**
G3	$\overline{CK}$	I	SSTL	**Complementary Clock Signal**
H3	CKE	I	SSTL	**Clock Enable**
Control Signals				
H7	$\overline{RAS}$	I	SSTL	**Row Address Strobe**
G8	$\overline{CAS}$	I	SSTL	**Column Address Strobe**
G7	$\overline{WE}$	I	SSTL	**Write Enable**
H8	$\overline{CS}$	I	SSTL	**Chip Select**
Address Signals				
J8	BA0	I	SSTL	**Bank Address Bus**
J7	BA1	I	SSTL	
K7	A0	I	SSTL	**Address Bus**
L8	A1	I	SSTL	
L7	A2	I	SSTL	
M8	A3	I	SSTL	
M2	A4	I	SSTL	
L3	A5	I	SSTL	
L2	A6	I	SSTL	
K3	A7	I	SSTL	
K2	A8	I	SSTL	
J3	A9	I	SSTL	
K8	A10	I	SSTL	
	AP	I	SSTL	
J2	A11	I	SSTL	
H2	A12	I	SSTL	
F9	A13	I	SSTL	

Ball#	Name	Pin Type	Buffer Type	Function
Data Signals ×8 Organization				
A8	DQ0	I/O	SSTL	**Data Signal Bus 7:0**
B7	DQ1	I/O	SSTL	
C7	DQ2	I/O	SSTL	
D7	DQ3	I/O	SSTL	
D3	DQ4	I/O	SSTL	
C3	DQ5	I/O	SSTL	
B3	DQ6	I/O	SSTL	
A2	DQ7	I/O	SSTL	
Data Strobe ×8 Organization				
E3	DQS	I/O	SSTL	**Data Strobe**
Data Mask ×8 Organization				
F3	DM	I	SSTL	**Data Mask**
Data Signals ×16 Organization				
A8	DQ0	I/O	SSTL	**Data Signal Bus 15:0**
B9	DQ1	I/O	SSTL	
B7	DQ2	I/O	SSTL	
C9	DQ3	I/O	SSTL	
C7	DQ4	I/O	SSTL	
D9	DQ5	I/O	SSTL	
D7	DQ6	I/O	SSTL	
E9	DQ7	I/O	SSTL	
E1	DQ8	I/O	SSTL	
D3	DQ9	I/O	SSTL	
D1	DQ10	I/O	SSTL	
C3	DQ11	I/O	SSTL	
C1	DQ12	I/O	SSTL	
B3	DQ13	I/O	SSTL	
B1	DQ14	I/O	SSTL	
A2	DQ15	I/O	SSTL	

Ball#	Name	Pin Type	Buffer Type	Function
Data Strobe ×16 Organization				
E3	UDQS	I/O	SSTL	**Data Strobe Upper Byte**
E7	LDQS	I/O	SSTL	**Data Strobe Lower Byte**
Data Mask ×16 Organization				
F3	UDM	I	SSTL	**Data Mask Upper Byte**
F7	LDM	I	SSTL	**Data Mask Lower Byte**
Power Supplies				
F1	V_{REF}	AI	—	**I/O Reference Voltage**
A9, B2, C8, D2, E8	V_{DDQ}	PWR	—	**I/O Driver Power Supply**
A7, F8, M7	V_{DD}	PWR	—	**Power Supply**
A1, B8, C2, D8, E2	V_{SSQ}	PWR	—	**I/O Driver Power Supply_GND**
A3, F2, M3	V_{SS}	PWR	—	**Power Supply_GND**
Not Connected ×8 Organization				
B1, B9, C1, C9, D1, D9, E1, E7, E9, F7	NC	NC	—	**Not Connected**

Table 4 - Abbreviations for Ball Type

Abbreviation	Description
I	Standard input-only pin. Digital levels
O	Output. Digital levels
I/O	I/O is a bidirectional input/output signal
AI	Input. Analog levels
PWR	Power
GND	Ground
NC	Not Connected

Table 5 - Abbreviations for Buffer Type

Abbreviation	Description
SSTL	Serial Stub Terminated Logic (SSTL2)
LV-CMOS	Low Voltage CMOS
CMOS	CMOS Levels
OD	Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR

Figure 1 - Configuration for x8 Organization, TFBGA-60, Top View

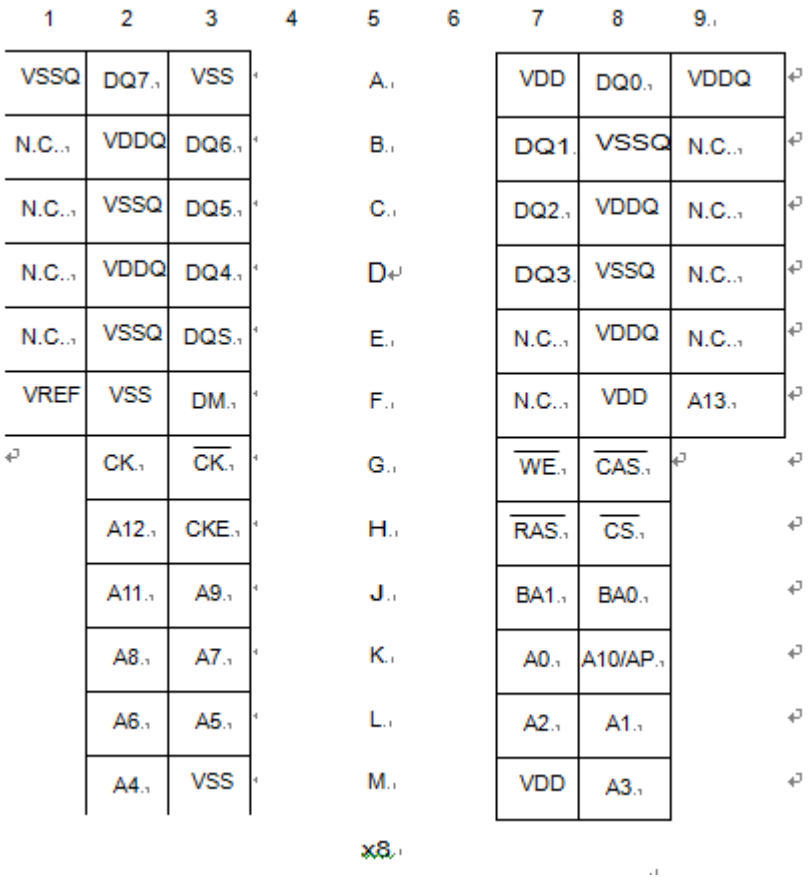
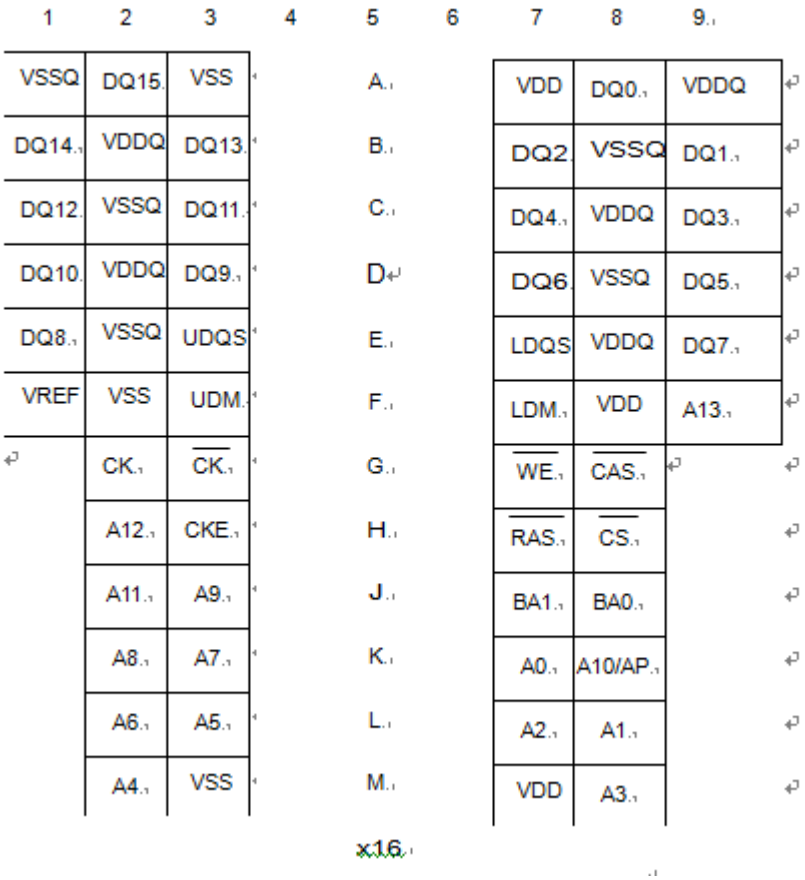


Figure 2 - Configuration for x16 Organization, TFBGA-60, Top View



2.2 Configuration for TSOPII-66

The pin configuration of a DDR SDRAM is listed by function in **Table 6**. The abbreviations used in the Pin#/Buffer Type column are explained in **Table 7** and **Table 8** respectively.

Table 6 - Configuration for TSOPII-66

Pin#	Name	Pin Type	Buffer Type	Function
Clock Signals				
45	CK	I	SSTL	**Clock Signal**
46	$\overline{CK}$	I	SSTL	**Complementary Clock Signal**
44	CKE	I	SSTL	**Clock Enable**
Control Signals				
23	$\overline{RAS}$	I	SSTL	**Row Address Strobe**
22	$\overline{CAS}$	I	SSTL	**Column Address Strobe**
21	$\overline{WE}$	I	SSTL	**Write Enable**
24	$\overline{CS}$	I	SSTL	**Chip Select**
Address Signals				
26	BA0	I	SSTL	**Bank Address Bus**
27	BA1	I	SSTL	
29	A0	I	SSTL	**Address Bus**
30	A1	I	SSTL	
31	A2	I	SSTL	
32	A3	I	SSTL	
35	A4	I	SSTL	
36	A5	I	SSTL	
37	A6	I	SSTL	
38	A7	I	SSTL	
39	A8	I	SSTL	
40	A9	I	SSTL	
28	A10	I	SSTL	
	AP	I	SSTL	
41	A11	I	SSTL	
42	A12	I	SSTL	
17	A13	I	SSTL	
Data Signals ×8 Organization				
2	DQ0	I/O	SSTL	**Data Signal Bus 7:0**
5	DQ1	I/O	SSTL	
8	DQ2	I/O	SSTL	
11	DQ3	I/O	SSTL	
56	DQ4	I/O	SSTL	
59	DQ5	I/O	SSTL	
62	DQ6	I/O	SSTL	
65	DQ7	I/O	SSTL	
Data Strobe ×8 Organization				
51	DQS	I/O	SSTL	**Data Strobe**

Pin#	Name	Pin Type	Buffer Type	Function
Data Mask ×8 Organization				
47	DM	I	SSTL	**Data Mask**
Data Signals ×16 Organization				
2	DQ0	I/O	SSTL	**Data Signal Bus 15:0**
4	DQ1	I/O	SSTL	
5	DQ2	I/O	SSTL	
7	DQ3	I/O	SSTL	
8	DQ4	I/O	SSTL	
10	DQ5	I/O	SSTL	
11	DQ6	I/O	SSTL	
13	DQ7	I/O	SSTL	
54	DQ8	I/O	SSTL	
56	DQ9	I/O	SSTL	
57	DQ10	I/O	SSTL	
59	DQ11	I/O	SSTL	
60	DQ12	I/O	SSTL	
62	DQ13	I/O	SSTL	
63	DQ14	I/O	SSTL	
65	DQ15	I/O	SSTL	
Data Strobe ×16 Organization				
51	UDQS	I/O	SSTL	**Data Strobe Upper Byte**
16	LDQS	I/O	SSTL	**Data Strobe Lower Byte**
Data Mask ×16 Organization				
47	UDM	I	SSTL	**Data Mask Upper Byte**
20	LDM	I	SSTL	**Data Mask Lower Byte**
Power Supplies				
49	V_{REF}	AI	—	**I/O Reference Voltage**
3, 9, 15, 55, 61	V_{DDQ}	PWR	—	**I/O Driver Power Supply**
1, 18, 33	V_{DD}	PWR	—	**Power Supply**
6, 12, 52, 58, 64	V_{SSQ}	PWR	—	**I/O Driver Power Supply_GND**
34,48, 66	V_{SS}	PWR	—	**Power Supply_GND**
Not Connected ×8 Organization				
4, 7, 10, 13, 14, 16, 19, 20, 25, 43, 50, 53, 54, 57, 60, 63	NC	NC	—	
Not Connected ×16 Organization				
14, 19, 25, 43, 50, 53	NC	NC	—	

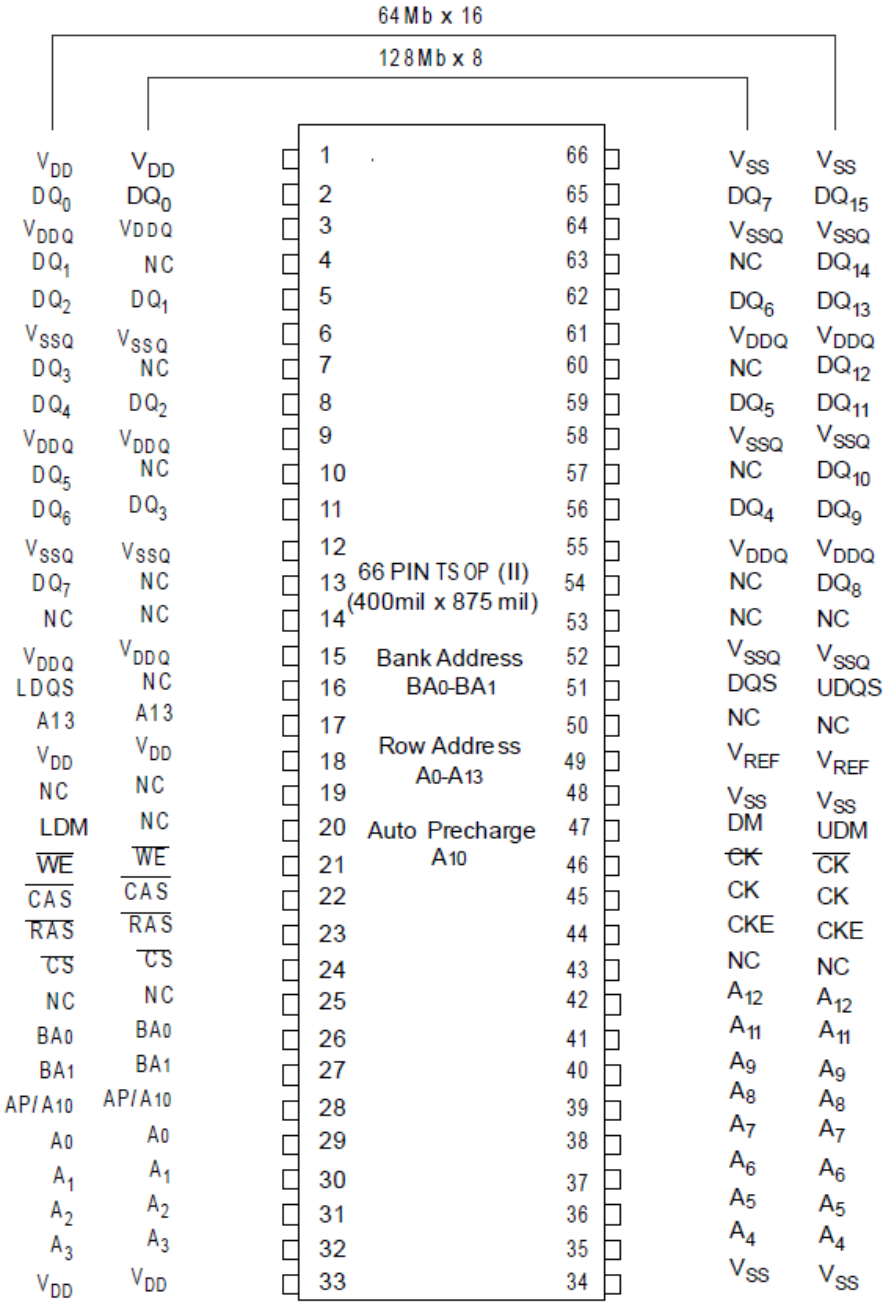
Table 7 - Abbreviations for Pin Type

Abbreviation	Description
I	Standard input-only pin. Digital levels
O	Output. Digital levels
I/O	I/O is a bidirectional input/output signal
AI	Input. Analog levels
PWR	Power
GND	Ground
NC	Not Connected

Table 8 - Abbreviations for Buffer Type

Abbreviation	Description
SSTL	Serial Stub Terminalted Logic (SSTL2)
LV-CMOS	Low Voltage CMOS
CMOS	CMOS Levels
OD	Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR

Figure 3 - Configuration for TSOPII-66, Top View



3 Functional Description

The 1Gbit Double-Data-Rate SDRAM uses a double-data-rate architecture to achieve high-speed operation.

3.1 Power-up and initialization sequence

The following sequence is required for Power-up and Initialization.

1. Simultaneously apply power to VDD and VDDQ.
2. Apply VREF and then VTT power. VTT must be applied after VDDQ to avoid device latchup, which may cause permanent damage to the device. Except for CKE, inputs are not recognized as valid until after VREF is applied.
3. Assert and hold CKE at a LVCMOS logic LOW. Maintaining an LVCMOS LOW level on CKE during power-up is required to ensure that the DQ and DQS outputs will be in the High-Z state, where they will remain until driven in normal operation (by a read access).
4. Provide stable clock signals.
5. Wait at least 200µ s.
6. Bring CKE HIGH, and provide at least one NOP or DESELECT command. At this point, the CKE input changes from a LVCMOS input to a SSTL_2 input only and will remain a SSTL_2 input unless a power cycle occurs.
7. Perform a PRECHARGE ALL command.
8. Wait at least tRP time; during this time NOPs or DESELECT commands must be given.
9. Using the MRS command, program the extended mode register (bit0 = 0 to enable the DLL and bit1 = 0 for normal drive; or bit1 = 1 for reduced drive and bit2 – bit*n* must be set to 0 [where *n* = most significant bit]).
10. Wait at least tMRD time; only NOPs or DESELECT commands are allowed.
11. Using the MRS command, program the mode register to set operating parameters and to reset the DLL. At least 200 clock cycles are required between a DLL reset and any READ command.
12. Wait at least tMRD time; only NOPs or DESELECT commands are allowed.
13. Issue a PRECHARGE ALL command.
14. Wait at least tRP time; only NOPs or DESELECT commands are allowed.
15. Issue an AUTO REFRESH command. This may be moved prior to step 13.
16. Wait at least tRFC time; only NOPs or DESELECT commands are allowed.
17. Issue an AUTO REFRESH command. This may be moved prior to step 13.
18. Wait at least tRFC time; only NOPs or DESELECT commands are allowed.
19. Although not required by the UniIC device, JEDEC requires an MRS command to clear the DLL bit (set bit8 = 0). If an MRS command is issued, the same operating parameters should be utilized as in step 11.
20. Wait at least tMRD time; only NOPs or DESELECT commands are supported.
21. At this point the DRAM is ready for any valid command. At least 200 clock cycles with CKE HIGH are required between step 11 (DLL RESET) and any READ command.

3.2 Mode Register Definition

The Mode Register is used to define the specific mode of operation of the DDR SDRAM.

BA1	BA0	A13 A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	Operating MODE						CL			BT	BL		

Table 9 - Mode Register Definition

Field	Bits	Description
BL	[2:0]	**Burst Length** *Note: All other bit combinations are RESERVED.* 001_B **2** 010_B **4** 011_B **8**
BT	3	**Burst Type** 0 Sequential 1 Interleaved
CL	[6:4]	**CAS Latency** *Note: All other bit combinations are RESERVED.* 010_B **2** 110_B **2.5** 011_B **3** 100_B **4**
MODE	[13:7]	**Operating Mode** *Note: All other bit combinations are RESERVED.* 0000000 Normal Operation without DLL Reset 0000010 Normal Operation with DLL Reset

3.2.1 Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit A3. The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in **Table 10**.

Table 10 - Burst Definition

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
	A2	A1	A0	Type = Sequential	Type = Interleaved
2			0	0-1	0-1
			1	1-0	1-0
4		0	0	0-1-2-3	0-1-2-3
		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
8	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

Notes
1. For a burst length of two, A1-Ai selects the two-data-element block; A0 selects the first access within the block.
2. For a burst length of four, A2-Ai selects the four-data-element block; A0-A1 selects the first access within the block.
3. For a burst length of eight, A3-Ai selects the eight-data- element block; A0-A2 selects the first access within the block.
4. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.

3.3 Extended Mode Register

The Extended Mode Register controls functions beyond those controlled by the Mode Register.

BA1	BA0	A13 A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	1	Operating MODE											DS	DLL

Table 11 - Extended Mode Register

Field	Bits	Description
DLL	0	**DLL Status** 0_B **Enabled** 1_B **Disabled**
DS	1	**Drive Strength** 0_B **Normal** 1_B **Weak**
MODE	[13:2]	**Operating Mode** 000000000000_B **Normal Operation** **Notes** *1. A2 must be 0 to provide compatibility with early DDR devices.* *2. All other bit combinations are RESERVED.*

4 Truth Tables

The truth tables in this chapter summarize the commands and there signal coding to control a standard Double-Data-Rate SDRAM.

Table 12 - Truth Table 1: Commands

Name (Function)	CS	RAS	CAS	WE	Address	Note
Deselect (NOP)	H	X	X	X	X	1)2)
No Operation (NOP)	L	H	H	H	X	1)2)
Active (Select Bank And Activate Row)	L	L	H	H	Bank/Row	1)3)
Read (Select Bank And Column, And Start Read Burst)	L	H	L	H	Bank/Col	1)4)
Write (Select Bank And Column, And Start Write Burst)	L	H	L	L	Bank/Col	1)4)
Burst Terminate	L	H	H	L	X	1)5)
Precharge (Deactivate Row In Bank Or Banks)	L	L	H	L	Code	1)6)
Auto Refresh Or Self Refresh (Enter Self Refresh Mode)	L	L	L	H	X	1)7)8)10)
Mode Register Set	L	L	L	L	Op-Code	1)9)

1) CKE is HIGH for all commands shown except Self Refresh.
2) Deselect and NOP are functionally interchangeable.
3) BA0, BA1 provide bank address and A0 - Ai provide row address.
4) BA0, BA1 provide bank address; A0 - Ai provide column address; A10 HIGH enables the Auto Precharge feature (nonpersistent), A10 LOW disables the Auto Precharge feature.
5) Applies only to read bursts with Auto Precharge disabled; this command is undefined (and should not be used) for read bursts with Auto Precharge enabled or for write bursts.
6) A10 LOW: BA0, BA1 determine which bank is precharged. A10 HIGH: all banks are precharged and BA0, BA1 are “Don’t Care”.
7) This command is AUTO REFRESH if CKE is HIGH; Self Refresh if CKE is LOW
8) Internal refresh counter controls row and bank addressing; all inputs and I/Os are “Don’t Care” except for CKE.
9) BA0, BA1 select either the Base or the Extended Mode Register (BA0 = 0, BA1 = 0 selects Mode Register; BA0 = 1, BA1 = 0 selects Extended Mode Register; other combinations of BA0-BA1 are reserved; A0 – A13 provide the op-code to be written to the selected Mode Register.
10) V_{REF} must be maintained during Self Refresh operation.

Table 13 - Truth Table 2: DM Operation

Name (Function)	DM	DQs	Note
Write Enable	L	Valid	1)
Write Inhibit	H	X	

1) Used to mask write data; provided coincident with the corresponding data.

Table 14 - Truth Table 3: Clock Enable (CKE)

Current State	CKE n-1	CKEn	Command n	Action n	Notes[3)-7)]
	Previous Cycle	Current Cycle			
Self Refresh	L	L	X	Maintain Self-Refresh	1)
Self Refresh	L	H	Deselect or NOP	Exit Self-Refresh	1)2)
Power Down	L	L	X	Maintain Power-Down	
Power Down	L	H	Deselect or NOP	Exit Power-Down	
All Banks Idle	H	L	Deselect or NOP	Precharge Power-Down Entry	
All Banks Idle	H	L	AUTO REFRESH	Self Refresh Entry	
Bank(s) Active	H	L	Deselect or NOP	Active Power-Down Entry	
	H	H	See **Table 15**		

1) V_{REF} must be maintained during Self Refresh operation
2) Deselect or NOP commands should be issued on any clock edges occurring during the Self Refresh Exit (t_{XSNR} *or* t_{XSRD}) period. A minimum of 200 clock cycles are needed before applying a read command to allow the DLL to lock to the input clock.
3) CKEn is the logic state of CKE at clock edge n; CKEn--1 was the state of CKE at the previous clock edge.
4) Current state is the state of the DDR SDRAM immediately prior to clock edge n.
5) COMMANDn is the command registered at clock edge n, and ACTIONn is a result of COMMANDn.
6) All states and sequences not shown are illegal or reserved.
7) Operation or timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.

Table 15 - Truth Table 4: Current State Bank n - Command to Bank n (same bank)

Current State	CS	RAS	CAS	WE	Command	Action	Notes[1)-6),12)]
Any	H	X	X	X	Deselect	NOP. Continue previous operation.	
	L	H	H	H	No Operation	NOP. Continue previous operation.	
Idle	L	L	H	H	Active	Select and activate row	
	L	L	L	H	AUTO REFRESH		7)
	L	L	L	L	MODE REGISTER SET		7)
Row Active	L	H	L	H	Read	Select column and start Read burst	8)
	L	H	L	L	Write	Select column and start Write burst	8)
	L	L	H	L	Precharge	Deactivate row in bank(s)	9)
Read (Auto Precharge Disabled)	L	H	L	H	Read	Select column and start new Read burst	8)
	L	L	H	L	Precharge	Truncate Read burst, start Precharge	9)
	L	H	H	L	BURST TERMINATE		10)
Write (Auto Precharge Disabled)	L	H	L	H	Read	Select column and start Read burst	8)11)
	L	H	L	L	Write	Select column and start Write burst	8)
	L	L	H	L	Precharge	Truncate Write burst, start Precharge	9)11)

1) This table applies when CKE n-1 was HIGH and CKE n is HIGH. and after tXSNR or tXSRD has been met (if the previous state was self refresh.2) This table is bank-specific, except where noted, i.e., the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state. Exceptions are covered in the notes below.
3) Current state definitions:
   Idle: The bank has been precharged, and t_{RP} has been met.
   Row Active: A row in the bank has been activated, and t_{RCD} has been met. No data bursts/accesses and no register accesses are in progress.
   Read: A Read burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
   Write: A Write burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
4) The following states must not be interrupted by a command issued to the same bank. DESELECT or NOP commands, or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and according to **Table 16**.
   Precharging: Starts with registration of a Precharge command and ends when t_{RP} is met. Once t_{RP} is met, the bank is in the idle state.
   Row Activating: Starts with registration of an Active command and ends when t_{RCD} is met. Once t_{RCD} is met, the bank is in the "row active" state.
   Read w/Auto Precharge Enabled: Starts with registration of a Read command with Auto Precharge enabled and ends when t_{RP} has been met. Once t_{RP} is met, the bank is in the idle state.
   Write w/Auto Precharge Enabled: Starts with registration of a Write command with Auto Precharge enabled and ends when t_{RP} has been met. Once t_{RP} is met, the bank is in the idle state.
5) The following states must not be interrupted by any executable command; Deselect or NOP commands must be applied on each positive clock edge during these states.
   Refreshing: Starts with registration of an Auto Refresh command and ends when t_{RFC} is met. Once t_{RFC} is met, the DDR SDRAM is in the "all banks idle" state.
   Accessing Mode Register: Starts with registration of a Mode Register Set command and ends when t_{MRD} has been met. Once t_{MRD} is met, the DDR SDRAM is in the "all banks idle" state.
   Precharging All: Starts with registration of a Precharge All command and ends when t_{RP} is met. Once t_{RP} is met, all banks is in the idle state.
6) All states and sequences not shown are illegal or reserved.
7) Not bank-specific; requires that all banks are idle and no bursts are in progress.
8) Reads or Writes listed in the Command/Action column include Reads or Writes with Auto Precharge enabled and Reads or Writes with Auto Precharge disabled.
9) May or may not be bank-specific; if all/any banks are to be precharged, all/any must be in a valid state for precharging.
10) Not bank-specific; BURST TERMINATE affects the most recent Read burst, regardless of bank.
11) Requires appropriate DM masking.
12) Operation or timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.

Table 16 - Truth Table 5: Current State Bank n - Command to Bank m (different bank)

Current State	CS	RAS	CAS	WE	Command	Action	Notes[1)-6),11)]
Any	H	X	X	X	Deselect	NOP. Continue previous operation	
	L	H	H	H	No Operation	NOP. Continue previous operation	
Idle	X	X	X	X	Any Command Otherwise Allowed to Bank m		
Row Activating, Active, or Precharging	L	L	H	H	Active	Select and activate row	
	L	H	L	H	Read	Select column and start Read burst	7)
	L	H	L	L	Write	Select column and start Write burst	7)
	L	L	H	L	Precharge		
Read (Auto Precharge Disabled)	L	L	H	H	Active	Select and activate row	
	L	H	L	H	Read	Select column and start new Read burst	7)
	L	L	H	L	Precharge		
Write (Auto Precharge Disabled)	L	L	H	H	Active	Select and activate row	
	L	H	L	H	Read	Select column and start Read burst	7)8)
	L	H	L	L	Write	Select column and start new Write burst	7)
	L	L	H	L	Precharge		
Read (With Auto Precharge)	L	L	H	H	Active	Select and activate row	
	L	H	L	H	Read	Select column and start new Read burst	7)9)
	L	H	L	L	Write	Select column and start Write burst	7)9)10)
	L	L	H	L	Precharge		
Write (With Auto Precharge)	L	L	H	H	Active	Select and activate row	
	L	H	L	H	Read	Select column and start Read burst	7)9)
	L	H	L	L	Write	Select column and start new Write burst	7)9)
	L	L	H	L	Precharge		

1) This table applies when CKE n-1 was HIGH and CKE n is HIGH (see **Table 14**: Clock Enable (CKE) and after t_{XSNR}/t_{XSRD} has been met, if the previous state was self refresh)
2) This table describes alternate bank operation, except where noted, i.e., the current state is for bank n and the commands shown are those allowed to be issued to bank m (assuming that bank m is in such a state that the given command is allowable). Exceptions are covered in the notes below.
3) Current state definitions:
   Idle: The bank has been precharged, and t_{RP} has been met.
   Row Active: A row in the bank has been activated, and t_{RCD} has been met. No data bursts/accesses and no register accesses are in progress.
   Read: A Read burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
   Write: A Write burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
4) AUTO REFRESH and Mode Register Set commands may only be issued when all banks are idle.
5) A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.
6) All states and sequences not shown are illegal or reserved.
7) Reads or Writes listed in the Command/Action column include Reads or Writes with Auto Precharge enabled and Reads or Writes with Auto Precharge disabled.
8) Requires appropriate DM masking.
9) Concurrent Auto Precharge:This device supports “Concurrent Auto Precharge”. When a read with auto precharge or a write with auto precharge is enabled any command may follow to the other banks as long as that command does not interrupt the read or write data transfer and all other limitations apply (e.g. contention between READ data and WRITE data must be avoided). The minimum delay from a read or write command with auto precharge enable, to a command to a different banks is summarized in **Table 17**.
10) A Write command may be applied after the completion of data output.
11) Operation or timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.

Table 17 - Truth Table 6: Concurrent Auto Precharge

From Command	To Command (different bank)	Minimum Delay with Concurrent Auto Precharge Support	Unit
WRITE w/AP	Read or Read w/AP	1 + (BL/2) + t_{WTR}	t_{CK}
	Write to Write w/AP	BL/2	t_{CK}
	Precharge or Activate	1	t_{CK}
Read w/AP	Read or Read w/AP	BL/2	t_{CK}
	Write or Write w/AP	CL (rounded up) + BL/2	t_{CK}
	Precharge or Activate	1	t_{CK}

5 Electrical Characteristics

This chapter describes the electrical characteristics.

5.1 Operating Conditions

This chapter contains the operating conditions tables.

Table 18 - Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Voltage on I/O pins relative to V_{SS}	V_{IN}, V_{OUT}	–0.5	—	V_{DDQ} + 0.5	V	—
Voltage on inputs relative to V_{SS}	V_{IN}	–1	—	+3.6	V	—
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}	–1	—	+3.6	V	—
Voltage on V_{DDQ} supply relative to V_{SS}	V_{DDQ}	–1	—	+3.6	V	—
Operating temperature (ambient)	T_A	0	—	+70	℃	Commercial
		–40	—	+85	℃	Industrial
Storage temperature (plastic)	T_{STG}	–55	—	+150	℃	—
Power dissipation (per SDRAM component)	P_D	—	1	—	W	—
Short circuit output current	I_{OUT}	—	50	—	mA	—

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Table 19 - Input and Output Capacitances

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Input Capacitance: CK, $\overline{CK}$	C_{I1}	2.0	—	3.0	pF	TSOPII[1)]
		1.5	—	2.5	pF	TFBGA [1)]
Delta Input Capacitance	C_{dI1}	—	—	0.25	pF	[1)]
Input Capacitance: All other input-only pins	C_{I2}	1.5	—	2.5	pF	TFBGA [1)]
		2.0	—	3.0	pF	TSOPII [1)]
Delta Input Capacitance: All other input-only pins	C_{dIO}	—	—	0.5	pF	[1)]
Input/Output Capacitance: DQ, DQS, DM	C_{IO}	3.5	—	4.5	pF	TFBGA [1)2)]
		4.0	—	5.0	pF	TSOPII [1)2)]
Delta Input/Output Capacitance: DQ, DQS, DM	C_{dIO}	—	—	0.5	pF	[1)]

1) These values are guaranteed by design and are tested on a sample base only. $V_{DDQ} = V_{DD} = 2.5\ V \pm 0.2\ V$, f = 100 MHz, $T_A = 25\ °C$, $V_{OUT(DC)} = V_{DDQ}/2$, V_{OUT} (Peak to Peak) 0.2 V. Unused pins are tied to ground.
2) DM inputs are grouped with I/O pins reflecting the fact that they are matched in loading to DQ and DQS to facilitate trace matching at the board level.

Table 20 - Electrical Characteristics and DC Operating Conditions

Parameter	Symbol	Values			Unit	Note/Test Condition [1]
		Min.	Typ.	Max.		
Device Supply Voltage	V_{DD}	2.3	2.5	2.7	V	
Output Supply Voltage	V_{DDQ}	2.3	2.5	2.7	V	[2]
Input Reference Voltage	V_{REF}	0.49 × V_{DDQ}	0.5 × V_{DDQ}	0.51 × V_{DDQ}	V	[3]
I/O Termination Voltage (System)	V_{TT}	V_{REF} – 0.04		V_{REF} + 0.04	V	[4]
Input High (Logic1) Voltage	$V_{IH.DC}$	V_{REF} + 0.15		V_{DDQ} + 0.3	V	[5]
Input Low (Logic0) Voltage	$V_{IL.DC}$	–0.3		V_{REF} – 0.15	V	[5]
Input Voltage Level, CK and $\overline{CK}$ Inputs	$V_{IN.DC}$	–0.3		V_{DDQ} + 0.3	V	[5]
Input Differential Voltage, CK and $\overline{CK}$ Inputs	$V_{ID.DC}$	0.36		V_{DDQ} + 0.6	V	[5][6]
VI-Matching Pull-up Current to Pull-down Current	VI_{Ratio}	0.71		1.4	—	[7]
Input Leakage Current	I_I	–2		2	µA	Any input 0 V ≤ V_{IN} ≤ V_{DD}; All other pins not under test = 0 V [8]
Output Leakage Current	I_{OZ}	–5		5	µA	DQs are disabled; 0 V ≤ V_{OUT} ≤ V_{DDQ} [8]
Output High Current, Normal Strength Driver	I_{OH}	-16.2		—	mA	V_{OUT} = 1.95 V
Output Low Current, Normal Strength Driver	I_{OL}	16.2		—	mA	V_{OUT} = 0.35 V

1) 0 °C ≤ T_A ≤ 70 °C; V_{DD} = V_{DDQ} = 2.5 V ± 0.2 V
2) Under all conditions, V_{DDQ} must be less than or equal to V_{DD}.
3) V_{REF} is expected to be equal to 0.5*VDDQ of the transmitting device, and to track variations in the dc level of the same. Peak to peak AC noise on V_{REF} may not exceed ± 2% $V_{REF.DC}$. V_{REF} is also expected to track noise variations in V_{DDQ}.
4) V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}.
5) Inputs are not recognized as valid until V_{REF} stabilizes.
6) V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.
7) The ratio of the pull-up current to the pull-down current is specified for the same temperature and voltage, over the entire temperature and voltage range, for device drain to source voltage from 0.25 to 1.0 V. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.
8) Values are shown per pin.

5.2 AC Characteristics

Notes 1-5 apply to the following Tables; Electrical Characteristics and DC Operating Conditions, AC Operating Conditions, I_{DD} Specifications and Conditions, and Electrical Characteristics and AC Timing.

Notes

1. All voltages referenced to VSS.
2. Tests for AC timing, IDD, and electrical, AC and DC characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. **Figure 4** represents the timing reference load used in defining the relevant timing parameters of the part. It is not intended to be either a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. System designers will use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers will correlate to their production test conditions (generally a coaxial transmission line terminated at the tester electronics).
4. AC timing and IDD tests may use a VIL to VIH swing of up to 1.5 V in the test environment, but input timing is still referenced to VREF (or to the crossing point for CK, $\overline{CK}$), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals is 1 V/ns in the range between VIL(AC) and VIH(AC).
5. The AC and DC input level specifications are as defined in the SSTL_2 Standard (i.e. the receiver effectively switches as a result of the signal crossing the AC input level, and remains in that state as long as the signal does not ring back above (below) the DC input LOW (HIGH) level).
6. For System Characteristics like Setup & Holdtime Derating for Slew Rate, I/O Delta Rise/Fall Derating, DDR SDRAM Slew Rate Standards, Overshoot & Undershoot specification and Clamp V-I characteristics see the latest Industry specification for DDR components.

Figure 4 - AC Output Load Circuit Diagram / Timing Reference Load

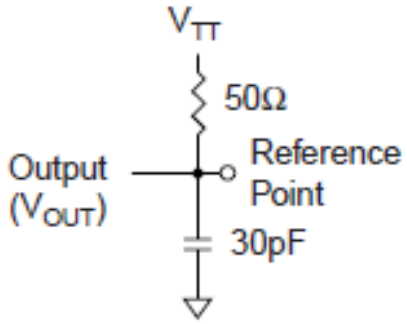


Table 21 - AC Operating Conditions

Parameter	Symbol	Values		Unit	Note/ Test Condition[1)2)3)]
		Min.	Max.		
Input High (Logic 1) Voltage, DQ, DQS and DM Signals	$V_{IH.AC}$	V_{REF} + 0.31	—	V	
Input Low (Logic 0) Voltage, DQ, DQS and DM Signals	$V_{IL.AC}$	—	V_{REF} – 0.31	V	
Input Differential Voltage, CK and $\overline{CK}$ Inputs	$V_{ID.AC}$	0.7	V_{DDQ} + 0.6	V	4)
Input Closing Point Voltage, CK and $\overline{CK}$ Inputs	$V_{IX.AC}$	0.5 × V_{DDQ}– 0.2	0.5 × V_{DDQ}+ 0.2	V	5)

1) 0 °C ≤ T_A ≤ 70 °C; V_{DD} = V_{DDQ} = 2.5 V ± 0.2 V
2) Input slew rate = 1 V/ns.
3) Inputs are not recognized as valid until V_{REF} stabilizes.
4) V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.
5) The value of V_{IX} is expected to equal 0.5 × V_{DDQ} of the transmitting device and must track variations in the DC level of the same.

Table 22 - AC Timing - Absolute Specifications

Parameter	Symbol	–5B		–6B		-7A		Unit	Note/ Test Condition [1)-5)20)]
		DDR400		DDR333		DDR266			
		Min.	Max.	Min.	Max.	Min.	Max.		
DQ output access time from CK/$\overline{CK}$	t_{AC}	–0.7	+0.7	–0.7	+0.7	-0.75	+0.75	ns	
CK high-level width	t_{CH}	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	
Clock cycle time	t_{CK}	—	—	—	—	—	—		12)
		5	7.5	—	—	—	—	ns	CL = 3.0 12)
		6	12	6	12	7.5	12	ns	CL = 2.5 12)
		7.5	12	7.5	12	7.5	12	ns	CL = 2.0 12)
CK low-level width	t_{CL}	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	
Auto precharge write recovery + precharge time	t_{DAL}	Min. : (t_{WR}/t_{CK})+(t_{RP}/t_{CK}) Max. : —						t_{CK}	6)
DQ and DM input hold time	t_{DH}	0.4	—	0.45	—	0.5	—	ns	13)
DQ and DM input pulse width (each input)	t_{DIPW}	1.75	—	1.75	—	1.75	—	ns	9)
DQS output access time from CK/$\overline{CK}$	t_{DQSCK}	–0.6	+0.6	–0.6	+0.6	-0.75	+0.75	ns	
DQS input low (high) pulse width (write cycle)	$t_{DQSL,H}$	0.35	—	0.35	—	0.35	—	t_{CK}	
DQS-DQ skew (DQS and associated DQ signals)	t_{DQSQ}	—	+0.40	—	+0.45	—	+0.5	ns	TSOPII 14)
DQS-DQ skew (DQS and associated DQ signals)	t_{DQSQ}	—	+0.40	—	+0.40	—	+0.5	ns	TFBGA 14)
Write command to 1st DQS latching transition	t_{DQSS}	0.72	1.25	0.75	1.25	0.75	1.25	t_{CK}	

Parameter	Symbol	–5B		–6B		-7A		Unit	Note/ Test Condition 1)-5)20)
		DDR400		DDR333		DDR266			
		Min.	Max.	Min.	Max.	Min.	Max.		
DQ and DM input setup time	t_{DS}	0.4	—	0.45	—	0.5	—	ns	13)
DQS falling edge hold time from CK (write cycle)	t_{DSH}	0.2	—	0.2	—	0.2	—	t_{CK}	
DQS falling edge to CK setup time (write cycle)	t_{DSS}	0.2	—	0.2	—	0.2	—	t_{CK}	
Clock Half Period	t_{HP}	min(t_{CL}, t_{CH})	—	min (t_{CL}, t_{CH})	—	min (t_{CL}, t_{CH})	—	ns	15)16)
Data-out high-impedance time from CK/$\overline{CK}$	t_{HZ}	—	+0.7	—	+0.7	—	+0.75	ns	7)
Address and control input hold time	t_{IH}	0.6	—	0.75	—	0.9	—	ns	fast slew rate 8)9)
		0.7	—	0.8	—	1.0	—	ns	slow slew rate 8)9)
Control and Addr. input pulse width (each input)	t_{IPW}	2.2	—	2.2	—	2.2	—	ns	9)
Address and control input setup time	t_{IS}	0.6	—	0.75	—	0.9	—	ns	fast slew rate 8)9)
		0.7	—	0.8	—	1.0	—	ns	slow slew rate 8)9)
Data-out low-impedance time from CK/$\overline{CK}$	t_{LZ}	–0.7	+0.7	–0.7	+0.7	–0.75	+0.75	ns	7)
Mode register set command cycle time	t_{MRD}	2	—	2	—	2	—	t_{CK}	
DQ/DQS output hold time from DQS	t_{QH}	t_{HP}–t_{QHS}	—	t_{HP} –t_{QHS}	—	t_{HP} –t_{QHS}	—	ns	16)
Data hold skew factor	t_{QHS}	—	+0.50	—	+0.55	—	+0.75	ns	TSOPII 16)
Data hold skew factor	t_{QHS}	—	+0.50	—	+0.50	—	+0.75	ns	TFBGA 16)
Active to Autoprecharge delay	t_{RAP}	t_{RCD}	—	t_{RCD}	—	t_{RCD}	—	ns	
Active to Precharge command	t_{RAS}	40	70E+3	42	70E+3	45	120E+3	ns	
Active to Active/Auto-refresh command period	t_{RC}	55	—	60	—	65	—	ns	
Active to Read or Write delay	t_{RCD}	15	—	18	—	20	—	ns	
Average Periodic Refresh Interval	t_{REFI}	—	7.8	—	7.8	—	7.8	µs	13)17)
Auto-refresh to Active/Auto-refresh command period	t_{RFC}	120	—	120	—	120	—	ns	
Precharge command period	t_{RP}	15	—	18	—	20	—	ns	
Read preamble	t_{RPRE}	0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}	18)
Read postamble	t_{RPST}	0.40	0.60	0.40	0.60	0.40	0.60	t_{CK}	18)
Active bank A to Active bank B command	t_{RRD}	10	—	12	—	15	—	ns	

Parameter	Symbol	–5B		–6B		-7A		Unit	Note/ Test Condition 1)-5)20)
		DDR400		DDR333		DDR266			
		Min.	Max.	Min.	Max.	Min.	Max.		
Write preamble	t_{WPRE}	Max. (0.25 × t_{CK}, 1.5 ns)	—	Max. (0.25× t_{CK}, 1.5 ns)	—	Max. (0.25× t_{CK}, 1.5 ns)	—	ns	
Write preamble setup time	t_{WPRES}	0	—	0	—	0	—	ns	10)
Write postamble	t_{WPST}	0.40	0.60	0.40	0.60	0.40	0.60	t_{CK}	11)
Write recovery time	t_{WR}	15	—	15	—	15	—	ns	
Internal write to read command delay	t_{WTR}	2	—	1	—	1	—	t_{CK}	
Exit self-refresh to non-read command	t_{XSNR}	126	—	126	—	127.5	—	ns	19)
Exit self-refresh to read command	t_{XSRD}	200	—	200	—	200	—	t_{CK}	

1) 0 °C ≤ T_A ≤ 70 °C; V_{DD} = V_{DDQ} = 2.5 V ± 0.2 V
2) Input slew rate ≥ 1 V/ns.
3) The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross: the input reference level for signals other than CK/$\overline{CK}$, is V_{REF}. CK/$\overline{CK}$ slew rate are ≥ 1.0 V/ns.
4) Inputs are not recognized as valid until V_{REF} stabilizes.
5) The Output timing reference level is V_{TT}.
6) For each of the terms, if not already an integer, round to the next highest integer. t_{CK} is equal to the actual system clock cycle time.
7) t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).
8) Fast slew rate ≥ 1.0 V/ns , slow slew rate ≥ 0.5 V/ns and < 1 V/ns for command/address and CK & $\overline{CK}$ slew rate > 1.0 V/ns, measured between $V_{IH.AC}$ and $V_{IL.AC}$.
9) These parameters guarantee device timing, but they are not necessarily tested on each device. They may be guaranteed by device design or tester correlation.
10) The specific requirement is that DQS be valid (HIGH,LOW, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW at this time, depending on t_{DQSS}.
11) The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.
12) The only time that the clock frequency is allowed to change is during self--refresh mode.
13) If refresh timing or tDS/tDH is violated, data corruption may occur and the data must be re--written with valid data before a valid READ can be executed.
14) tDQSQ Consists of data pin skew and output pattern effects, and p--channel to n--channel variation of the output drivers for any given cycle.
15) 24.Min (tCL, tCH) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for tCL and tCH.
16) tQH = tHP - tQHS, where: tHP = minimumhalf clock period for any given cycle and is defined by clock high or clock low (tCH, tCL). tQHS accounts for 1) The pulse duration distortion of on-chip clock circuits; and 2) The worst case push-out of DQS on one transition followed by the worst case pull-in of DQon the next transition, both of which are, separately, due to data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers.
17) A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM device.
18) tRPST end point and tRPREbegin point are not referenced to a specific voltage level but specify when the device output is no longer driving (tRPST), or begins driving (tRPRE).
19) In all circumstances, tXSNR can be satisfied using tXSNR = tRFCmin + 1*tCK.
20) Operation or timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAMmust be powered down and then restarted through the specified initialization sequence before normal operation can continue.

5.3 IDD Specification

Table 23 - IDD Conditions

Parameter	Symbol
Operating Current: one bank; active/ precharge; $t_{RC} = t_{RCMIN}$; $t_{CK} = t_{CKMIN}$; DQ, DM, and DQS inputs changing once per clock cycle; address and control inputs changing once every two clock cycles. $\overline{CS}$ = high between valid commands.	I_{DD0}
Operating Current: one bank; active/read/precharge; Burst = 4; $\overline{CS}$ = high between valid commands.	I_{DD1}
Precharge Power-Down Standby Current: all banks idle; power-down mode; CKE $\leq V_{ILMAX}$; $t_{CK} = t_{CKMIN}$; $V_{IN} = V_{REF}$ for DQ, DQS and DM	I_{DD2P}
Precharge Floating Standby Current: $\overline{CS} \geq V_{IHMIN}$, all banks idle; CKE $\geq V_{IHMIN}$; $t_{CK} = t_{CKMIN}$, address and other control inputs changing once per clock cycle, $V_{IN} = V_{REF}$ for DQ, DQS and DM.	I_{DD2F}
Precharge Quiet Standby Current: $\overline{CS} \geq V_{IHMIN}$, all banks idle; CKE $\geq V_{IHMIN}$; $t_{CK} = t_{CKMIN}$, address and other control inputs stable at $\geq V_{IHMIN}$ or $\leq V_{ILMAX}$; $V_{IN}=V_{REF}$ for DQ, DQS and DM.	I_{DD2Q}
Active Power-Down Standby Current: one bank active; power-down mode; CKE $\leq V_{ILMAX}$; $t_{CK}= t_{CKMIN}$; $V_{IN} = V_{REF}$ for DQ, DQS and DM.	I_{DD3P}
Active Standby Current: one bank active; $\overline{CS} \geq V_{IHMIN}$; CKE $\geq V_{IHMIN}$; $t_{RC} = t_{RASMAX}$; $t_{CK} = t_{CKMIN}$; DQ, DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	I_{DD3N}
Operating Current: one bank active; Burst = 2; reads; continuous burst; address and control inputs changing once per clock cycle; 50% of data outputs changing on every clock edge; CL = 2 for DDR200 and DDR266A, CL = 3 for DDR333; $t_{CK} = t_{CKMIN}$; I_{OUT} = 0 mA	I_{DD4R}
Operating Current: one bank active; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; 50% of data outputs changing on every clock edge; CL = 2 for DDR200 and DDR266A, CL = 3 for DDR333; $t_{CK} = t_{CKMIN}$	I_{DD4W}
Auto-Refresh Current: $t_{RC} = t_{RFCMIN}$, burst refresh	I_{DD5}
Self-Refresh Current: CKE $\leq$ 0.2 V; external clock on; $t_{CK} = t_{CKMIN}$	I_{DD6}
Operating Current: four bank; four bank interleaving with BL = 4	I_{DD7}

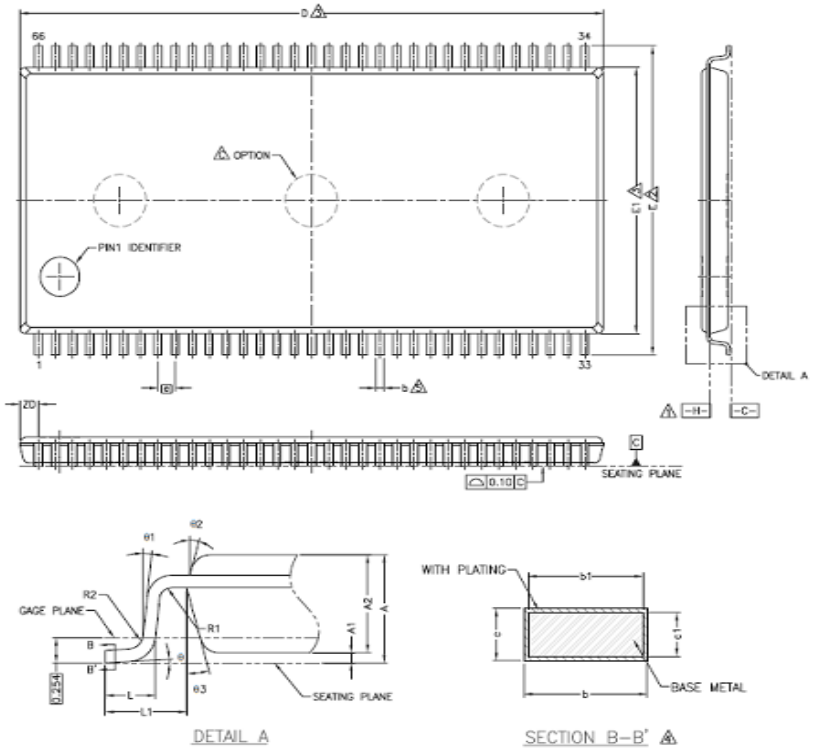
Table 24 - IDD Specification

Symbol	–5B	–6B	-7A	Unit	Note[1)2)3)]
	DDR400	DDR333	DDR266		
	Max.	Max.	Max.		
I_{DD0}	90	75	70	mA	×8
	95	85	80	mA	×16
I_{DD1}	105	90	80	mA	×8
	125	110	95	mA	×16
I_{DD2P}	12	12	12	mA	×8
	12	12	12	mA	×16
I_{DD2F}	45	40	35	mA	×8
	45	40	35	mA	×16
I_{DD2Q}	40	35	35	mA	×8
	40	35	35	mA	×16
I_{DD3P}	45	40	35	mA	×8
	50	45	45	mA	×16
I_{DD3N}	65	55	50	mA	×8
	70	65	60	mA	×16
I_{DD4R}	130	115	100	mA	×8
	185	155	135	mA	×16
I_{DD4W}	125	105	95	mA	×8
	170	140	125	mA	×16
I_{DD5}	190	175	165	mA	×8
	190	175	160	mA	×16
I_{DD6} [4)]	14	14	14	mA	×8
	14	14	14	mA	×16
I_{DD7}	220	180	155	mA	×8
	260	220	190	mA	×16

1) Test conditions : V_{DD} = 2.7 V, T_A = 95 °C.
2) I_{DD} specifications are tested after the device is properly initialized.
3) This version IDD value just for reference.
4) Enables on-chip refresh and address counters.

6 Package Outlines

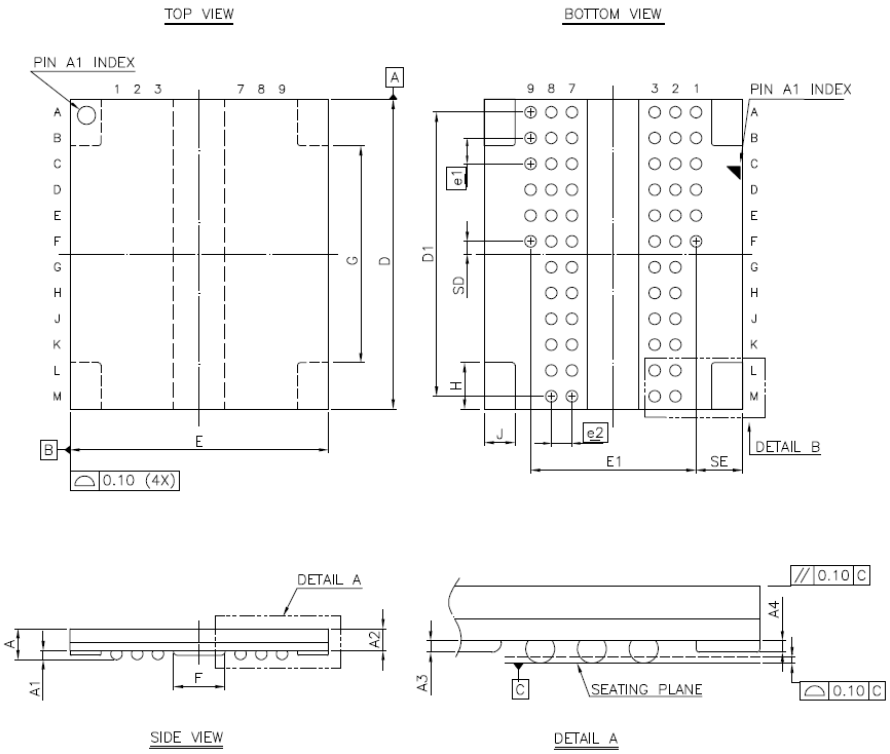
Figure 5 - Package Outline PG-TSOPII-66

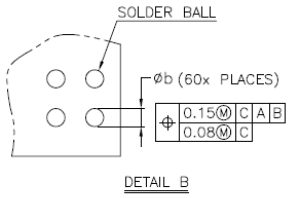


SYM.	DIMENSION (MM)			DIMENSION (INCH)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	–	–	1.20	–	–	0.047
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.22	–	0.38	0.009	–	0.015
b1	0.22	0.30	0.33	0.009	0.012	0.013
c	0.12	–	0.21	0.005	–	0.008
c1	0.10	0.127	0.16	0.004	0.005	0.006
D	22.22 BSC			0.875 BSC		
ZD	0.71 REF			0.028 REF		
E	11.76 BSC			0.463 BSC		
E1	10.16 BSC			0.400 BSC		
L	0.40	0.50	0.60	0.016	0.020	0.024
L1	0.80 REF			0.031 REF		
e	0.65 BSC			0.026 BSC		
R1	0.12	–	–	0.005	–	–
R2	0.12	–	0.25	0.005	–	0.010
θ	0°	–	8°	0°	–	8°
θ1	0°	–	–	0°	–	–
θ2	10°	15°	20°	10°	15°	20°
θ3	10°	15°	20°	10°	15°	20°

NOTE:
1. DATUM PLANE -H- COINCIDENT WITH BOTTOM OF LEAD, WHERE LEAD EXITS BODY.
2. TO BE DETERMINED AT SEATING PLANE -C- .
3. DIMENSION D AND E1 ARE DETERMINED AT DATUM -H- .
   DIMENSION D DOES NOT INCLUDE MOLD PROTRUSIONS OR GATE BURRS. MOLD PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE.
   DIMENSION E1 DOES NOT INCLUDE INTERLEAD MOLD PROTRUSIONS. INTERLEAD MOLD PROTRUSIONS SHALL NOT EXCEED 0.25mm PER SIDE.
4. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.
6. CONTROLLING DIMENSION: MILLIMETER.
7. REFER TO JEDEC STD MS-024, FC.

Figure 6 - Package Outline PG-TFBGA-60





SYM.	DIMENSION (mm)			DIMENSION (inch)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.30	0.35	0.40	0.012	0.014	0.016
A2	—	—	0.84	—	—	0.033
A3	0.10	0.15	0.20	0.004	0.006	0.008
A4	0.18	0.20	0.22	0.007	0.008	0.009
b	0.40	0.45	0.50	0.016	0.018	0.020
D	11.90	12.00	12.10	0.469	0.472	0.476
D1	11.00 BSC			0.433 BSC		
E	9.90	10.00	10.10	0.390	0.394	0.398
E1	6.40 BSC			0.252 BSC		
F	2.00 BSC			0.079 BSC		
G	8.40 BSC			0.331 BSC		
H	1.80 BSC			0.071 BSC		
J	1.20 BSC			0.047 BSC		
SD	0.50 BSC			0.020 BSC		
SE	1.80 BSC			0.071 BSC		
e1	1.00 BSC			0.039 BSC		
e2	0.80 BSC			0.031 BSC		

NOTE:
1. CONTROLLING DIMENSION : MILLIMETER.
2. REFERENCE DOCUMENT : JEDEC MO-207.

7 Product Nomenclature

For reference the UniIC SDRAM component nomenclature is enclosed in this chapter.

Table 25 - Examples for Nomenclature Fields

Example for	Field Number										
	1	2	3	4	5	6	7	8	9	10	11
DDR SDRAM	SCE	25	D	1G	16	0	A	F	–	6B	I

Table 26 - DDR Memory Components

Field	Description	Values	Coding
1	UniIC Component Prefix	SCB	UniIC Commercial Memory components
		SCE	UniIC ECC Memory components
		SCX	UniIC Robustness ECC Memory components
2	Interface Voltage [V]	25	SSTL_2, + 2.5 V (± 0.2 V)
3	DRAM Technology	D	DDR
4	Component Density [Mbit]	32	32 Mbit
		64	64 Mbit
		128	128 Mbit
		256	256 Mbit
		1G	1 Gbit
5	Number of I/Os	40	× 4
		80	× 8
		16	× 16
6	Product Variant	0	monolithic
		2	2 die stack
		4	4 die stack
7	Die Revision	A	First
		B	Second
		C	Third
8	Package, Lead-Free Status	E	TSOPII, lead-free
		T	TSOPII, Black
		F	FBGA, lead-free
9	Power	–	Standard power product
		L	Low power product
10	Speed Grade	–5B	DDR–400 3–3–3
		–6B	DDR–333 2.5–3–3
		–7A	DDR–266 2–2–2
11	Temperature range [1)]	Blank	Commercial temperature range (0°C – +70 °C)
		I	Industrial temperature range (-40°C – +85 °C)
		A2	Automotive temperature range, A2: -40 °C to 105 °C
		A3	Automotive temperature range, A3: -40 °C to 95 °C
		X	High-Rel temperature range: -55 °C to 125 °C

1) Double-Refresh rate required for operation >105°C.

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